FAST CMOS 18-BIT REGISTER

IDT74FCT162823AT/CT

FEATURES:

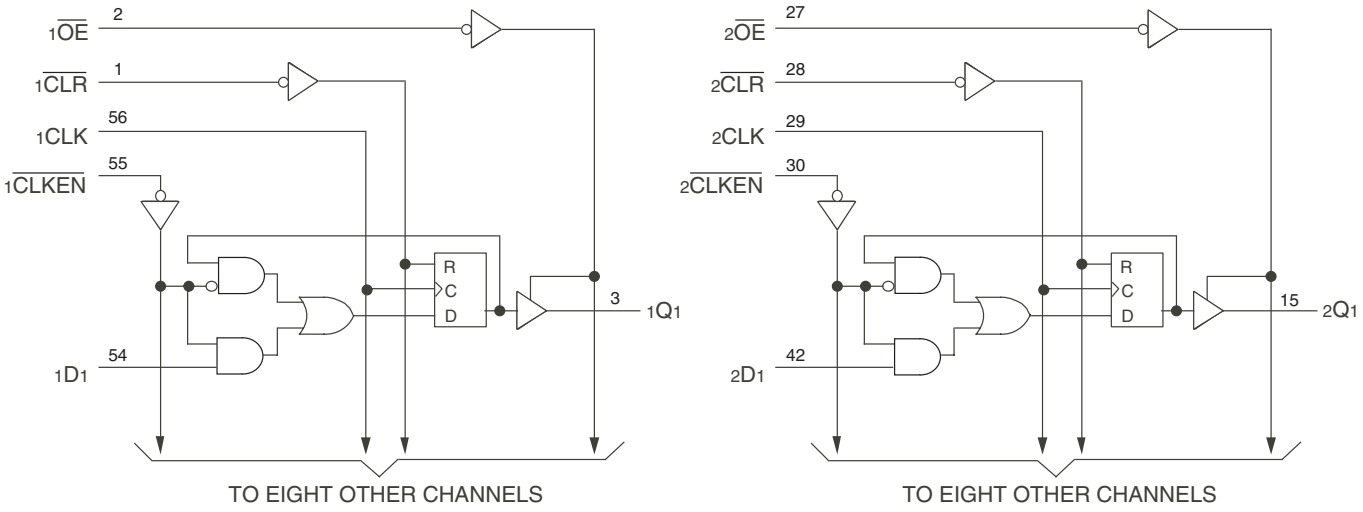
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- Low input and output leakage ≤1µA (max.)
- V_{CC} = 5V ±10%
- Balanced Output Drivers of ±24mA
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- Available in SSOP and TSSOP packages

DESCRIPTION:

The FCT162823T 18-bit bus interface register is built using advanced, dual metal CMOS technology. These high-speed, low-power registers with clock enable (x$\overline{CLKEN}$) and clear (x$\overline{CLR}$) controls are ideal for parity bus interfacing in high-performance synchronous systems. The control inputs are organized to operate the device as two 9-bit registers or one 18-bit register. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162823T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times – reducing the need for external series terminating resistors. The FCT162823T is a plug-in replacement for the FCT16823T and ABT16823 for on-board interface applications.

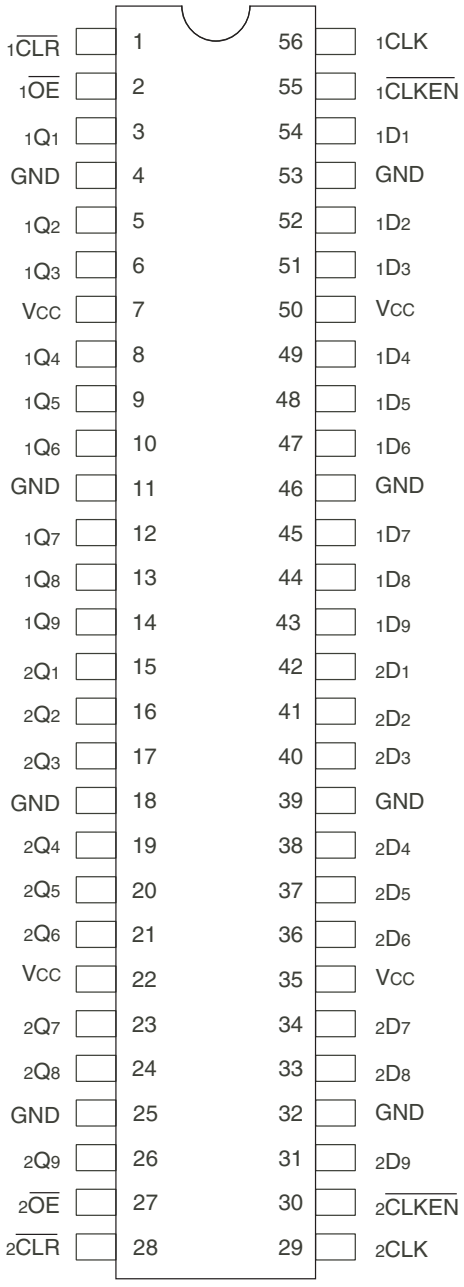
FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to 7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Outputs and I/O terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xCLK	Clock Inputs
$x\overline{CLKEN}$	Clock Enable Inputs (Active LOW)
$x\overline{CLR}$	Asynchronous clear Inputs (Active LOW)
$x\overline{OE}$	Output Enable Inputs (Active LOW)
xOx	3-State Outputs

FUNCTION TABLE(1)

Inputs					Outputs	
$x\overline{OE}$	$x\overline{CLR}$	$x\overline{CLKEN}$	xCLK	xDx	xQx	Function
H	X	X	X	X	Z	High Z
L	L	X	X	X	L	Clear
L	H	H	X	X	Q(2)	Hold
H	H	L	↑	L	Z	Load
H	H	L	↑	H	Z	
L	H	L	↑	L	L	
L	H	L	↑	H	H	

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
2. Output level before indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[4]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[4]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[4]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[4]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max		—	5	500	µA
I_{CCH}		V_{IN} = GND or V_{CC}					
I_{CCZ}							

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –24mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}					
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 24mA	—	0.3	0.55	V
		V_{IN} = V_{IH} or V_{IL}					

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = $x\overline{CLKEN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = $x\overline{CLKEN}$ = GND at fi = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = $x\overline{CLKEN}$ = GND at fi = 2.5MHz 50% Duty Cycle Eighteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	4.2	7.1[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	22.1[5]	

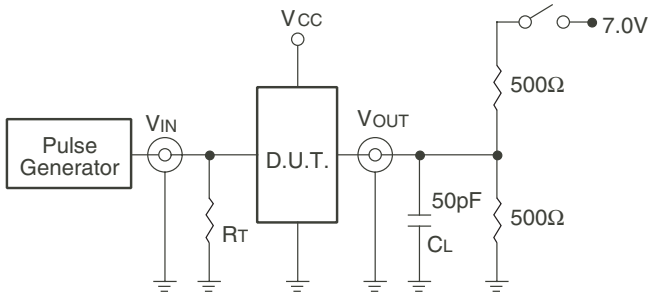
NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

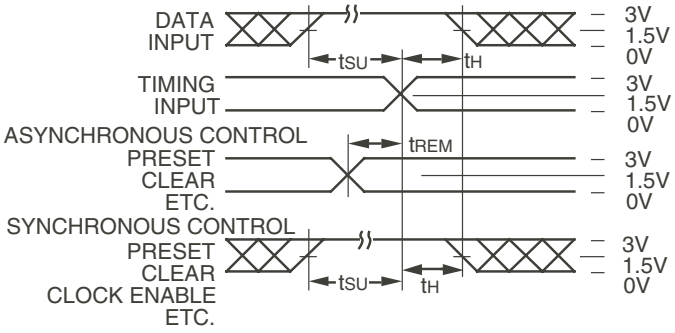
Symbol	Parameter	Condition[1]	FCT162823AT		FCT162823CT		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLKx to xOx	C_L = 50pF R_L = 500Ω	1.5	10	1.5	4.7	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	20	1.5	8	
t_{PHL}	Propagation Delay x$\overline{CLR}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	14	1.5	4.7	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xOx	C_L = 50pF R_L = 500Ω	1.5	12	1.5	4.4	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	23	1.5	9	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xOx	C_L = 50pF[4] R_L = 500Ω	1.5	7	1.5	3.6	ns
		C_L = 50pF R_L = 500Ω	1.5	8	1.5	3.6	
t_{SU}	Set-up Time HIGH or LOW xDx to xCLK	C_L = 50pF R_L = 500Ω	3	—	1.5	—	ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	0	—	ns
t_{SU}	Set-up Time HIGH or LOW, x$\overline{CLKEN}$ to xCLK		3	—	2.5	—	ns
t_H	Hold Time HIGH or LOW, x$\overline{CLKEN}$ to xCLK		0	—	0	—	ns
t_W	xCLK Pulse Width HIGH or LOW		6	—	3	—	ns
t_W	x$\overline{CLR}$ Pulse Width LOW		6	—	3	—	ns
t_{REM}	Recovery Time, x$\overline{CLR}$ to xCLK		6	—	3	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. This condition is guaranteed but not tested.

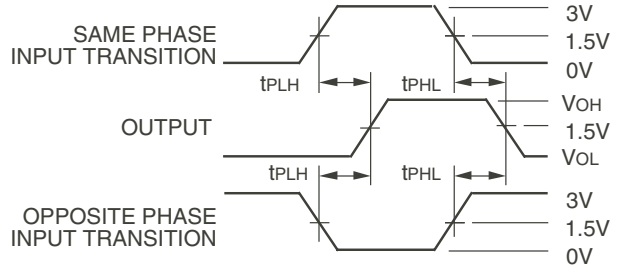
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

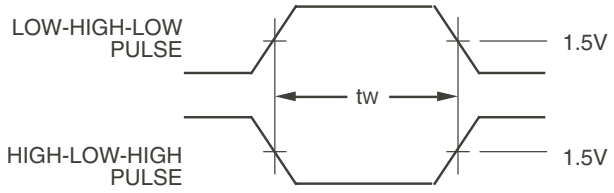
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

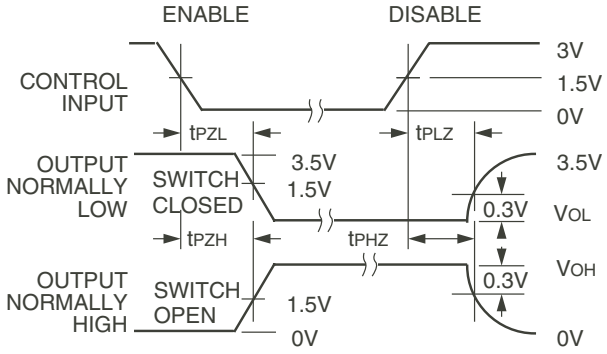
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

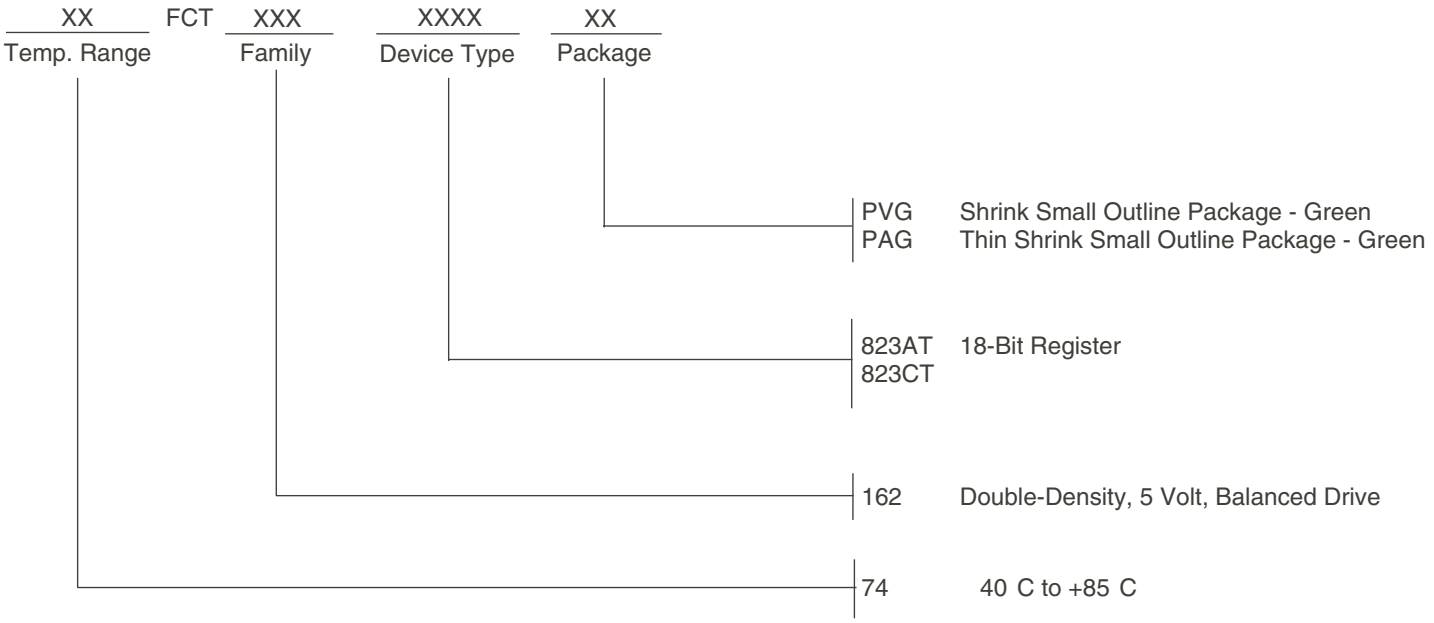


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



Datasheet Document History

09/06/09 Pg. 7 Updated the ordering information by removing the "IDT" notation and non RoHS part.

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