ADJD-S371-QR999

Miniature Surface-Mount
RGB Digital Color Sensor Module

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant

Description

ADJD-S371-QR999 is a cost effective, 4 channel digital output RGB+CLEAR sensor in miniature surface-mount package with a mere size of 3.9 x 4.5 x 1.8 mm. It is an IC module with combination of White LED and CMOS IC with integrated RGB filters + Clear channel and analog-to-digital converter front end.

It is ideal for applications like color detection, measurement, illumination sensing for display backlight adjustment such as colors, contrast and brightness enhancement in mobile devices which demand higher package integration, small footprint and low power consumption.

The 2-wire serial output allows direct interface to microcontroller or other logic control for further signal processing without additional component such as analog to digital converter. With the wide sensing range of 100 lux to 100,000 lux, the sensor can be used for many applications with different light levels by adjusting the gain setting. Additional features include a selectable sleep mode to minimize current consumption when the sensor is not in use.

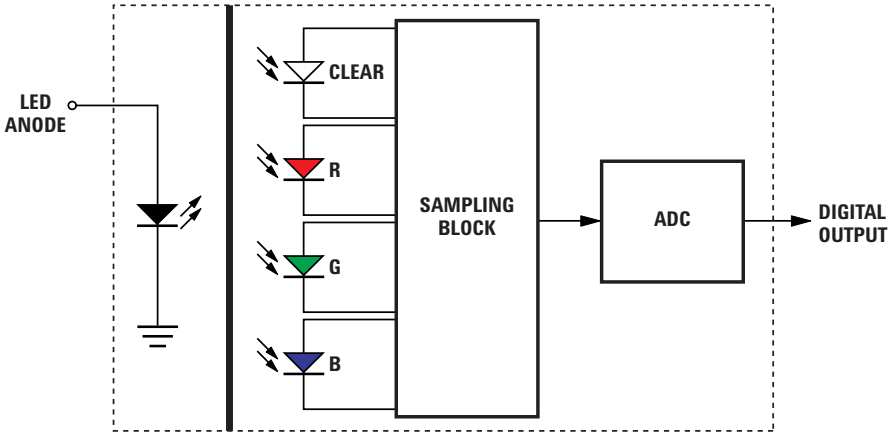
Features

- Four channel integrated light to digital converter (Red, Green, Blue and Clear).
- 10 bit digital output resolution
- Independent gain selection for each channel
- Wide sensitivity coverage: 0.1 klux - 100 klux
- Two wire serial communication
- Built in oscillator/selectable external clock
- Low power mode (sleep mode)
- Small 3.9 x 4.5 x 1.8 mm module
- Integrated solution with sensor, LED and separator in module for ease of design
- Lead free

Applications

- Mobile appliances
- Consumer appliances

Functional Block Diagram



Electrical Specifications

Absolute Maximum Ratings (Sensor) [1, 2]

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{STG_ABS}	-40	85	°C	
Digital Supply Voltage, D_{VDD} to D_{VSS}	V_{DDD_ABS}	2.5	3.6	V	
Analog Supply Voltage, A_{VDD} to A_{VSS}	V_{DDA_ABS}	2.5	3.6	V	
Input Voltage	V_{IN_ABS}	2.5	3.6	V	All I/O pins
Human Body Model ESD Rating	ESD_{HBM_ABS}		2	kV	All pins, human body model per JESD22-A114

Absolute Maximum Ratings at T_A = 25°C (LED)

Parameter	Symbol	Minimum	Maximum	Units
DC Forward Current	I_F		10	mA
Power Dissipation			39	mW
Reverse Voltage @ IR = 100 µA	V_R		5	V
Operating Temperature Range		-20	85	°C
Storage Temperature Range		-40	85	°C

Recommended Operating Conditions (Sensor)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Free Air Operating Temperature	T_A	0	25	70	°C
Digital Supply Voltage, D_{VDD} to D_{VSS}	V_{DDD}	2.5	2.6	3.6	V
Analog Supply Voltage, A_{VDD} to A_{VSS}	V_{DDA}	2.5	2.6	3.6	V
Output Current Load High	I_{OH}			3	mA
Output Current Load Low	I_{OL}			3	mA
Input Voltage High Level[4]	V_{IH}	0.7 V_{DDD}		V_{DDD}	V
Input Voltage Low Level[4]	V_{IL}	0		0.3 V_{DDD}	V

Electrical Characteristics at $T_A = 25°C$ (LED)

Parameter	Symbol	Minimum	Typical	Maximum	Units
DC Forward Voltage @ $I_F = 5$ mA	V_F		2.85	3.35	V
Reverse Breakdown Voltage @ $I_R = 100$ µA	V_R	5			V

DC Electrical Specifications (Sensor)
Over Recommended Operating Conditions (unless otherwise specified)

Parameter	Symbol	Conditions	Minimum	Typical[3]	Maximum	Units
Output Voltage High Level[5]	V_{OH}	$I_{OH} = 3$ mA		V_{DDD} - 0.4		V
Output Voltage Low Level[6]	V_{OL}	$I_{OH} = 3$ mA		0.2		V
Supply Current[7]	I_{DD_STATIC}	(Note 8)		3.8	5	mA
Sleep-Mode Supply Current[7]	I_{DD_SLP}	(Note 8)		2		µA
Input Leakage Current	I_{LEAK}		-10		10	µA

AC Electrical Specifications (Sensor)
Over Recommended Operating Conditions (unless otherwise specified)

Parameter	Symbol	Conditions	Minimum	Typical[3]	Maximum	Units
Internal Clock Frequency	$f_{_CLK_int}$			26		MHz
External Clock Frequency	$f_{_CLK_ext}$		16		40	MHz
2-Wire Interface Frequency	$f_{_2wire}$			100		kHz

Optical Specification (Sensor)

Parameter	Symbol	Conditions	Minimum	Typical[3]	Maximum	Units
Dark Offset	V_D	Ee = 0		20		LSB

Minimum Sensitivity [3]

Parameter	Symbol	Conditions		Minimum	Typical (Note 3)	Maximum	Units
Irradiance Responsivity	Re	λ_P = 460 nm Refer Note 9	B		152		LSB/(mW cm^{-2})
		λ_P = 542 nm Refer Note 10	G		178		
		λ_P = 645 nm Refer Note 11	R		254		
		λ_P = 645 nm Refer Note 11	Clear		264		

Maximum Sensitivity [3]

Parameter	Symbol	Conditions		Minimum	Typical (Note 3)	Maximum	Units
Irradiance Responsivity	Re	λ_P = 460 nm Refer Note 9	B		3796		LSB/(mW cm^{-2})
		λ_P = 542 nm Refer Note 10	G		4725		
		λ_P = 645 nm Refer Note 11	R		6288		
		λ_P = 645 nm Refer Note 11	Clear		6590		

Saturation Irradiance for Minimum Sensitivity [12]

Parameter	Symbol	Conditions		Minimum	Typical (Note 3)	Maximum	Units
Saturation Irradiance		λ_P = 460 nm Refer Note 9	B		6.73		mW/cm^2
		λ_P = 542 nm Refer Note 10	G		5.74		
		λ_P = 645 nm Refer Note 11	R		4.03		
		λ_P = 645 nm Refer Note 11	Clear		3.87		

Saturation Irradiance for Maximum Sensitivity [12]

Parameter	Symbol	Conditions		Minimum	Typical (Note 3)	Maximum	Units
Saturation Irradiance		λ_P = 460 nm Refer Note 9	B		0.27		mW/cm^2
		λ_P = 542 nm Refer Note 10	G		0.22		
		λ_P = 645 nm Refer Note 11	R		0.16		
		λ_P = 645 nm Refer Note 11	Clear		0.16		

Notes:
1. The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The device should not be operated at these limits. The parametric values defined in the "Electrical Specifications" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Specified at room temperature (25°C) and $V_{DDD} = V_{DDA} = 2.5$ V.
4. Applies to all DI pins.
5. Applies to all DO pins. SDASLV go tri-state when output logic high. Minimum V_{OH} depends on the pull-up resistor value.
6. Applies to all DO and DIO pins.
7. Refers to total device current consumption.
8. Output and bidirectional pins are not loaded.
9. Test condition is blue light of peak wavelength (λ_P) 460 nm and spectral half width ($\lambda^1/_2$) 25 nm.
10. Test condition is green light of peak wavelength (λ_P) 542 nm and spectral half width ($\lambda^1/_2$) 35 nm.
11. Test condition is red light of peak wavelength (λ_P) 645 nm and spectral half width ($\lambda^1/_2$) 20 nm.
12. Saturation irradiance = (MSB)/(Irradiance responsivity).

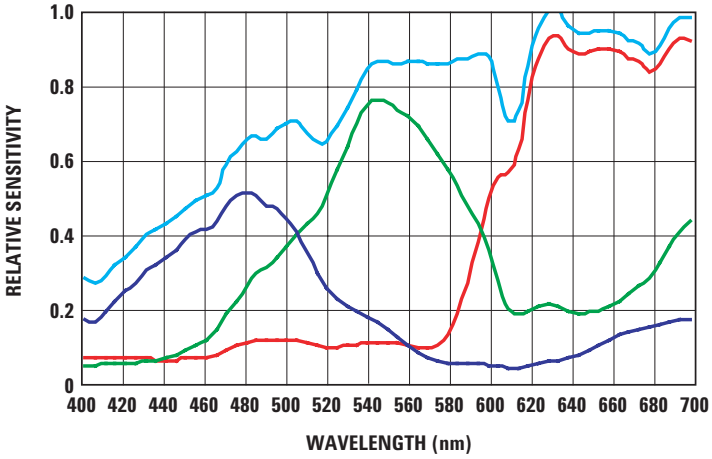


Figure 1. Typical spectral response when the gains for all the color channels are set at equal

Serial Interface Timing Information

Parameter	Symbol	Minimum	Maximum	Units
SCL Clock Frequency	f_{scl}	0	100	kHz
(Repeated) START Condition Hold Time	$t_{HD:STA}$	4	-	µs
Data Hold Time	$t_{HD:CAT}$	0	3.45	µs
SCL Clock Low Period	t_{LOW}	4.7	-	µs
SCL Clock High Period	t_{HIGH}	4.0	-	µs
Repeated START Condition Setup Time	$t_{SU:STA}$	4.7	-	µs
Data Setup Time	$t_{SU:DAT}$	250	-	µs
STOP Condition Setup Time	$t_{SU:STD}$	4.0	-	µs
Bus Free Time Between START and STOP Conditions	t_{BUF}	4.7	-	µs

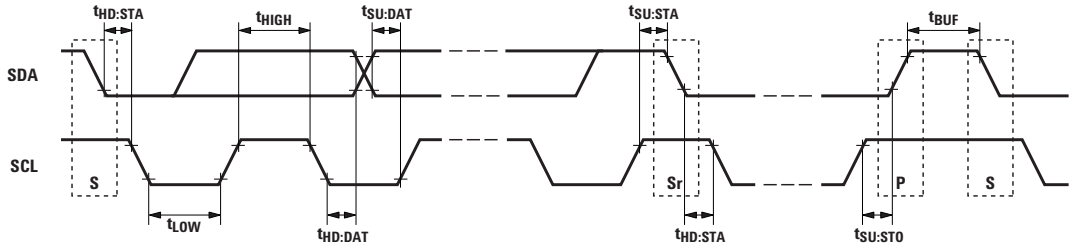


Figure 2. Serial interface bus timing waveforms

Serial Interface Reference

Description

The programming interface to the ADJD-S371-QR999 is a 2-wire serial bus. The bus consists of a serial clock (SCL) and a serial data (SDA) line. The SDA line is bi-directional on ADJD-S371-QR999 and must be connected through a pull-up resistor to the positive power supply. When the bus is free, both lines are HIGH.

The 2-wire serial bus on ADJD-S371-QR999 requires one device to act as a master while all other devices must be slaves. A master is a device that initiates a data transfer on the bus, generates the clock signal and terminates the data transfer while a device addressed by the master is called a slave. Slaves are identified by unique device addresses.

Both master and slave can act as a transmitter or a receiver but the master controls the direction for data transfer. A transmitter is a device that sends data to the bus and a receiver is a device that receives data from the bus.

The ADJD-S371-QR999 serial bus interface always operates as a slave transceiver with a data transfer rate of up to 100kbit/s.

START/STOP Condition

The master initiates and terminates all serial data transfers. To begin a serial data transfer, the master must send a unique signal to the bus called a START condition. This is defined as a HIGH to LOW transition on the SDA line while SCL is HIGH.

The master terminates the serial data transfer by sending another unique signal to the bus called a STOP condition. This is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH.

The bus is considered to be busy after a START (S) condition. It will be considered free a certain time after the STOP (P) condition. The bus stays busy if a repeated START (Sr) is sent instead of a STOP condition.

The START and repeated START conditions are functionally identical.

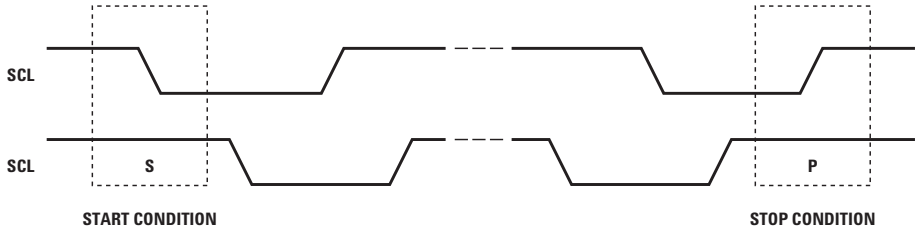


Figure 3. START/STOP condition

Data Transfer

The master initiates data transfer after a START condition. Data is transferred in bits with the master generating one clock pulse for each bit sent. For a data bit to be valid, the SDA data line must be stable during the HIGH period of the SCL clock line. Only during the LOW period of the SCL clock line can the SDA data line change state to either HIGH or LOW.

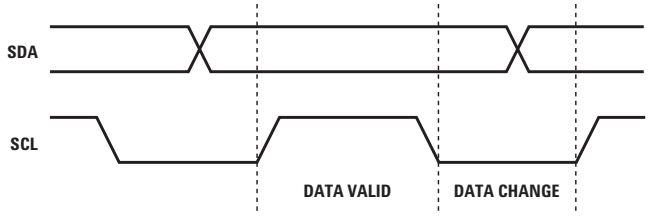


Figure 4. Data bit transfer

The SCL clock line synchronizes the serial data transmission on the SDA data line. It is always generated by the master. The frequency of the SCL clock line may vary throughout the transmission as long as it still meets the minimum timing requirements.

The master by default drives the SDA data line. The slave drives the SDA data line only when sending an acknowledge bit after the master writes data to the slave or when the master requests the slave to send data.

The SDA data line driven by the master may be implemented on the negative edge of the SCL clock line. The master may sample data driven by the slave on the positive edge of the SCL clock line. Figure shows an example of a master implementation and how the SCL clock line and SDA data line can be synchronized.

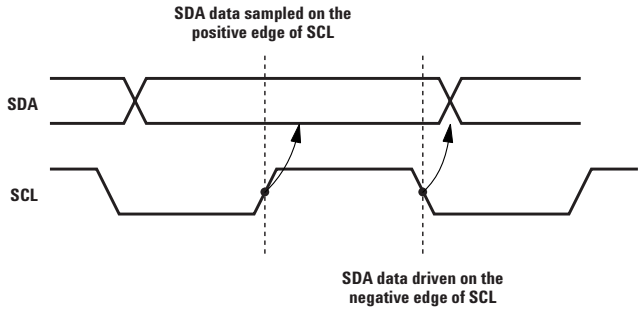


Figure 5. Data bit synchronization

A complete data transfer is 8-bits long or 1-byte. Each byte is sent most significant bit (MSB) first followed by an acknowledge or not acknowledge bit. Each data transfer can send an unlimited number of bytes (depending on the data format).

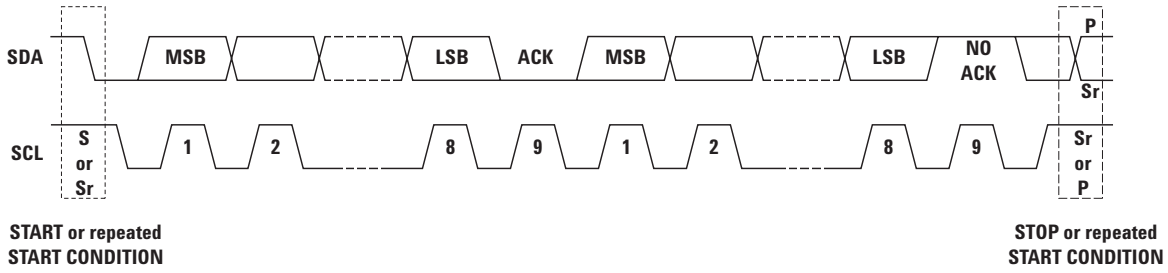


Figure 6. Data byte transfer

Acknowledge/Not Acknowledge

The receiver must always acknowledge each byte sent in a data transfer. In the case of the slave-receiver and master-transmitter, if the slave-receiver does not send an acknowledge bit, the master-transmitter can either STOP the transfer or generate a repeated START to start a new transfer.

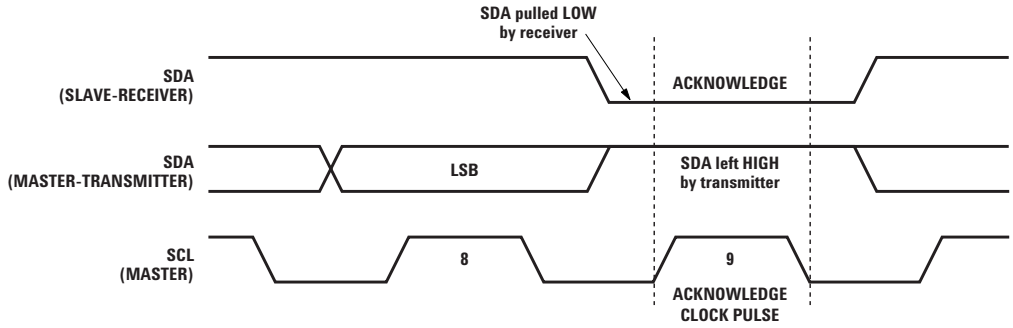


Figure 7. Slave-receiver acknowledge

In the case of the master-receiver and slave-transmitter, the master generates a not acknowledge to signal the end of the data transfer to the slave-transmitter. The master can then send a STOP or repeated START condition to begin a new data transfer.

In all cases, the master generates the acknowledge or not acknowledge SCL clock pulse.

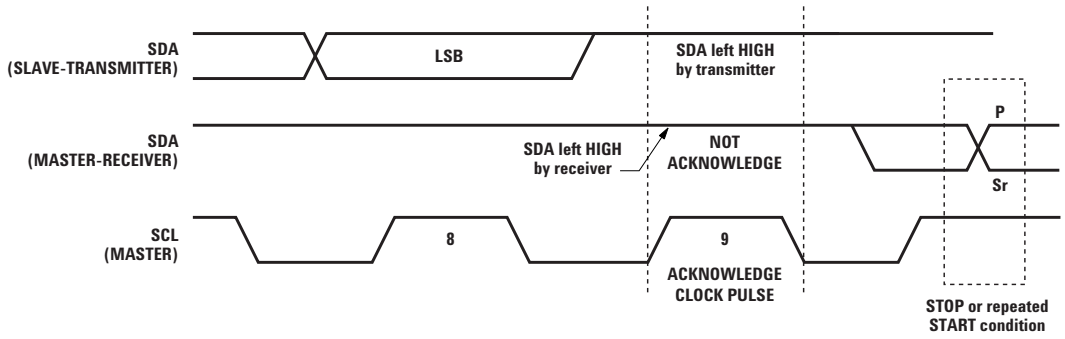


Figure 8. Master-receiver acknowledge

Addressing

Each slave device on the serial bus needs to have a unique address. This is the first byte that is sent by the master-transmitter after the START condition. The address is defined as the first seven bits of the first byte.

The eighth bit or least significant bit (LSB) determines the direction of data transfer. A 'one' in the LSB of the first byte indicates that the master will read data from the addressed slave (master-receiver and slave-transmitter). A 'zero' in this position indicates that the master will write data to the addressed slave (master-transmitter and slave-receiver).

A device whose address matches the address sent by the master will respond with an acknowledge for the first byte and set itself up as a slave-transmitter or slave-receiver depending on the LSB of the first byte.

The slave address on ADJD-S371-QR999 is 0x74 (7-bits).

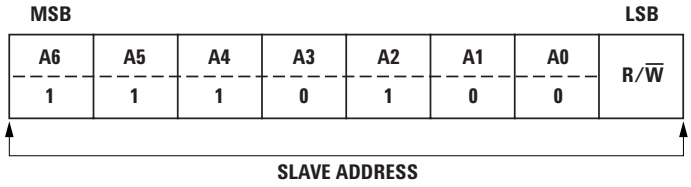


Figure 9. Slave addressing

Data Format

ADJD-S371-QR999 uses a register-based programming architecture. Each register has a unique address and controls a specific function inside the chip.

To write to a register, the master first generates a START condition. Then it sends the slave address for the device it wants to communicate with. The least significant bit (LSB) of the slave address must indicate that the master wants to write to the slave. The addressed device will then acknowledge the master.

The master writes the register address it wants to access and waits for the slave to acknowledge. The master then writes the new register data. Once the slave acknowledges, the master generates a STOP condition to end the data transfer.

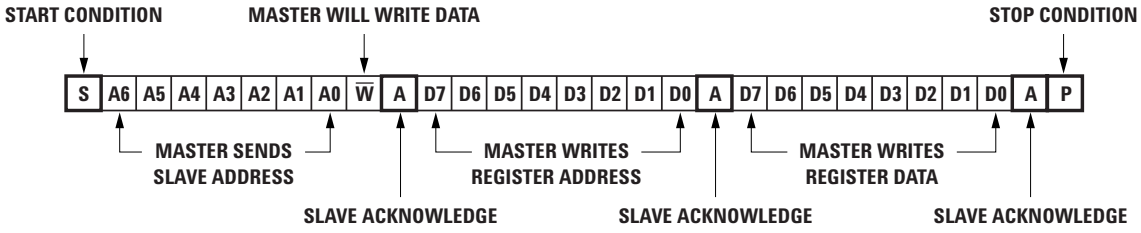


Figure 10. Register byte write protocol

To read from a register, the master first generates a START condition. Then it sends the slave address for the device it wants to communicate with. The least significant bit (LSB) of the slave address must indicate that the master wants to write to the slave. The addressed device will then acknowledge the master.

The master writes the register address it wants to access and waits for the slave to acknowledge. The master then generates a repeated START condition and resends the slave address sent previously. The least significant bit (LSB) of the slave address must indicate that the master wants to read from the slave. The addressed device will then acknowledge the master.

The master reads the register data sent by the slave and sends a no acknowledge signal to stop reading. The master then generates a STOP condition to end the data transfer.

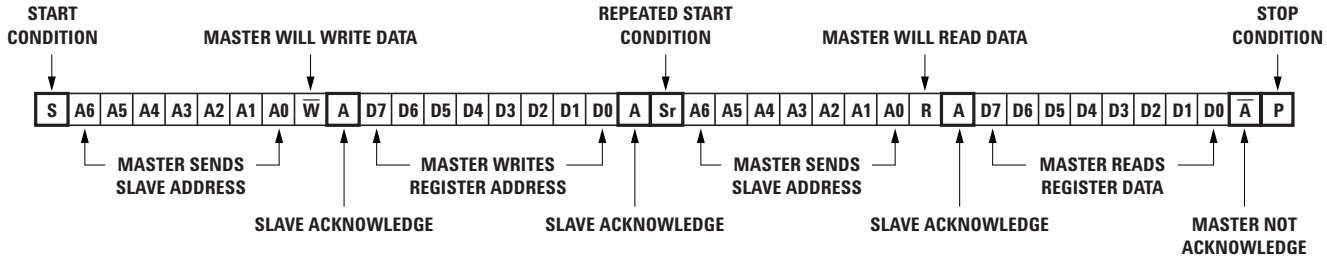
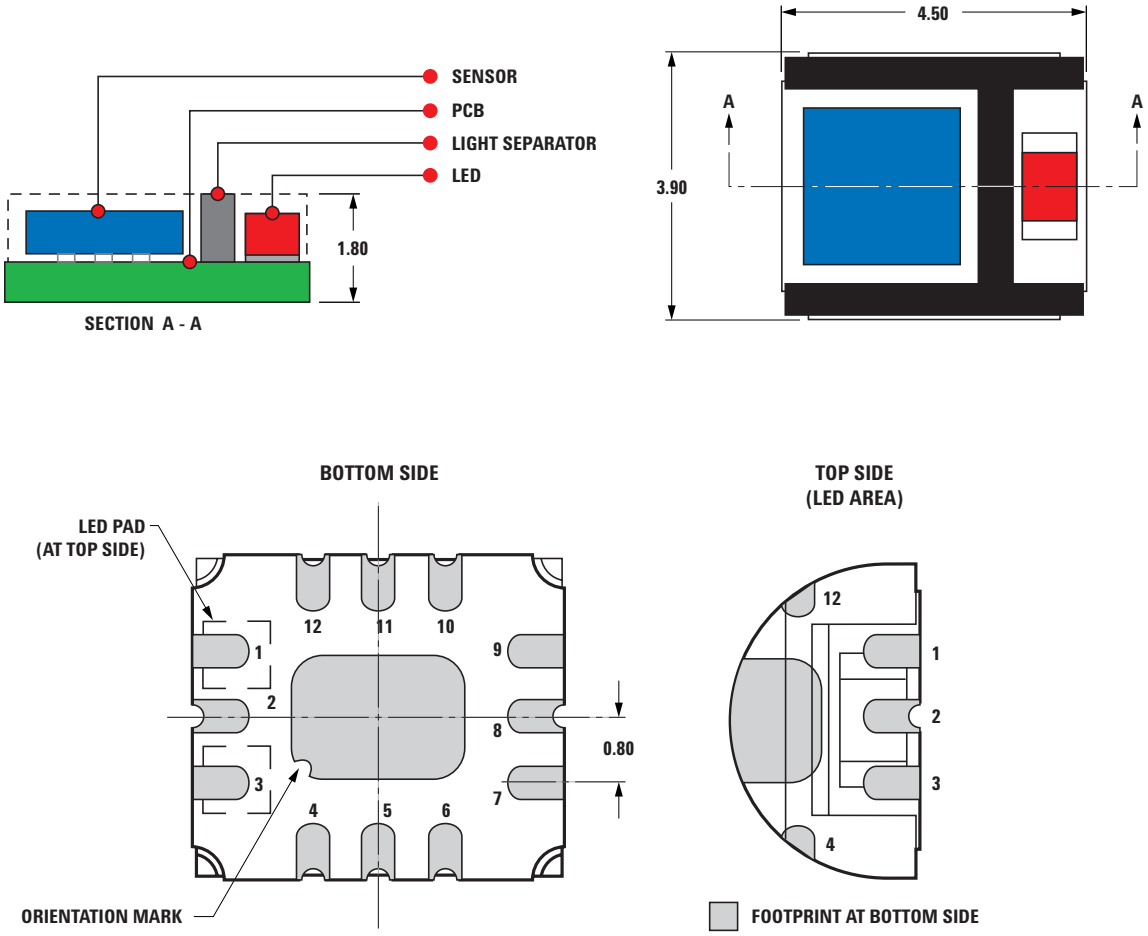


Figure 11. Register byte read protocol

Mechanical Drawing



Pin	Name	Description
1	LED -VE	LED cathode
2	NC	No connection
3	LED +VE	LED anode
4	SDA	Bidirectional data pin. A pull-up resistor should be tied to SDA because it goes tri-state to output logic 1
5	DVDD	Digital power pin
6	SCL	Serial interface clock
7	AVDD	Analog power pin
8	SLEEP	Sleep pin. When SLEEP = 1, the device goes into sleep mode. In sleep mode, all analog circuits are powered down and the clock signal is gated away from the core logic resulting in very low current consumption.
9	AGND	Analog ground pin
10	XRST	Reset pin. Global, asynchronous, active-low system reset. When asserted low, XRST resets all registers. Minimum reset pulse low is 1us and must be provided by external circuitry.
11	DGND	Digital ground pin
12	XCLK	External clock input

Description	Nominal	Tolerances
Body size (W, mm)	3.90	+0.6
Body size (L, mm)	4.50	±0.2
Overall thickness (t, mm)	1.80	±0.2
Terminal pitch (mm)	0.8	±0.08

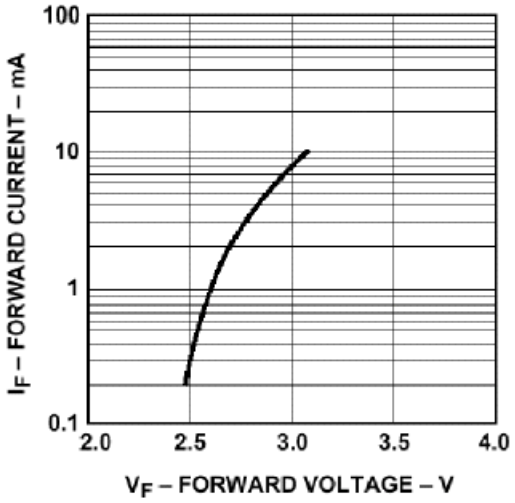


Figure 12: Forward current vs forward voltage (LED)

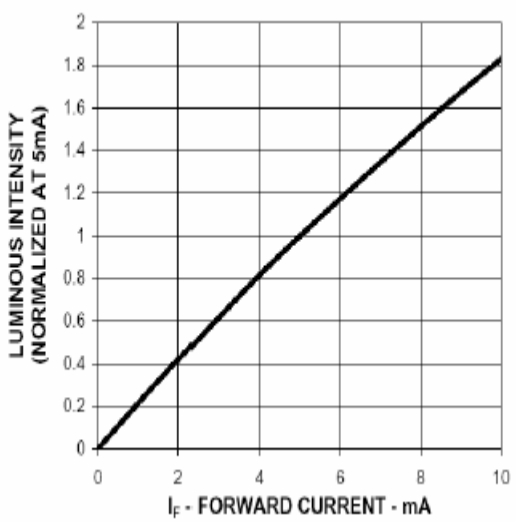
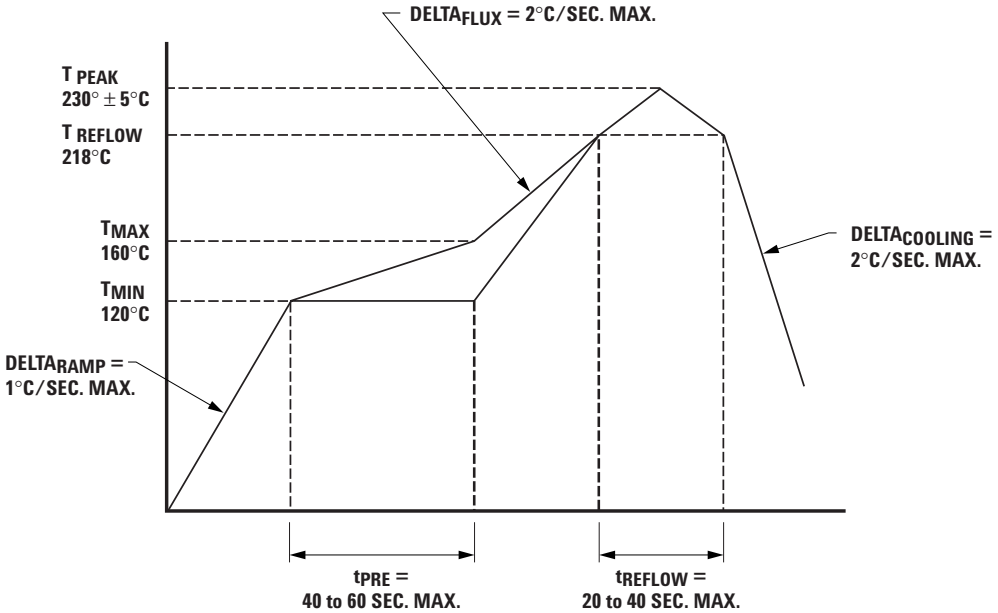


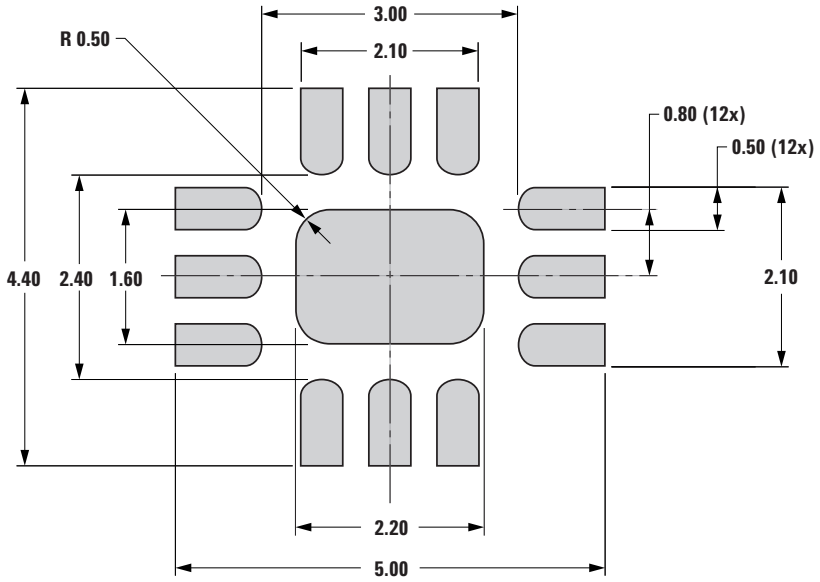
Figure 13: Luminous intensity vs forward current (LED)

Reflow Profile

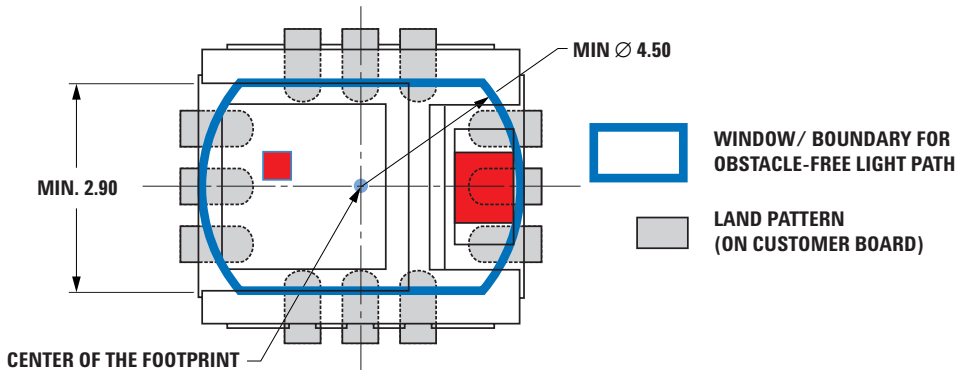
It is recommended that Henkel Pb-free solder paste LF310 be used for soldering ADJD-S371-QR999. Below is the recommended reflow profile.



Recommended Land Pattern (on customer board)



Recommended Aperture Dimensions with Respect to Mounting Axis on Customer Board



Recommendations for Handling and Storage of ADJD-S371-QR999

This product is qualified as Moisture Sensitive Level 3 per Jedec J-STD-020. Precautions when handling this moisture sensitive product is important to ensure the reliability of the product. Do refer to Avago Application Note AN5305 Handling Of Moisture Sensitive Surface Mount Devices for details.

A. Storage before use

- Unopened moisture barrier bag (MBB) can be stored at 30°C and 90% RH or less for maximum 1 year.
- It is not recommended to open the MBB prior to assembly (e.g., for IQC).
- It should also be sealed with a moisture absorbent material (Silica Gel) and an indicator card (cobalt chloride) to indicate the moisture within the bag.

B. Control after opening the MBB

- The humidity indicator card (HIC) shall be read immediately upon opening of MBB.
- The components must be kept at <30°C/60% RH at all time and all high temperature related process including soldering, curing or rework need to be completed within 168 hrs.

C. Control for unfinished reel

- For any unused components, they need to be stored in sealed MBB with desiccant or desiccator at <5% RH.

D. Control of assembled boards

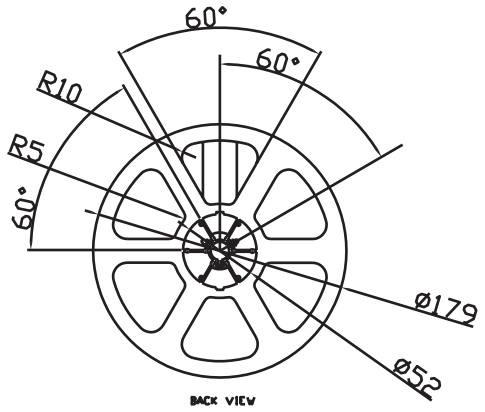
- If the PCB soldered with the components is to be subjected to other high temperature processes, the PCB need to be stored in sealed MBB with desiccant or desiccator at <5% RH to ensure no components have exceeded their floor life of 168 hrs.

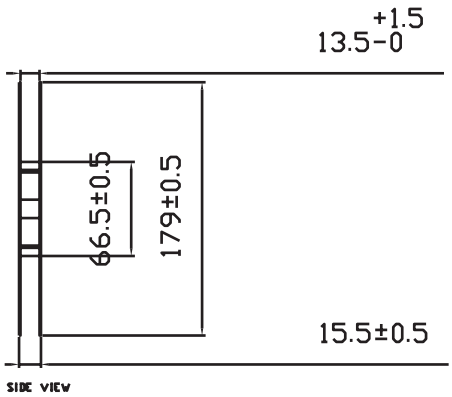
E. Baking is required if:

- "10%" or "15%" HIC indicator turns pink.
- The components are exposed to condition of >30°C/60% RH at any time.
- The components floor life exceeded 168 hrs.
- Recommended baking condition (in component form): 125°C for 24 hrs.

Package Tape and Reel Dimensions

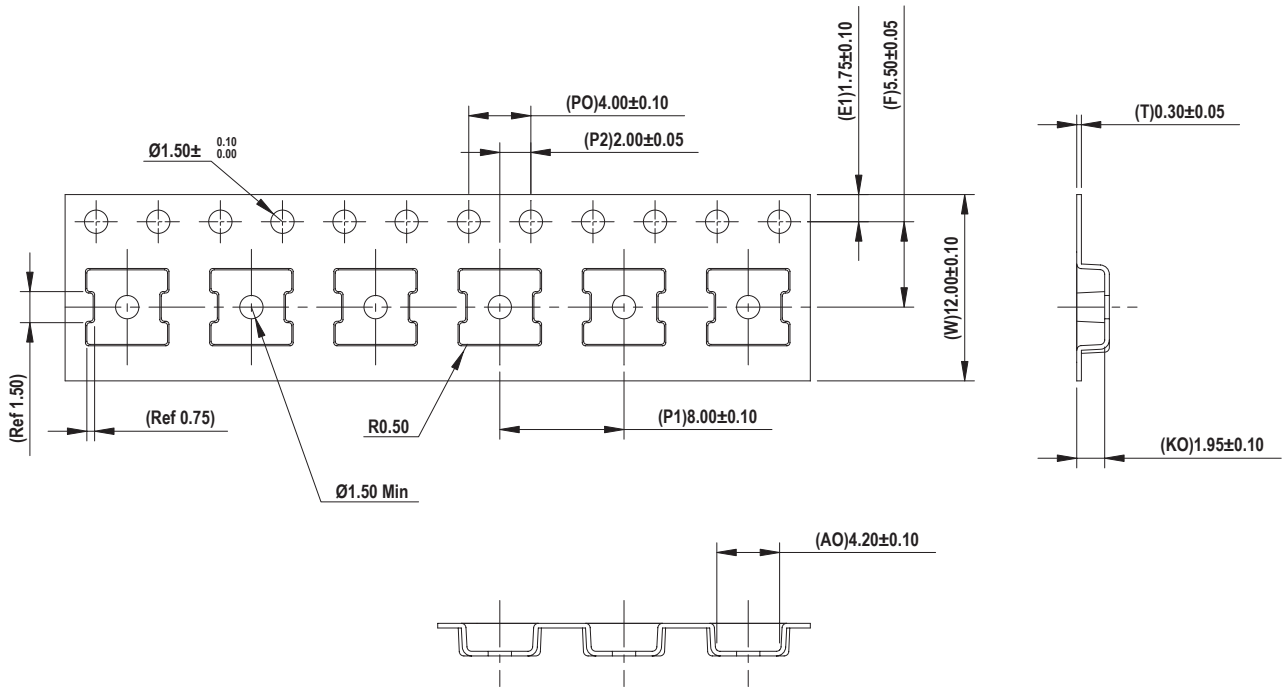
Reel Dimensions





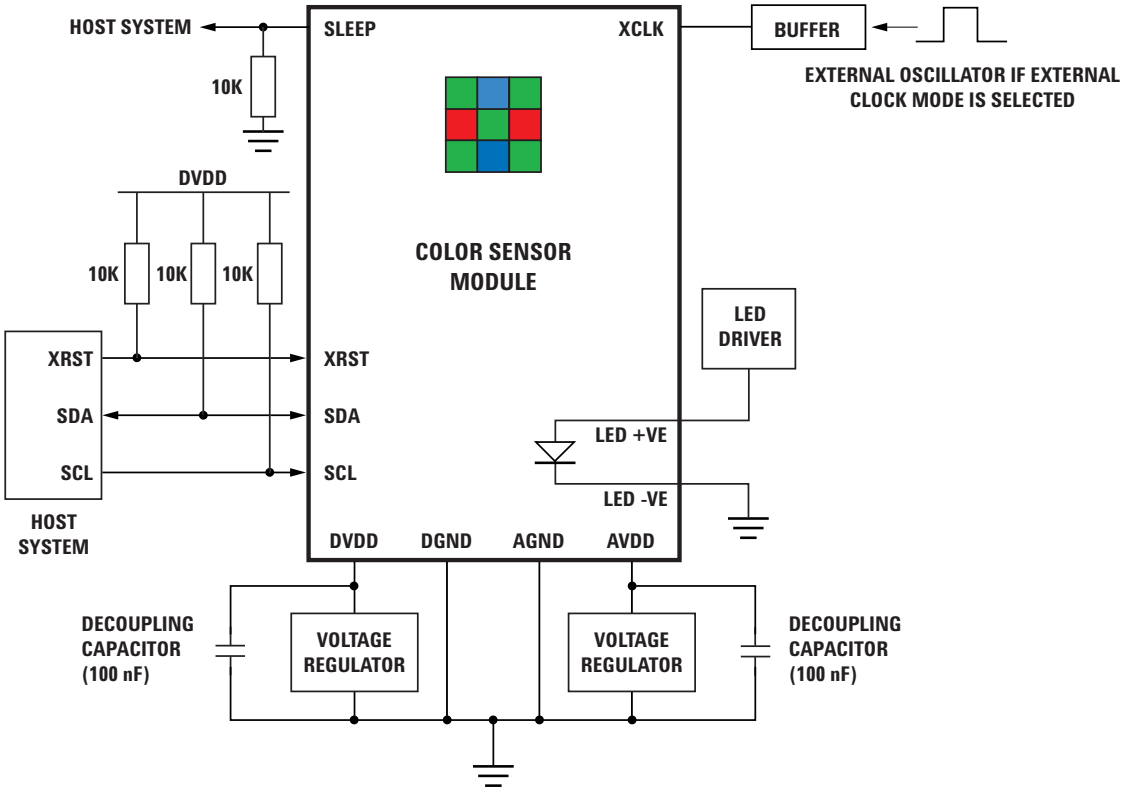
Note:
1. Dimensions are in milimeters (mm)

Carrier Tape Dimensions



Notes:
1. AO measured at 0.3mm above base of pocket
2. 10 pitches cumulative tolerance is ±0.2mm
3. Dimensions are in millimeters (mm)

Appendix A: Typical Application Diagram



Note:

1 It is recommended to drive the LED with DC current at I_F = 5mA

Appendix B: Sensor Register List

	ADD (DEC)	ADD (HEX)	MNEMONIC	WIDTH	RESET (DEC)	TYPE	ACCESS	B7	B6	B5	B4	B3	B2	B1	B0	NOTES
FN	0	0	CTRL	2	0	BITS	R/W	N/A						GOF5	GS5R	
	1	1	CONFIG	3	0	BITS	R/W	N/A					EXTCLK	SLEEP	TOF5	
SENSOR	6	6	CAP_RED	4	15	NUMBER	R/W	N/A					CAP_RED[3:0]			
	7	7	CAP_GREEN	4	15	NUMBER	R/W	N/A					CAP_GREEN[3:0]			
	8	8	CAP_BLUE	4	15	NUMBER	R/W	N/A					CAP_BLUE[3:0]			
	9	9	CAP_CLEAR	4	15	NUMBER	R/W	N/A					CAP_CLEAR[3:0]			
	10	A	INT_RED_LO	8	0	NUMBER	R/W	INT_RED[7:0]								
	11	B	INT_RED_HI	8	0	NUMBER	R/W	INT_RED[11:8]								
	12	C	INT_GREEN_LO	8	0	NUMBER	R/W	INT_GREEN[7:0]								
	13	D	INT_GREEN_HI	8	0	NUMBER	R/W	INT_GREEN[11:8]								
	14	E	INT_BLUE_LO	8	0	NUMBER	R/W	INT_BLUE[7:0]								
	15	F	INT_BLUE_HI	8	0	NUMBER	R/W	INT_BLUE[11:8]								
	16	10	INT_CLEAR_LO	8	0	NUMBER	R/W	INT_CLEAR[7:0]								
	17	11	INT_CLEAR_HI	8	0	NUMBER	R/W	INT_CLEAR[11:8]								
SAMPLE DATA	64	40	DATA_RED_LO	8	0	NUMBER	R	DATA_RED[7:0]								11/10-bit data
	65	41	DATA_RED_HI	3	0	NUMBER	R	N/A					DATA_RED[9:8]			
	66	42	DATA_GREEN_LO	8	0	NUMBER	R	DATA_GREEN[7:0]								
	67	43	DATA_GREEN_HI	3	0	NUMBER	R	N/A					DATA_GREEN[9:8]			
	68	44	DATA_BLUE_LO	8	0	NUMBER	R	DATA_BLUE[7:0]								
	69	45	DATA_BLUE_HI	3	0	NUMBER	R	N/A					DATA_BLUE[9:8]			
	70	46	DATA_CLEAR_LO	8	0	NUMBER	R	DATA_CLEAR[7:0]								
	71	47	DATA_CLEAR_HI	3	0	NUMBER	R	N/A					DATA_CLEAR[9:8]			
OFFSET DATA	72	48	OFFSET_RED	6	0	NUMBER	R	SIGN_RED	OFFSET_RED[6:0]							sign = 1 is -ve
	73	49	OFFSET_GREEN	8	0	NUMBER	R	SIGN_GREEN	OFFSET_GREEN[6:0]							
	74	4A	OFFSET_BLUE	8	0	NUMBER	R	SIGN_BLUE	OFFSET_BLUE[6:0]							
	75	4B	OFFSET_CLEAR	8	0	NUMBER	R	SIGN_CLEAR	OFFSET_CLEAR[6:0]							

1) CTRL: Control Register

B7	B6	B5	B4	B3	B2	B1	B0
N/A						GOFS	GSSR

N/A	Not available.
GSSR	Get sensor reading. Active high and automatically cleared. Result is stored in registers 64-71 (DEC).
GOFS	Get offset reading. Active high and automatically cleared. Result is stored in registers 72-75 (DEC).

2) CONFIG: Configuration Register

B7	B6	B5	B4	B3	B2	B1	B0
N/A					EXTCKL	SLEEP	TOFS

N/A	Not available.
EXTCLK	External clock mode. Active high.
SLEEP	Sleep mode. Active high and external clock mode only. Automatically cleared if otherwise.
TOFS	Trim offset mode. Active high.

3) CAP_RED: Capacitor Settings Register for Red Channel

B7	B6	B5	B4	B3	B2	B1	B0
N/A				CAP_RED[3:0]			

N/A	Not available.
CAP_RED	Number of red channel capacitors.

4) CAP_GREEN: Capacitor Settings Register for Green Channel

B7	B6	B5	B4	B3	B2	B1	B0
N/A				CAP_GREEN[3:0]			

N/A	Not available.
CAP_GREEN	Number of green channel capacitors.

5) CAP_BLUE: Capacitor Settings Register for Blue Channel

B7	B6	B5	B4	B3	B2	B1	B0
N/A				CAP_BLUE[3.0]			

N/A	Not available.
CAP_BLUE	Number of blue channel capacitors.

6) CAP_CLEAR: Capacitor Settings Register for Clear Channel

B7	B6	B5	B4	B3	B2	B1	B0
N/A				CAP_CLEAR[3:0]			

N/A	Not available.
CAP_CLEAR	Number of clear channel capacitors.

7) INT_RED: Integration Time Slot Setting Register for Red Channel

B7	B6	B5	B4	B3	B2	B1	B0
CAP_RED[7:0]							

B7	B6	B5	B4	B3	B2	B1	B0
N/A				INT_RED[11:8]			

INT_RED	Number of red channel integration time slots.

8) INT_GREEN: Integration Time Slot Setting Register for Green Channel

B7	B6	B5	B4	B3	B2	B1	B0
INT_GREEN[7:0]							

B7	B6	B5	B4	B3	B2	B1	B0
N/A				INT_GREEN[11:8]			

INT_GREEN	Number of green channel integration time slots.

9) INT_BLUE: Integration Time Slot Setting Register for Blue Channel

B7	B6	B5	B4	B3	B2	B1	B0
INT_BLUE[7:0]							

B7	B6	B5	B4	B3	B2	B1	B0
N/A				INT_BLUE[11:8]			

INT_BLUE	Number of blue channel integration time slots.

10) INT_CLEAR: Integration Time Slot Setting Register for Clear Channel

B7	B6	B5	B4	B3	B2	B1	B0
INT_CLEAR[7:0]							

B7	B6	B5	B4	B3	B2	B1	B0
N/A				INT_CLEAR[11:8]			

INT_CLEAR	Number of clear channel integration time slots.

11) DATA_RED_LO: Low Byte Register of Red Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
DATA_RED[7:0]							

DATA_RED	Red channel ADC data.

12) DATA_RED_HI: High Byte Register of Red Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
N/A						DATA_RED[9:8]	

N/A	Not available.
DATA_RED	Red channel ADC data.

13) DATA_GREEN_LO: Low Byte Register of Green Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
DATA_GREEN[7:0]							

DATA_GREEN	Green channel ADC data.

14) DATA_GREEN_HI: High Byte Register of Green Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
N/A						DATA_GREEN[9:8]	

N/A	Not available.
DATA_GREEN	Green channel ADC data.

15) DATA_BLUE_LO: Low Byte Register of Blue Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
DATA_BLUE[7:0]							

DATA_BLUE	Blue channel ADC data.

16) DATA_BLUE_HI: High Byte Register of Blue Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
N/A						DATA_BLUE[9:8]	

N/A	Not available.
DATA_BLUE	Blue channel ADC data.

17) DATA_CLEAR_LO: Low Byte Register of Clear Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
DATA_CLEAR[7:0]							

DATA_CLEAR	Clear channel ADC data.

18) DATA_CLEAR_HI: High Byte Register of Clear Channel Sensor ADC Reading

B7	B6	B5	B4	B3	B2	B1	B0
N/A						DATA_CLEAR[9:8]	

N/A	Not available.
DATA_CLEAR	Clear channel ADC data.

19) OFFSET_RED: Offset Data Register for Red Channel

B7	B6	B5	B4	B3	B2	B1	B0
SIGN_RED	OFFSET_RED[6:0]						

SIGN_RED	Sign bit. 0 = POSITIVE, 1 = NEGATIVE.
OFFSET_RED	Red channel ADC offset data.

20) OFFSET_GREEN: Offset Data Register for Green Channel

B7	B6	B5	B4	B3	B2	B1	B0
SIGN_GREEN	OFFSET_GREEN[6:0]						

SIGN_GREEN	Sign bit. 0 = POSITIVE, 1 = NEGATIVE.
OFFSET_GREEN	Green channel ADC offset data.

21) OFFSET_BLUE: Offset Data Register for Blue Channel

B7	B6	B5	B4	B3	B2	B1	B0
SIGN_BLUE	OFFSET_BLUE[6:0]						

SIGN_BLUE	Sign bit. 0 = POSITIVE, 1 = NEGATIVE.
OFFSET_BLUE	Blue channel ADC offset data.

22) OFFSET_CLEAR: Offset Data Register for Clear Channel

B7	B6	B5	B4	B3	B2	B1	B0
SIGN_CLEAR	OFFSET_CLEAR[6:0]						

SIGN_CLEAR	Sign bit. 0 = POSITIVE, 1 = NEGATIVE.
OFFSET_CLEAR	Clear channel ADC offset data.

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AV02-0314EN - July 24, 2007