3-WIRE SERIAL INTERFACE REAL-TIME CLOCK ICs WITH VOLTAGE MONITORING FUNCTION

R×5C338A

NO. EA-053-170413

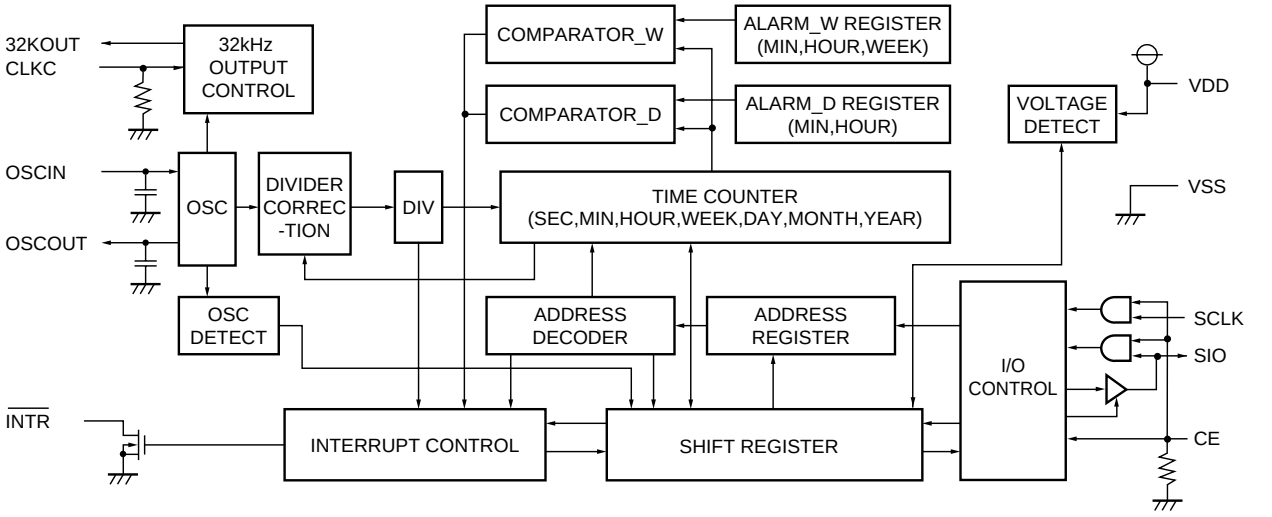
OUTLINE

The R×5C338A are CMOS real-time clock ICs connected to the CPU by three signal lines CE (Chip Enable), SCLK (Serial Clock), and SIO (Serial Input/Output), and configured to perform serial transmission of time and calendar data to the CPU. These models incorporate different functional circuits. The periodic interrupt circuit is configured to generate interrupt signals with six selectable interrupts ranging from 0.5 seconds to 1 month. The 2 alarm circuits generate interrupt signals at preset times. The oscillation circuit is driven under constant voltage so that fluctuations in oscillation frequency due to voltage are small and supply current is also small (TYP. 0.35µA at 3 volts). The oscillation halt sensing circuit can be used to judge the validity of internal data in such events as power-on. The supply voltage monitoring circuit is configured to record a drop in supply voltage below two selectable supply voltage monitoring threshold settings. The 32-kHz clock output function is intended to output sub-clock pulses for the external microcomputer. The oscillation adjustment circuit is intended to adjust time counts with high precision by correcting deviations in the oscillation frequency of the crystal oscillator. These models come in an ultra-compact 10-pin SSOP (RS5C338A with a height of 1.25mm and a pin pitch of 0.5mm)and 10-pin SSOP-G (RV5C338A with a height of 1.2mm and a pin pitch of 0.5mm).

FEATURES

- Timekeeping supply voltage ranging from 1.45 to 5.5 volts
- Low supply current: TYP. 0.35µA (MAX. 0.8µA) at 3 volts (at 25˚C)
- Only three signal lines (SCLK, SIO, and CE) required for connection to the CPU.
  Maximum clock frequency of 2 MHz (with V_{DD} of 5 volts)
- Time counters (counting hours, minutes, and seconds) and calendar counters (counting years, months, days, and weeks) (in BCD format)
- 1900/2000 identification bit for Year 2000 compliance
- Interrupt circuit configured to generate interrupt signals (with interrupts ranging from 0.5 seconds to 1 month) to the CPU and provided with an interrupt flag and an interrupt halt circuit
- 2 alarm circuits (Alarm_W for week , hour , and minute alarm settings and Alarm_D for hour and minute alarm settings)
- 32-kHz clock circuit (CMOS output, equipped with a control pin)
- Oscillation halt sensing circuit which can be used to judge the validity of internal data
- Supply voltage monitoring circuit with two supply voltage monitoring threshold settings
- Automatic identification of leap years up to the year 2099
- Selectable 12-hour and 24-hour mode settings
- Built-in oscillation stabilization capacitors (C_G and C_D)
- High precision oscillation adjustment circuit
- CMOS process
- Ultra-compact 10-pin SSOP (RS5C338A with a height of 1.25mm and size of 6.4×3.5mm)
  Ultra-compact 10-pin SSOP-G (RV5C338A with a height of 1.20mm and size of 4.0×2.9mm)

BLOCK DIAGRAM



SELECTION GUIDE

Part Number is designated as follows:

R V 5C338A - E2 - F ←Part Number
↑ ↑ ↑
R a 5C338A - bb – c

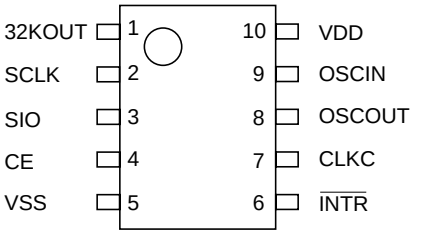
Code	Description
a	Designation of the package. S: SSOP10 V: SSOP10G
bb	Designation of the taping type. Only E2 is available.
c	Designation of the lead plating.

APPLICATIONS

- Communication devices (multi function phone, portable phone, PHS or pager)
- OA devices (fax, portable fax)
- Computer (desk-top and mobile PC, portable word-processor, PDA, electric note or video game)
- AV components (portable audio unit, video camera,camera, digital camera or remote controller)
- Home appliances (rice cooker, electric oven)
- Other (car navigation system, multi-function watch)

PIN CONFIGURATION

• 10-pin SSOP-G, 10-pin SSOP



PIN DESCRIPTIONS

Pin No.	Symbol	Name	Description
4	CE	Chip Enable Input	The CE pin is used for interfacing with the CPU. Should be held high to allow access to the CPU. Incorporates a pull-down resistor. Should be held low or open when the CPU is powered off. Allows a maximum input voltage of 5.5 volts regardless of supply voltage.
2	SCLK	Serial Clock Input	The SCLK pin is used to input clock pulses synchronizing the input and output of data to and from the SIO pin. Allows a maximum input voltage of 5.5 volts regardless of supply voltage.
3	SIO	Serial Input/Output	The SIO pin is used to input and output data intended for writing and reading in synchronization with the SCLK pin. CMOS input/output.
6	$\overline{\text{INTR}}$	Interrupt Output	The $\overline{\text{INTR}}$ pin is used to output periodic interrupt signals to the CPU and alarm interrupt signals (Alarm_W, Alarm_D). Disabled at power-on from 0 volts. Nch. open drain output.
1	32KOUT	32-kHz Clock Output	The 32KOUT pin is used to output 32.768-kHz clock pulses. Enabled at power-on from 0 volts. CMOS output. This pin is disabled if the CLKC pin is set to low or open.
7	CLKC	Clock Control Input	The CLCK pin is used to control output of the 32KOUT pin. The clock output is disabled and held low when the pin is set to low or open. Incorporates a pull-down resistor.
9 8	OSCIN OSCOUT	Oscillation Circuit Input/Output	The OSCIN and OSCOUT pins are used to connect the 32.768-kHz crystal oscillator (with all other oscillation circuit components built into the R×5C338A.)
10 5	VDD VSS	Positive Power Supply Input Negative Power Supply Input	The VDD pin is connected to the power supply. The VSS pin is grounded.

ABSOLUTE MAXIMUM RATINGS

(Vss=0V)

Symbol	Item	Conditions	Ratings	Unit
V_{DD}	Supply Voltage		–0.3 to +6.5	V
V_I	Input Voltage 1	SIO	–0.3 to V_{DD}+0.3	V
	Input Voltage 2	SCLK, CE,CLKC	–0.3 to +6.5	
V_O	Output Voltage 1	SIO, 32KOUT	–0.3 to V_{DD}+0.3	V
	Output Voltage 2	$\overline{INTR}$	–0.3 to +6.5	
P_D	Power Dissipation	Topt=25˚C	300	mW
Topt	Operating Temperature		–40 to +85	˚C
Tstg	Storage Temperature		–55 to +125	˚C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITIONS

(Vss=0V,Topt=–40 to +85˚C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD}	Supply Voltage		2.0		5.5	V
V_{CLK}	Timekeeping Voltage		1.45		5.5	V
f_{XT}	Oscillation Frequency			32.768		kHz
V_{PUP}	Pull-up Voltage	$\overline{INTR}$			5.5	V

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified : Vss=0V, V_{DD}=3V, Topt=–40 to +85°C

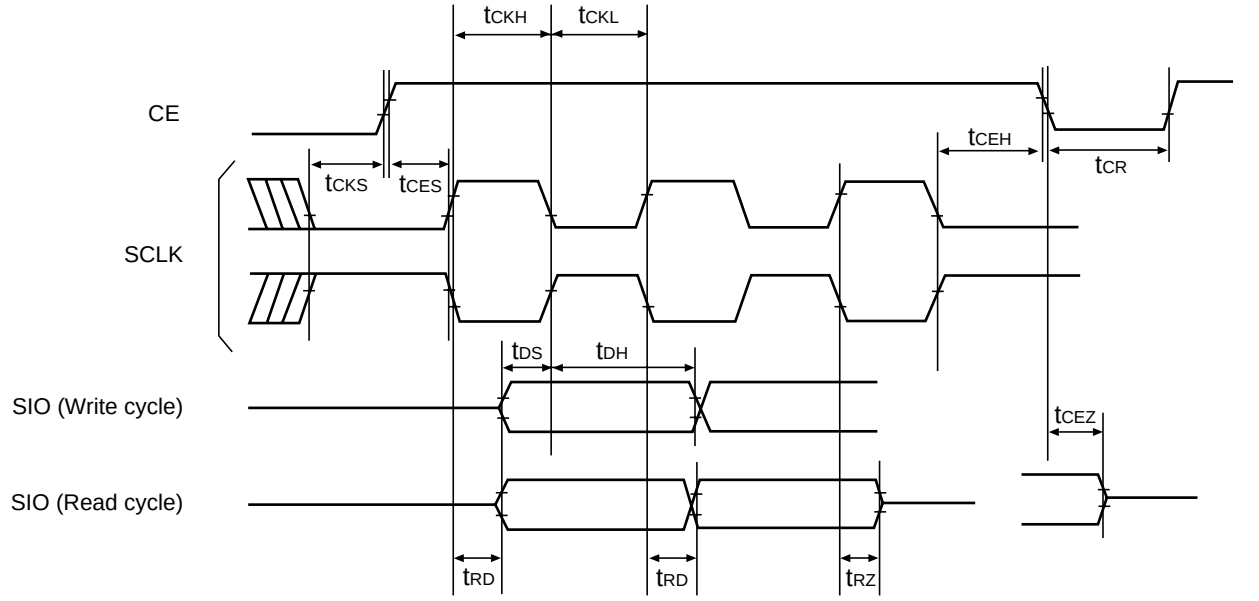
Symbol	Item	Pin name	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH1}	"H" Input Voltage	SCLK,CE,CLKC	V_{DD}=2.5 to 5.5V	0.8V_{DD}		5.5	V
V_{IH2}	"H" Input Voltage	SIO		0.8V_{DD}		V_{DD}+0.3	
V_{IL}	"L" Input Voltage	SCLK,CE,SIO,CLKC		–0.3		0.2V_{DD}	
I_{OH}	"H" Output Current	SIO,32KOUT	V_{OH}=V_{DD}–0.5V			–0.5	mA
I_{OL1}	"L" Output Current	$\overline{INTR}$	V_{OL}=0.4V	2			mA
I_{OL2}		SIO,32KOUT	V_{OL}=0.4V	0.5			
I_{IL}	Input Leakage Current	SCLK	V_I=5.5V or Vss V_{DD}=5.5V	–1		1	µA
R_{DNCE}	Pull-down Resistance	CE		40	120	400	kΩ
I_{CLKC}	Pull-down Resistance Input Current	CLKC			0.35	1.0	µA
I_{OZ1}	Output Off-state Leakage Current	SIO	Vo=5.5V or Vss V_{DD}=5.5V	–1		1	µA
I_{OZ2}		$\overline{INTR}$	V_O=5.5V	–1		1	
I_{DD1}	Standby Current	V_{DD}	V_{DD}=3V,CE=OPEN Output=OPEN 32KOUT=Off mode*1		0.35	0.8	µA
V_{DETH}	Supply Voltage Monitoring Voltage ("H")	V_{DD}	Topt=–30 to +70°C	1.90	2.10	2.30	V
V_{DETL}	Supply Voltage Monitoring Voltage ("L")	V_{DD}	Topt=–30 to +70°C	1.45	1.60	1.80	V
C_G	Internal Oscillation Capacitance 1	OSCIN			12		pF
C_D	Internal Oscillation Capacitance 2	OSCOUT			12		

*1) For standby current for outputting 32.768-kHz clock pulses from the 32KOUT pin, see "USAGES, 7. Typical Characteristics".

AC ELECTRICAL CHARACTERISTICS

Unless otherwisespecified : Vss=0V, Topt=–40 to +85°C
Input/output conditions : V_{IH}=0.8 × V_{DD}, V_{IL}=0.2 × V_{DD}, V_{OH}=0.8 × V_{DD}, V_{OL}=0.2 × V_{DD}, C_L=50pF

Symbol	Item	Conditions	V_{DD}≥2.5V			V_{DD}≥4.5			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{CES}	CE Set-up Time		400			200			ns
t_{CEH}	CE Hold Time		400			200			ns
t_{CR}	CE Recovery Time		62			62			µs
f_{SCLK}	SCLK Clock Frequency				1.0			2.0	MHz
t_{CKH}	SCLK Clock “H” Time		400			200			ns
t_{CKL}	SCLK Clock “L” Time		400			200			ns
t_{CKS}	SCLK Set-up Time		200			100			ns
t_{RD}	Data Output Delay Time				300			150	ns
t_{RZ}	Data Output Floating Time				300			150	ns
t_{CEZ}	Data Output Floating Time After Falling of CE				300			150	ns
t_{DS}	Input Data Set-up Time		200			100			ns
t_{DH}	Input Data Hold Time		200			100			ns



*) For read/write timing, see Paragraph “USAGES, 1.5 Considerations in Reading and Writing Time Data”

GENERAL DESCRIPTION

1. Interface with CPU

The R×5C338A are connected to the CPU by three signal lines CE (Chip Enable), SCLK (Serial Clock), SIO (Serial Input/Output), through which it reads and write data from and to the CPU. The CPU can access when the CE pin is held high. Access clock pulses have a maximum frequency of 2MHz (at 5 volts), allowing high-speed data transfer to the CPU.

2. Clock and Calendar Function

The R×5C338A read and write time data from and to the CPU in units ranging from seconds to the last two digits of the calendar year. The calendar year will automatically be identified as a leap year when its last two digits are a multiple of 4. Also available is the 1900/2000 identification bit for Year 2000 compliance. Consequently, leap years up to the year 2099 can automatically be identified as such.

*) The year 2000 is a leap year while the year 2100 is not a leap year.

3. Alarm Function

The R×5C338A incorporate an alarm circuit configured to generate interrupt signals to the CPU for output at preset times. The alarm circuit allows two types of alarm settings specified by the Alarm_W registers and the Alarm_D registers. The Alarm_W registers allow week, hour, and minute alarm settings including combinations of multiple day-of-week settings such as “Monday, Wednesday, and Friday” and “Saturday and Sunday”. The Alarm_D registers allow hour and minute alarm settings. Both Alarm_W and Alarm_D signals are output from the $\overline{\text{INTR}}$ pin. The current alarm settings specified by these two registers can be checked from the CPU by using a polling function..

4. High-precision Oscillation Adjustment Function

The R×5C338A have built-in oscillation stabilization capacitors (C_G and C_D), which can be connected to an external crystal oscillator to configure an oscillation circuit. To correct deviations in the oscillation frequency of the crystal oscillator, the oscillation adjustment circuit is configured to allow correction of a time count gain or loss (up to ±1.5 ppm at 25°C) from the CPU within a maximum range of approximately ±189 ppm in increments of approximately 3 ppm. Such oscillation frequency adjustment in each system has the following advantages:

- Allows timekeeping with much higher precision than conventional real-time clocks while using a crystal oscillator with a wide range of precision variations.
- Corrects seasonal frequency deviations through seasonal oscillation adjustment.
- Allows timekeeping with higher precision particularly in systems with a temperature sensing function through oscillation adjustment in tune with temperature fluctuations.

5. Oscillation Halt Sensing Function and Supply Voltage Monitoring Function

The R×5C338A incorporate an oscillation halt sensing circuit equipped with internal registers configured to record any past oscillation halt, thereby identifying whether they are powered on from 0 volts or battery backed-up. As such, the oscillation halt sensing circuit is useful for judging the validity of time data.
The R×5C338A also incorporate a supply voltage monitoring circuit equipped with internal registers configured to record any drop in supply voltage below a certain threshold value. Supply voltage monitoring threshold settings can be selected between 2.1 and 1.6 volts through internal register settings.
The oscillation halt sensing circuit is configured to confirm the established invalidation of time data in contrast to the supply voltage monitoring circuit intended to confirm the potential invalidation of time data. Further, the supply voltage monitoring circuit can be applied to battery supply voltage monitoring.

6. Periodic Interrupt Function

The R×5C338A incorporate a periodic interrupt circuit configured to generate periodic interrupt signals aside from interrupt signals generated by the alarm circuit for output from the $\overline{\text{INTR}}$ pin. Periodic interrupt signals have five selectable frequency settings of 2Hz (once per 0.5 seconds), 1Hz (once per 1 second), 1/60Hz (once per 1 minute), 1/3600Hz (once per 1 hour), and monthly (the first day of every month). Further, periodic interrupt signals also have two selectable waveforms of a normal pulse form (with a frequency of 2Hz or 1Hz) and special form adapted to interruption from the CPU in the level mode (with second, minute, hour, and month interrupts). The register records of periodic interrupt signals can be monitored by using a polling function.

7. 32-kHz Clock Output Function

The R×5C338A incorporate a 32-kHz clock circuit configured to generate clock pulses with the oscillation frequency of a 32.768-kHz crystal oscillator for output from the 32KOUT pin. The 32KOUT pin is CMOS output and the output from this pin is enabled and disabled when the CLKC pin is held high, and low or open, respectively. The 32-kHz clock output can be disabled by certain register settings. But it cannot be disabled without manipulation of any two registers with different addresses, to prevent disabling in such events as the runaway of the CPU. The 32-kHz clock circuit is enabled at power-on, when the CLKC pin is held high.

FUNCTIONAL DESCRIPTIONS

1. Address Mapping

	Address				Register	Data*1							
	A_3	A_2	A_1	A_0		D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Second Counter	–*2	S_{40}	S_{20}	S_{10}	S_8	S_4	S_2	S_1
1	0	0	0	1	Minute Counter	–	M_{40}	M_{20}	M_{10}	M_8	M_4	M_2	M_1
2	0	0	1	0	Hour Counter	–	–	H_{20} $P/\overline{A}$	H_{10}	H_8	H_4	H_2	H_1
3	0	0	1	1	Day-of-week Counter	–	–	–	–	–	W_4	W_2	W_1
4	0	1	0	0	Day-of-month Counter	–	–	D_{20}	D_{10}	D_8	D_4	D_2	D_1
5	0	1	0	1	Month Counter and Century Bit	$\overline{19}/20$	–	–	MO_{10}	MO_8	MO_4	MO_2	MO_1
6	0	1	1	0	Year Counter	Y_{80}	Y_{40}	Y_{20}	Y_{10}	Y_8	Y_4	Y_2	Y_1
7	0	1	1	1	Oscillation Adjustment Register*3	(0)*4	F_6	F_5	F_4	F_3	F_2	F_1	F_0
8	1	0	0	0	Alarm_W (minute register)	–	WM_{40}	WM_{20}	WM_{10}	WM_8	WM_4	WM_2	WM_1
9	1	0	0	1	Alarm_W (hour register)	–	–	WH_{20} $WP/\overline{A}$	WH_{10}	WH_8	WH_4	WH_2	WH_1
A	1	0	1	0	Alarm_W (day-of-week register)	–	WW_6	WW_5	WW_4	WW_3	WW_2	WW_1	WW_0
B	1	0	1	1	Alarm_D (minute register)	–	DM_{40}	DM_{20}	DM_{10}	DM_8	DM_4	DM_2	DM_1
C	1	1	0	0	Alarm_D (hour register)	–	–	DH_{20} $DP/\overline{A}$	DH_{10}	DH_8	DH_4	DH_2	DH_1
D	1	1	0	1		–	–	–	–	–	–	–	–
E	1	1	1	0	Control Register 1*3	WALE	DALE	$\overline{12}/24$	$\overline{CLEN2}$	TEST	CT_2	CT_1	CT_0
F	1	1	1	1	Control Register 2*3	VDSL	VDET	SCRATCH	XSTP	$\overline{CLEN1}$	CTFG	WAFG	DAFG

*1) All the data listed above accept both reading and writing.
*2) The data marked with "–" is invalid for writing and reset to 0 for reading.
*3) When the XSTP bit is set to 1 in control register 2, all the bits are reset to 0 in oscillation adjustment register 1, control register 1 and control register 2 excluding the XSTP bit.
*4) Writing to the oscillation adjustment register requires zero filling the (0) bit.

2. Register Settings

2.1 Control Register 1 (at Address Eh)

D7	D6	D5	D4	D3	D2	D1	D0	
WALE	DALE	$\overline{12}$/24	$\overline{CLEN2}$	TEST	CT_2	CT_1	CT_0	(For writing)
WALE	DALE	$\overline{12}$/24	$\overline{CLEN2}$	TEST	CT_2	CT_1	CT_0	(For reading)
0	0	0	0	0	0	0	0	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

2.1-1 WALE, DALE

Alarm_W Enable Bit and Alarm_D Enable Bit

WALE, DALE	Description	
0	Disabling the alarm interrupt circuit (under the control of the settings of the Alarm_W registers and the Alarm_D registers).	(Default setting)
1	Enabling the alarm interrupt circuit (under the control of the settings of the Alarm_W registers and the Alarm_D registers)	

2.1-2 $\overline{12}$/24-hour Mode Selection Bit

$\overline{12}$/24-hour Time Display System Selection bit

$\overline{12}$/24	Description
0	Selecting the 12-hour mode with a.m. and p.m. indications.
1	Selecting the 24-hour mode

Setting the $\overline{12}$/24 bit to 0 and 1 specifies the 12-hour mode and the 24-hour mode, respectively.

Table of Time Digit Indications

24-hour mode	12-hour mode	24-hour mode	12-hour mode
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

*) Setting the $\overline{12}$/24 bit should precede writing time data.

2.1-3 $\overline{\text{CLEN2}}$

32-kHz Clock Output Bit 2

$\overline{\text{CLEN2}}$	Description	
0	Enabling the 32-kHz clock circuit	(Default setting)
1	Disabling the 32-kHz clock circuit	

For the R×5C338A, setting the $\overline{\text{CLEN2}}$ bit or the $\overline{\text{CLEN1}}$ bit (D3 in the control register 2) to 0, and the CLKC pin to high specifies generating clock pulses with the oscillation frequency of the 32.768-kHz crystal oscillator for output from the 32KOUT pin. Conversely, setting both the $\overline{\text{CLEN1}}$ and the $\overline{\text{CLEN2}}$ bit to 1 or CLKC pin to low specifies disabling ("L") such output.

2.1-4 TEST

Test Bit

TEST	Description	
0	Normal operation mode	(Default setting)
1	Test mode	

The TEST bit is used only for testing in the factory and should normally be set to 0.

2.1-5 CT_2, CT_1, and CT_0

Periodic Interrupt Selection Bits

CT_2	CT_1	CT_0	Description		
			Waveform mode	Interrupt cycle and falling timing	
0	0	0	—	Off ("H")	(Default setting)
0	0	1	—	Fixed at low ("L")	
0	1	0	Pulse Mode	2Hz (Duty cycle of 50%)	
0	1	1	Pulse Mode	1Hz (Duty cycle of 50%)	
1	0	0	Level Mode	Once per 1 second (Synchronized with second counter increment)	
1	0	1	Level Mode	Once per minute (at 00 seconds of every minute)	
1	1	0	Level Mode	Once per hour (at 00 minutes and 00 seconds of every hour)	
1	1	1	Level Mode	Once per month (at 00 hours, 00 minutes, and 00 seconds of first day of every month)	

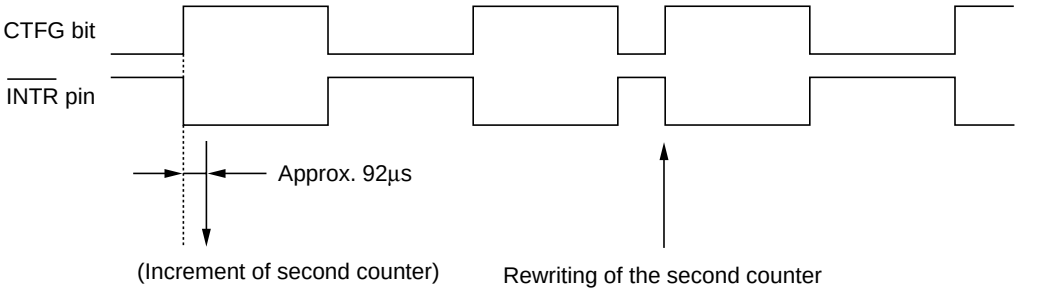
1) Pulse Mode : 2-Hz and 1-Hz clock pulses are output in synchronization with the increment of the second counter as illustrated in the timing chart on the next page.

2) Level Mode : periodic interrupt signals are output with selectable interrupt cycle settings of 1 second, 1 minute, 1 hour, and 1 month. The increment of the second counter is synchronized with the falling edge of periodic interrupt signals. For example, periodic interrupt signals with an interrupt cycle setting of 1 second are output in synchronization with the increment of the second counter as illustrated in the timing chart below.

3) When the oscillation adjustment circuit is used, the interrupt cycle will fluctuate once per 20 seconds as follows:
Pulse Mode : the "L" period of output pulses will increment or decrement by a maximum of ±3.784ms.
For example, 1-Hz clock pulses will have a duty cycle of 50 ±0.3784%.
Level Mode : a periodic interrupt cycle of 1 second will increment or decrement by a maximum of ±3.784ms.

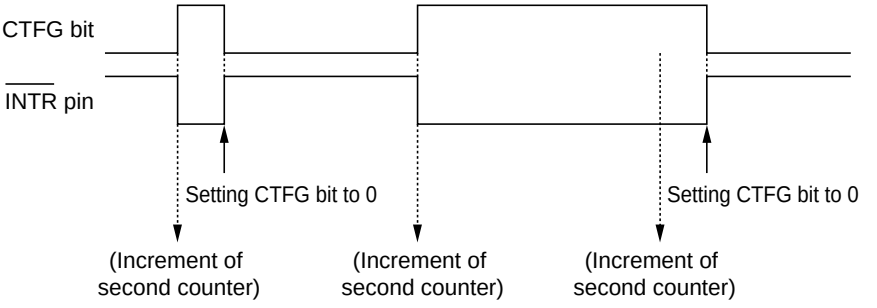
Relation Between the Mode Waveform and the CTFG Bit

• Pulse mode



*) In the pulse mode, the increment of the second counter is delayed by approximately 92µs from the falling edge of clock pulses. Consequently, time readings immediately after the falling edge of clock pulses may appear to lag behind the time counts of the real-time clocks by approximately 1 second. Rewriting the second counter will reset the other time counters of less than 1 second, driving the INTR pin low.

• Level mode



2.2 Control Register 2 (at Address Fh)

D7	D6	D5	D4	D3	D2	D1	D0	
VDSL	VDET	SCRATCH	XSTP	$\overline{\text{CLEN1}}$	CTFG	WAFG	DAFG	(For writing)
VDSL	VDET	SCRATCH	XSTP	$\overline{\text{CLEN1}}$	CTFG	WAFG	DAFG	(For reading)
0	0	0	1	0	0	0	0	Default setting*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

2.2-1 VDSL

Supply Voltage Monitoring Threshold Selection Bit

VDSL	Description	
0	Selecting the supply voltage monitoring threshold setting of 2.1 volts.	(Default setting)
1	Selecting the supply voltage monitoring threshold setting of 1.6 volts.	

The VDSL bit is intended to select the supply voltage monitoring threshold settings.

2.2-2 VDET

Supply Voltage Monitoring Result Indication Bit

VDET	Description	
0	Indicating supply voltage above the supply voltage monitoring threshold settings.	(Default setting)
1	Indicating supply voltage below the supply voltage monitoring threshold settings.	

Once the VDET bit is set to 1, the supply voltage monitoring circuit will be disabled while the VDET bit will hold the setting of 1. The VDET bit accepts only the writing of 0, which restarts the supply voltage monitoring circuit. Conversely, setting the VDET bit to 1 causes no event.

2.2-3 SCRATCH

Scratch Bit

SCRATCH	Description	
0		(Default setting)
1		

The SCRATCH bit is intended for scratching and accepts the reading and writing of 0 and 1. The SCRATCH bit will be set to 0 when the XSTP bit is set to 1 in the control register 2.

2.2-4 XSTP

Oscillator Halt Sensing Bit

XSTP	Description	
0	Sensing a normal condition of oscillation	
1	Sensing a halt of oscillation	(Default setting)

The XSTP bit is for sensing a halt in the oscillation of the crystal oscillator. The oscillation halt sensing circuit operates only when the CE pin is "L".

- The XSTP bit will be set to 1 once a halt in the oscillation of the crystal oscillator is caused by such events as power-on from 0 volts and a drop in supply voltage. The XSTP bit will hold the setting of 1 even after the restart of oscillation. As such, the XSTP bit can be applied to judge the validity of clock and calendar data after power-on or a drop in supply voltage.
- When the XSTP bit is set to 1, all bits will be reset to 0 in the oscillation adjustment register, control register 1, and control register 2, stopping the output from the $\overline{\text{INTR}}$ pin and starting the output of 32.768-kHz clock pulses from the 32KOUT pin.
  (32KOUT output is disabled when CLKC pin is set to low.)
- The XSTP bit accepts only the writing of 0, which restarts the oscillation halt sensing circuit. Conversely, setting the XSTP bit to 1 causes no event.

2.2-5 $\overline{\text{CLEN1}}$

32-kHz Clock Output Bit 1

$\overline{\text{CLEN1}}$	Description	
0	Enabling the 32-kHz clock output	(Default setting)
1	Disabling the 32-kHz clock output	

Setting the $\overline{\text{CLEN1}}$ bit or the $\overline{\text{CLEN2}}$ bit (D4 in control register 1) to 0, and the CLKC pin to high specifies generating clock pulses with the oscillation frequency of the 32.768-kHz crystal oscillator for output from the 32KOUT pin. Conversely, setting both the $\overline{\text{CLEN1}}$ bit and the $\overline{\text{CLEN2}}$ bit to 1 or the CLKC pin to low specifies disabling ("L") such output.

2.2-6 CTFG

Periodic Interrupt Flag Bit

CTFG	Description	
0	Periodic interrupt output "H" (OFF)	(Default setting)
1	Periodic interrupt output "L" (ON)	

The CTFG bit is set to 1 when the periodic interrupt signals are output from the $\overline{\text{INTR}}$ pin ("L"). The CTFG bit accepts only the writing of 0 in the level mode, which disables ("H") the $\overline{\text{INTR}}$ pin until it is enabled ("L") again in the next interrupt cycle. Conversely, setting the CTFG bit to 1 causes no event.

2.2-7 WAFG and DAFG

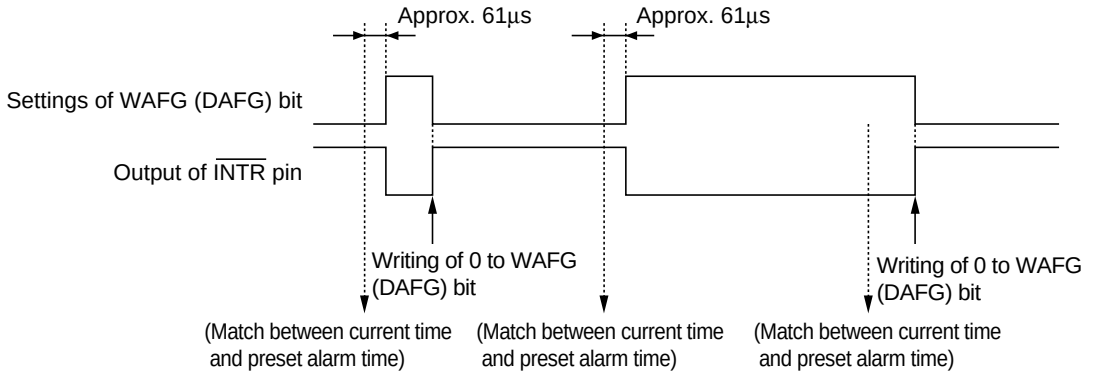
Alarm_W Flag Bit and Alarm_D Flag Bit

WAFG, DAFG	Description
0	Indicating a mismatch between current time and preset alarm time
1	Indicating a match between current time and preset alarm time

(Default setting)

The WAFG and DAFG bits are valid only when the WALE and DALE bits have the setting of 1, which is caused approximately 61µs after any match between current time and preset alarm time specified by the Alarm_W registers and the Alarm_D registers. The WAFG and DAFG bits accept only the writing of 0, which disables ("H") the $\overline{\text{INTR}}$ pin until it is enabled ("L") again at the next preset alarm time. Conversely, setting the WAFG and DAFG bits to 1 causes no event. The WAFG and DAFG bits will have the reading of 0 when the alarm interrupt circuit is disabled with the WALE and DALE bits set to 0. The settings of the WAFG and DAFG bits are synchronized with the output of the $\overline{\text{INTR}}$ pin as shown in the timing chart below.

Output Relationships Between the WAFG or DAFG Bit and $\overline{\text{INTR}}$



2.3 Time Counters (at Addresses 0h to 2h)

· Time digit display (BCD format) as follows:

The second digits range from 00 to 59 and are carried to the minute digit in transition from 59 to 00.

The minute digits range from 00 to 59 and are carried to the hour digits in transition from 59 to 00.

The hour digits range as shown in "2.1-2 $\overline{12}$/24: $\overline{12}$-/24-hour Mode Selection Bit" and are carried to the day-of-month and day-of-week digits in transition from PM11 to AM12 or from 23 to 00.

· Any writing to the second counter resets divider units of less than 1 second.

· Any carry from lower digits with the writing of non-existent time may cause the time counters to malfunction. Therefore, such incorrect writing should be replaced with the writing of existent time data.

2.3-1 Second Counter (at Address 0h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	S_{40}	S_{20}	S_{10}	S_8	S_4	S_2	S_1	(For writing)
0	S_{40}	S_{20}	S_{10}	S_8	S_4	S_2	S_1	(For reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.3-2 Minute Counter (at Address 1h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	M_{40}	M_{20}	M_{10}	M_8	M_4	M_2	M_1	(For writing)
0	M_{40}	M_{20}	M_{10}	M_8	M_4	M_2	M_1	(For reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.3-3 Hour Counter (at Address 2h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	P/$\overline{A}$ or H_{20}	H_{10}	H_8	H_4	H_2	H_1	(For writing)
0	0	P/$\overline{A}$ or H_{20}	H_{10}	H_8	H_4	H_2	H_1	(For reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

2.4 Day-of-week Counter (at Address 3h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	—	—	—	W_4	W_2	W_1	(For writing)
0	0	0	0	0	W_4	W_2	W_1	(For reading)
0	0	0	0	0	Indefinite	Indefinite	Indefinite	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

- The day-of-week counter is incremented by 1 when the day-of-week digits are carried to the day-of-month digits.
- Day-of-week display (incremented in septimal notation):
  $(W_4, W_2, W_1) = (0, 0, 0) \rightarrow (0, 0, 1) \rightarrow \cdots \rightarrow (1, 1, 0) \rightarrow (0, 0, 0)$
- Correspondences between days of the week and the day-of-week digits are user-definable (e.g. Sunday = 0, 0, 0)
- The writing of (1, 1, 1) to (W_4, W_2, W_1) is prohibited except when days of the week are unused.

2.5 Calendar Counters (at Address 4h to 6h)

- The calendar counters are configured to display the calendar digits in BCD format by using the automatic calendar function as follows:

  The day-of-month digits (D_{20} to D_1) range from 1 to 31 for January, March, May, July, August, October, and December; from 1 to 30 for April, June, September, and November; from 1 to 29 for February in leap years; from 1 to 28 for February in ordinary years.

  The day-of-month digits are carried to the month digits in reversion from the last day of the month to 1. The month digits (MO_{10} to MO_1) range from 1 to 12 and are carried to the year digits in reversion from 12 to 1.

  The year digits (Y_{80} to Y_1) range from 00 to 99 (00, 04, 08, ... , 92, and 96 in leap years) and are carried to the $\overline{19}/20$ digits in reversion from 99 to 00.

  The $\overline{19}/20$ digits cycle between 0 and 1 in reversion from 99 to 00 in the year digits.
- Any carry from lower digits with the writing of non-existent calendar data may cause the calendar counters to malfunction. Therefore, such incorrect writing should be replaced with the writing of existent calendar data.

2.5-1 Day-of-month Counter (at Address 4h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	D_{20}	D_{10}	D_8	D_4	D_2	D_1	(For writing)
0	0	D_{20}	D_{10}	D_8	D_4	D_2	D_1	(For reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.5-2 Month Counter + Century Bit (at Address 5h)

D7	D6	D5	D4	D3	D2	D1	D0	
$\overline{19}/20$	—	—	MO_{10}	MO_8	MO_4	MO_2	MO_1	(For writing)
$\overline{19}/20$	0	0	MO_{10}	MO_8	MO_4	MO_2	MO_1	(For reading)
Indefinite	0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.5-3 Year Counter (at Address 6h)

D7	D6	D5	D4	D3	D2	D1	D0	
Y_{80}	Y_{40}	Y_{20}	Y_{10}	Y_8	Y_4	Y_2	Y_1	(For writing)
Y_{80}	Y_{40}	Y_{20}	Y_{10}	Y_8	Y_4	Y_2	Y_1	(For reading)
Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

2.6 Oscillation Adjustment Register (at Address 7h)

D7	D6	D5	D4	D3	D2	D1	D0	
(0)	F_6	F_5	F_4	F_3	F_2	F_1	F_0	(For writing)
(0)	F_6	F_5	F_4	F_3	F_2	F_1	F_0	(For reading)
0	0	0	0	0	0	0	0	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

2.6-1 (0) Bit

The (0) bit should be set to 0 to allow writing to the oscillation adjustment register. The (0) bit will be set to 0 when the XSTP bit is set to 1 in the control register 2.

2.6-2 F_6 to F_0

The oscillation adjustment circuit is configured to change time counts of 1 second on the basis of the settings of the oscillation adjustment register when the second digits read 00, 20, or 40 seconds. Normally, the second counter is incremented once per 32768 32.768-kHz clock pulses generated by the crystal oscillator. Writing to the F_6 to F_0 bits activates the oscillation adjustment circuit.

- The oscillation adjustment circuit will not operate with the same timing (00, 20, or 40 seconds) as the timing of writing to the oscillation adjustment register.
- The F_6 bit setting of 0 causes an increment of time counts by $((F_5, F_4, F_3, F_2, F_1, F_0) - 1) \times 2$.
  The F_6 bit setting of 1 causes a decrement of time counts by $((\overline{F_5}, \overline{F_4}, \overline{F_3}, \overline{F_2}, \overline{F_1}, \overline{F_0}) + 1) \times 2$.
  The settings of "*, 0, 0, 0, 0, 0, *" ("*" representing either "0" or "1") in the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits cause neither an increment nor decrement of time counts.

Example:

When the second digits read 00, 20, or 40, the settings of "0, 0, 0, 0, 1, 1, 1" in the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits cause an increment of the current time counts of 32768 by $(7-1) \times 2$ to 32780 (a current time count loss). When the second digits read 00, 20, or 40, the settings of "0, 0, 0, 0, 0, 0, 1" in the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits cause neither an increment nor a decrement of the current time counts of 32768.

When the second digits read 00, 20, or 40, the settings of "1, 1, 1, 1, 1, 1, 0" in the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits cause a decrement of the current time counts of 32768 by $(-2) \times 2$ to 32764 (a current time count gain).

An increase of two clock pulses once per 20 seconds causes a time count loss of approximately 3ppm (2 / (32768 × 20=3.051ppm). Conversely, a decrease of two clock pulses once per 20 seconds causes a time count gain of 3ppm. Consequently, deviations in time counts can be corrected with a precision of ±1.5ppm. Note that the oscillation adjustment circuit is configured to correct deviations in time counts and not the oscillation frequency of the 32.768-kHz clock pulses. For further details, see "USAGE, 2.4 Oscillation Adjustment Circuit".

2.7 Alarm_W Register (at Address 8h to Ah)

2.7-1 Alarm_W Minute Register (at Address 8h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	WM_{40}	WM_{20}	WM_{10}	WM_8	WM_4	WM_2	WM_1	(For writing)
0	WM_{40}	WM_{20}	WM_{10}	WM_8	WM_4	WM_2	WM_1	(For reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.7-2 Alarm_W Hour Register (at Address 9h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	WH_{20},WP/$\overline{A}$	WH_{10}	WH_8	WH_4	WH_2	WH_1	(For writing)
0	0	WH_{20},WP/$\overline{A}$	WH_{10}	WH_8	WH_4	WH_2	WH_1	(For reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.7-3 Alarm_W Day-of-week Register (at Address Ah)

D7	D6	D5	D4	D3	D2	D1	D0	
—	WW_6	WW_5	WW_4	WW_3	WW_2	WW_1	WW_0	(For writing)
0	WW_6	WW_5	WW_4	WW_3	WW_2	WW_1	WW_0	(For reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

- The D5 bit of the Alarm_W hour register represents WP/$\overline{A}$ when the 12-hour mode is selected (0 for a.m. and 1 for p.m.). and WH_{20} when the 24-hour mode is selected (tens in the hour digits).
- The Alarm _W registers should not have any non-existent alarm time settings. (Note that any mismatch between current time and preset alarm time specified by the Alarm_W registers may disable the alarm circuit.)
- When the 12-hour mode is selected, the hour digits read 12 and 32 for 0 a.m. and 0 p.m., respectively (see "2.1-2 $\overline{12}$/24: $\overline{12}$-/24-hour Mode Selection Bit").
- WW_0 to WW_6 correspond to W_4, W_2, and W_1 of the day-of-week counter with settings ranging from (0, 0, 0) to (1, 1, 0).
- WW_0 to WW_6 with respective settings of 0 disable the outputs of the Alarm_W registers.

Example of Alarm Time Setting

Preset alarm time	Day-of-week							12-hour mode				24-hour mode			
	Sun. WW_0	Mon. WW_1	Tue. WW_2	Wed. WW_3	Thu. WW_4	Fri. WW_5	Sat. WW_6	10-hour	1-hour	10-min	1-min	10-hour	1-hour	10-min	1-min
00:00 a.m. on all days	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
01:30 a.m. on all days	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
11:59 a.m. on all days	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
00:00 p.m. on Mondays to Fridays	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
01:30 p.m. on Sundays	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
11:59 p.m. on Mondays, Wednesdays, and Fridays	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

Note that the correspondence between WW_0 to WW_6 and the days of the week shown in the above table is only an example and not mandatory.

2.8 Alarm_D Register (at Address Bh and Ch)

2.8-1 Alarm_D Minute Register (at Address Bh)

D7	D6	D5	D4	D3	D2	D1	D0	
—	DM_{40}	DM_{20}	DM_{10}	DM_8	DM_4	DM_2	DM_1	(For writing)
0	DM_{40}	DM_{20}	DM_{10}	DM_8	DM_4	DM_2	DM_1	(For reading)
0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

2.8-2 Alarm_D Hour Register (at Address Ch)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	DH_{20},$DP/\overline{A}$	DH_{10}	DH_8	DH_4	DH_2	DH_1	(For writing)
0	0	DH_{20},$DP/\overline{A}$	DH_{10}	DH_8	DH_4	DH_2	DH_1	(For reading)
0	0	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Indefinite	Default settings*

*) Default settings: Default value means read/written values when the XSTP bit is set to "1" due to power-on from 0 volts or supply voltage drop.

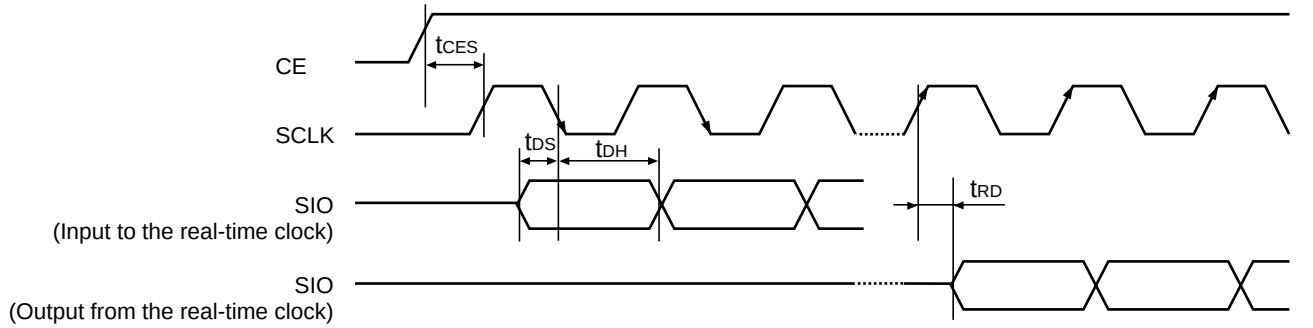
- The D5 bit represents $DP/\overline{A}$ when the 12-hour mode is selected (0 for a.m. and 1 for p.m.). and DH_{20} when the 24-hour mode is selected (tens in the hour digits).
- The Alarm_D registers should not have any non-existent alarm time settings. (Note that any mismatch between current time and preset alarm time specified by the Alarm_D registers may disable the alarm circuit.)
- When the 12-hour mode is selected, the hour digits read 12 and 32 for 0 a.m. and 0 p.m., respectively (see "2.1-2 $\overline{12}$/24: $\overline{12}$-/24-hour Mode Selection Bit").

USAGES

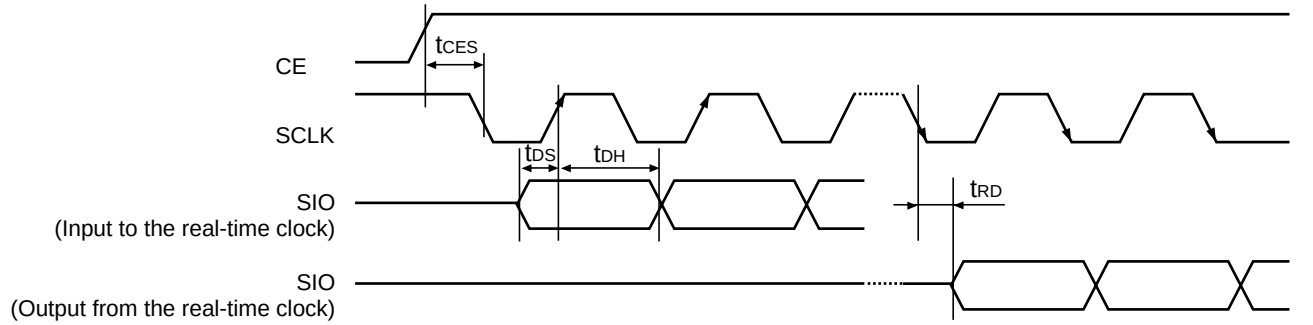
1. Data Transfer Formats

1.1 Timing Between CE Pin Transition and Data Input/Output

The R×5C338A adopt a 3-wire serial interface by which it uses the CE (Chip Enable), SCLK (Serial Clock), and SIO (Serial Input/Output), pins to receive and send data to and from the CPU. The 3-wire serial interface provides two types of input/output timings with which the output and input from the SIO pin output and input are synchronized with the rising and falling edges of the SCLK pin input, respectively, and vice versa. The R×5C338A are configured to select either one of two different input/output timings depending on the level of the SCLK pin in the low to high transition of the CE pin. Namely, when the SCLK pin is held low in the low to high transition of the CE pin, the models will select the timing with which the output and input from the SIO pin are synchronized with the rising and falling edges of the SCLK pin input, respectively, as illustrated in the timing chart below.

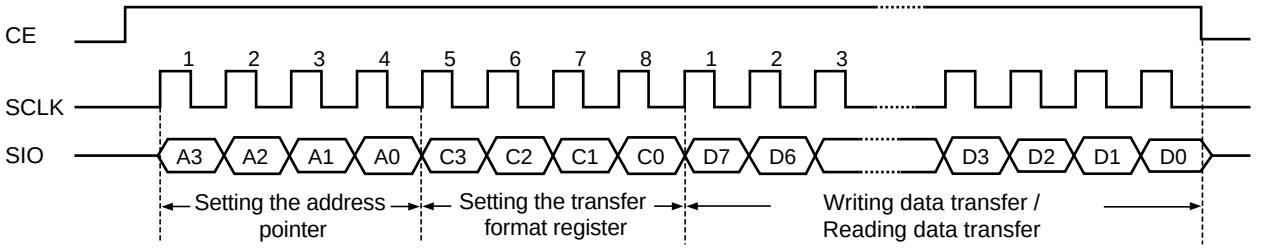


Conversely, when the SCLK pin is held high in the low to high transition of the CE pin, the models will select the timing with which the output and input from the SIO pin are synchronized with the falling and rising edges of the SCLK pin input, respectively as illustrated in the timing chart below.



1.2 Data Transfer Formats

Data transfer is commenced in the low to high transition of the CE pin input and completed in its high to low transition. Data transfer is conducted serially in multiple units of 1 byte (8 bits). The former 4 bits are used to specify in the address pointer a head address with which data transfer is to be commenced from the host. The latter 4 bits are used to select either reading data transfer or writing data transfer and set the transfer format register to specify an appropriate data transfer format. All data transfer formats are designed to transfer the most significant bit (MSB) first.



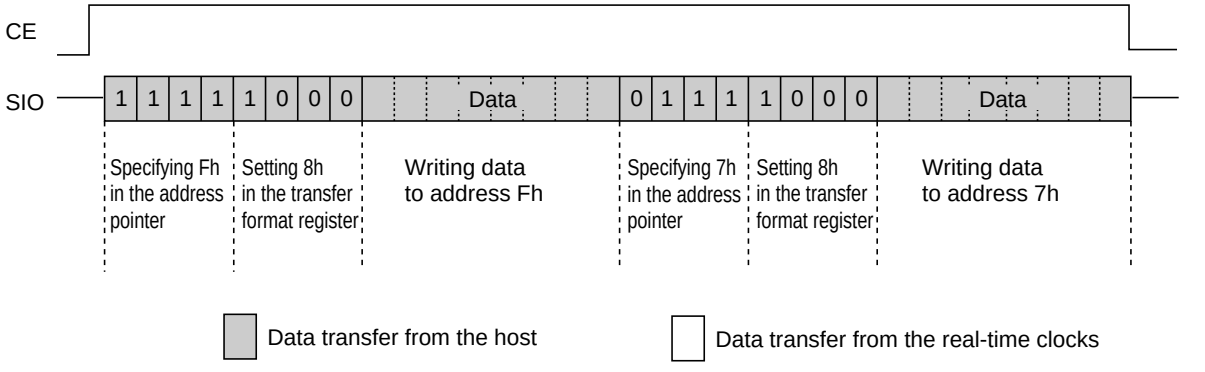
Two types of data transfer formats are available for reading data transfer and writing data transfer each.

1.3 Writing Data Transfer Formats

1.3-1 1-byte Writing Data Transfer Format

The first type of writing data transfer format is designed to transfer 1-byte data at a time and can be selected by specifying in the address pointer a head address with which writing data transfer is to be commenced and then writing the setting of 8h to the transfer format register. This 1-byte writing data transfer can be completed by driving the CE pin low or continued by specifying a new head address in the address pointer and setting the transfer format.

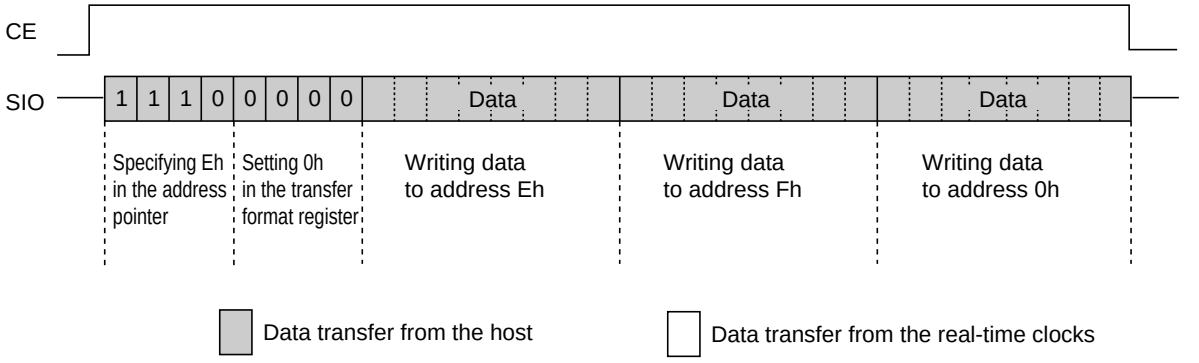
Example of 1-byte Writing Data Transfer (For Writing Data to Addresses Fh and 7h)



1.3-2 Burst Writing Data Transfer Format

The second type of writing data transfer format is designed to transfer a sequence of data serially and can be selected by specifying in the address pointer a head address with which writing data transfer is to be commenced and then writing the setting of 0h to the transfer format register. The address pointer is incremented for each transfer of 1-byte data and cycled from Fh to 0h. This burst writing data transfer can be completed by driving the CE pin low.

Example of Burst Writing Data Transfer (For Writing Data to Addresses Eh, Fh, and Oh)

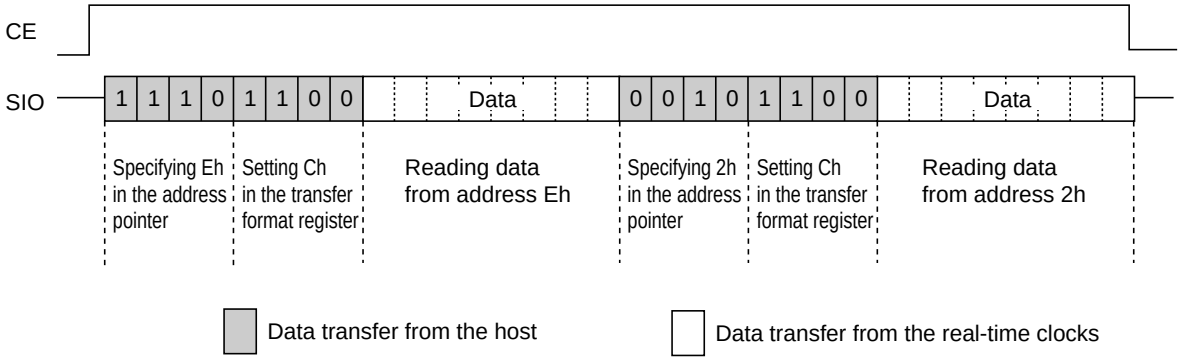


1.4 Reading Data Transfer Formats

1.4-1 1-byte Reading Data Transfer Format

The first type of reading data transfer format is designed to transfer 1-byte data at a time and can be selected by specifying in the address pointer a head address with which reading data transfer is to be commenced and then the setting of writing Ch to the transfer format register. This 1-byte reading data transfer can be completed by driving the CE pin low or continued by specifying a new head address in the address pointer and setting the transfer format.

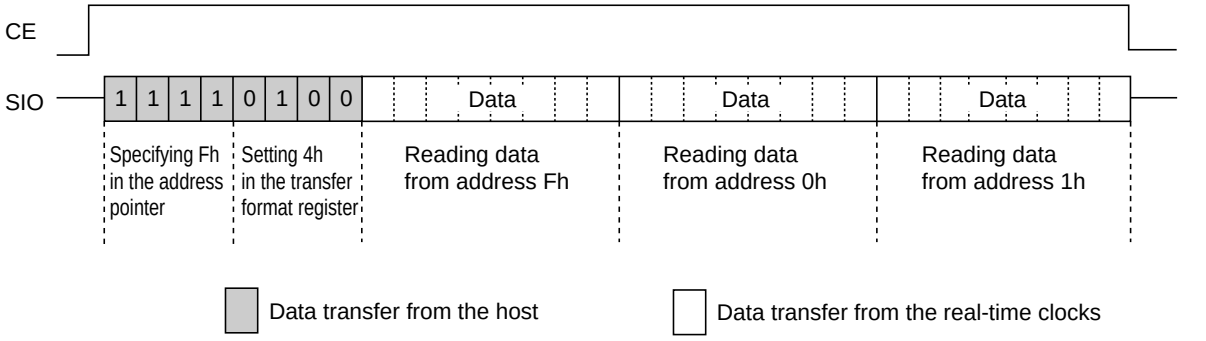
Example of 1-byte Reading Data Transfer (For Reading Data from Addresses Eh and 2h)



1.4-2 Burst Reading Data Transfer Format

The second type of reading data transfer format is designed to transfer a sequence of data serially and can be selected by specifying in the address pointer a head address with which reading data transfer is to be commenced and then writing the setting of 4h to the transfer format register. The address pointer is incremented for each transfer of 1-byte data and cycled from Fh to 0h. This burst reading data transfer can be completed by driving the CE pin low.

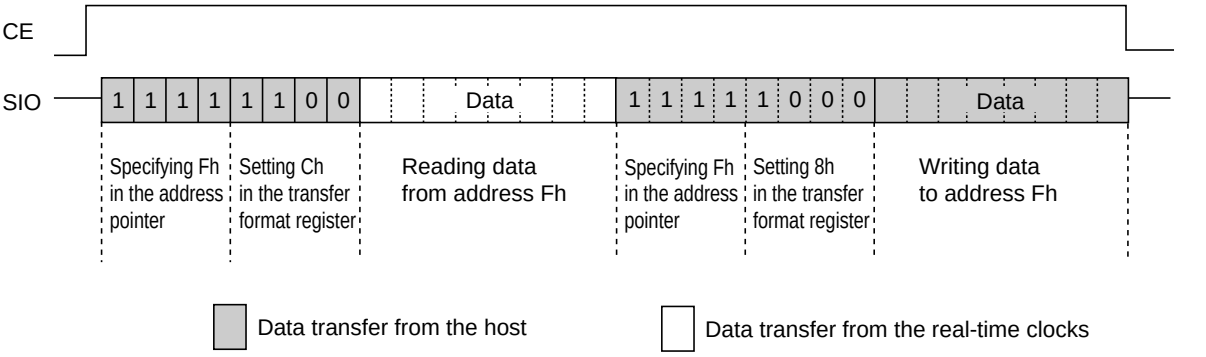
Example of Burst Reading Data Transfer (For Reading Data from Addresses Fh, 0h, and 1h)



1.4-3 Combination of 1-byte Reading and Writing Data Transfer Formats

The 1-byte reading and writing data transfer formats can be combined together and further followed by any other data transfer format.

Example of Combination of 1-byte Reading and Writing Data Transfer (For Reading and Writing Data from and to Address Fh)

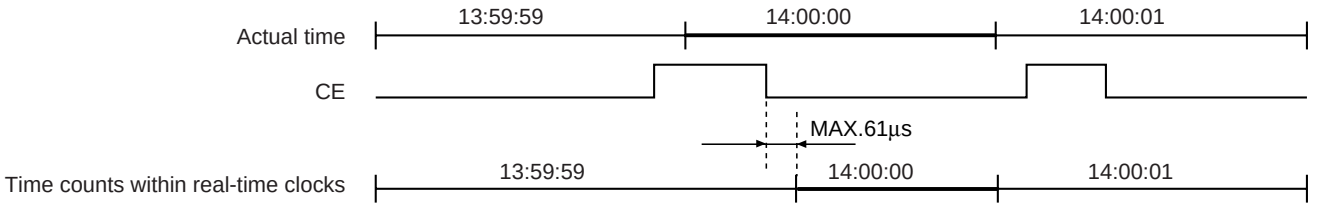


The reading and writing data transfer formats correspond to the settings in the transfer format register as shown in the table below.

	1-byte transfer	Burst (Successive) transfer
Writing data transfer (for writing to real-time clock)	8h (1,0,0,0)	0h (0,0,0,0)
Reading data transfer (for reading from real-time clock)	Ch (1,1,0,0)	4h (0,1,0,0)

1.5 Considerations in Reading and Writing Time Data

Any carry to the second digits in the process of reading or writing time data may cause reading or writing erroneous time data. For example, suppose a carry out of 13:59:59 into 14:00:00 occurs in the process of reading time data in the middle of shifting from the minute digits to the hour digits. At this moment, the second digits, the minute digits, and the hour digits read 59 seconds, 59 minutes, and 14 hours, respectively (indicating 14:59:59) to cause the reading of time data deviating from actual time virtually 1 hour. A similar error also occurs in writing time data. To prevent such errors in reading and writing time data, the R×5C338A have the function of temporarily locking any carry of the time digits during the high interval of the CE pin and unlocking such a carry in its high to low transition. Note that a carry of the second digits can be locked for only 1 second, during which time the CE pin should be driven low.

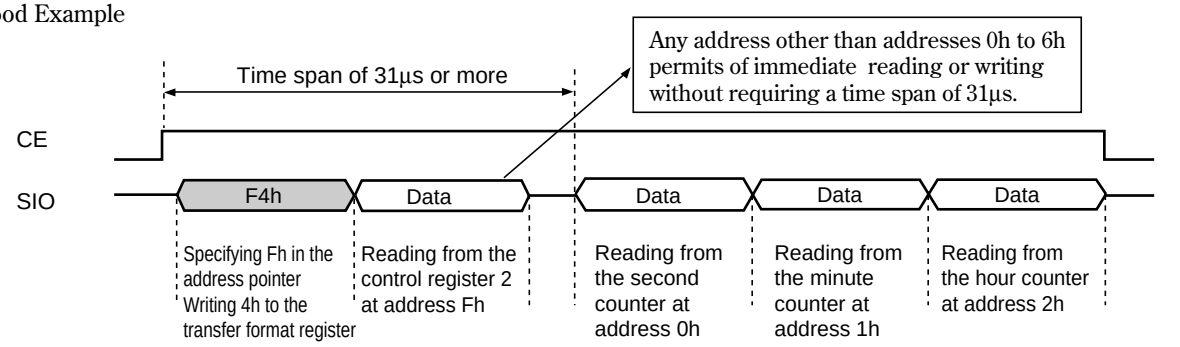


The effective use of this function requires the following considerations in reading and writing time data:

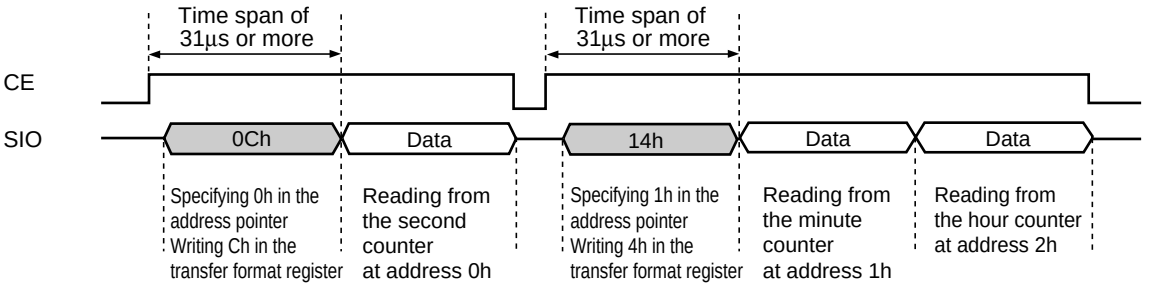
(1) Hold the CE pin high in each session of reading or writing time data.
(2) Ensure that the high interval of the CE pin lasts within 1 second. Should there be any possibility of the host going down in the process of reading or writing time data, make arrangements in the peripheral circuitry as to drive the CE pin low or open at the moment that the host actually goes down.
(3) Leave a time span of 31µs or more from the low to high transition of the CE pin to the start of access to addresses 0h to 6h in order that any ongoing carry of the time digits may be completed within this time span.
(4) Leave a time span of 61µs or more from the high to low transition of the CE pin to its low to high transition in order that any ongoing carry of the time digits during the high interval of the CE pin may be adjusted within this time span.
(5) The considerations listed in (1), (3), and (4) above are not required when the process of reading or writing time data is obviously free from any carry of the time digits (e.g. reading or writing time data in synchronization with the periodic interrupt function in the level mode or the alarm interrupt function).

Good and bad examples of reading and writing time data are illustrated on the next page.

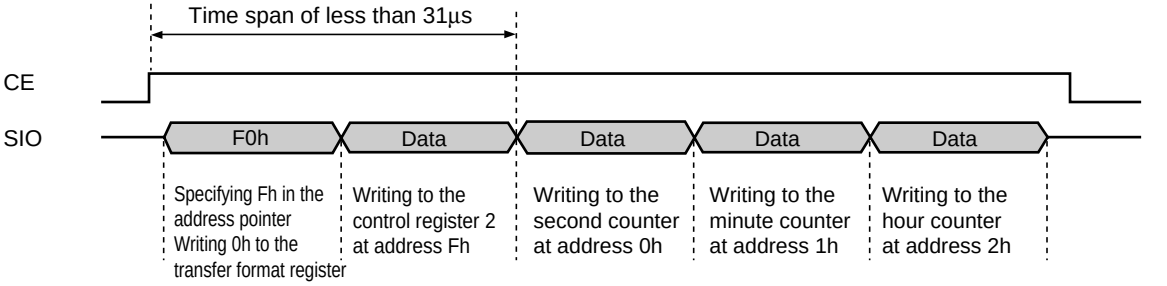
Good Example



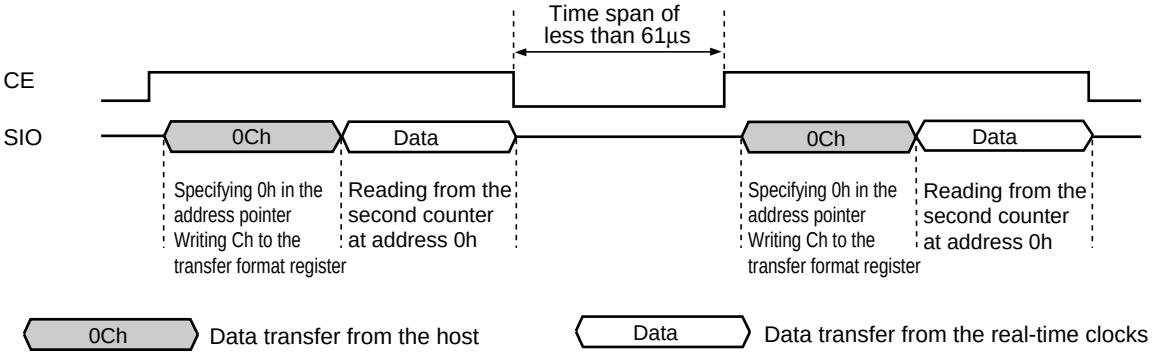
Bad Example (1) (Where the CE pin is once driven low in the process of reading time data)



Bad Example (2) (Where a time span of less than 31µs is left until the start of the process of writing time data)

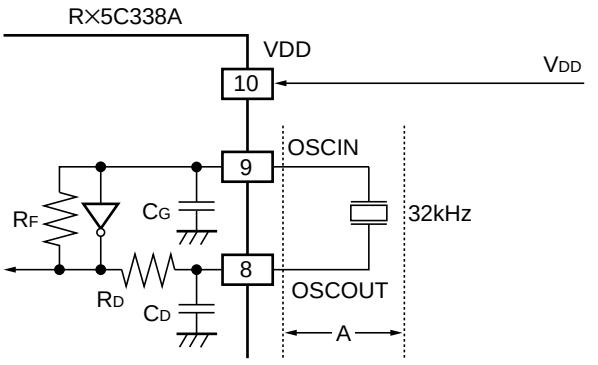


Bad Example (3) (Where a time span of less than 61µs is left between the adjacent processes of reading time data)



2. Configuration of Oscillation Circuit and Correction of Time Count Deviations

2.1 Configuration of Oscillating Circuit



Typical externally-equipped element
X'tal: 32.768kHz
(R_1=30kΩ TYP.)
(C_L=6pF to 8pF)

Standard values of internal elements
R_F=15MΩ TYP.
R_D=120kΩ TYP.
C_G, C_D=12pF TYP.

The oscillation circuit is driven at a constant voltage of approximately 1.2 volts relative to the level of the V_{SS} pin input. As such, it is configured to generate an oscillating waveform with a peak-to-peak voltage on the order of 1.2 volts on the positive side of the V_{SS} pin input.

Considerations in Handling Crystal Oscillators

Generally, crystal oscillators have basic characteristics including an equivalent series resistance (R_1) indicating the ease of their oscillation and a load capacitance (C_L) indicating the degree of their center frequency. Particularly, crystal oscillators intended for use with the R×5C338A are recommended to have a typical R_1 value of 30kΩ and a typical C_L value of 6 to 8pF. To confirm these recommended values, contact the manufacturers of crystal oscillators intended for use with these particular models.

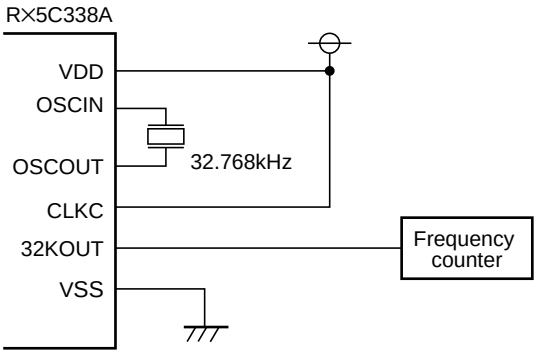
Considerations in Installing Components around the Oscillation Circuit

1) Install the crystal oscillator in the closest possible vicinity to the real-time clock ICs.
2) Avoid laying any signal lines or power lines in the vicinity of the oscillation circuit (particularly in the area marked "←A→" in the above figure).
3) Apply the highest possible insulation resistance between the OSCIN and OSCOUT pins and the printed circuit board.
4) Avoid using any long parallel lines to wire the OSCIN and OSCOUT pins.
5) Take extreme care not to cause condensation, which leads to various problems such as oscillation halt.

Other Relevant Considerations

1) For external input of 32.768-kHz clock pulses to the OSCIN pin:
   DC coupling: Prohibited due to an input level mismatch.
   AC coupling: Permissible except that the oscillation halt sensing circuit does not guarantee perfect operation because it may cause sensing errors due to such factors as noise.
2) To maintain stable characteristics of the crystal oscillator, avoid driving any other IC through 32.768-kHz clock pulses output from the OSCOUT pin.

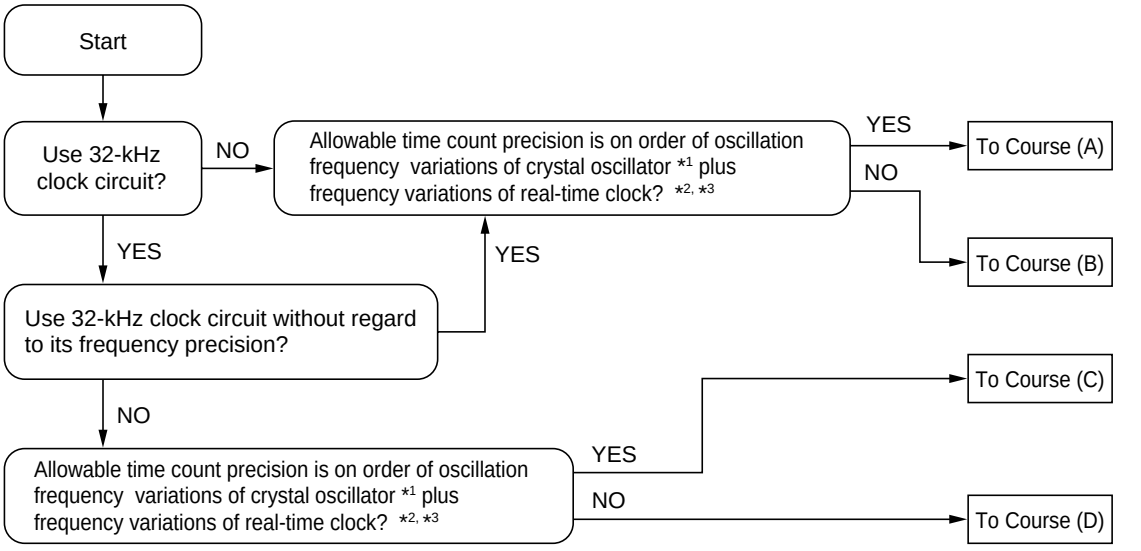
2.2 Measurement of Oscillation Frequency



★1) The R×5C338A are configured to generate 32.768-kHz clock pulses for output from the 32KOUT pin at power-on conditionally on setting the XSTP bit to 1 in the control register 2.
★2) A frequency counter with 6 (more preferably 7) or more digits on the order of 1ppm is recommended for use in the measurement of the oscillation frequency of the oscillation circuit.
★3) The CLKC input should be connected to the V_{DD} pin with a pull-up resistor.

2.3 Adjustment of Oscillation Frequency

The oscillation frequency of the oscillation circuit can be adjusted by varying procedures depending on the usage of the R×5C338A in the system into which they are to be built and on the allowable degree of time count errors. The flow chart below serves as a guide to selecting an optimum oscillation frequency adjustment procedure for the relevant system.



★1) Generally, crystal oscillators for commercial use are classified in terms of their center frequency depending on their load capacitance (C_L) and further divided into ranks on the order of ±10, ± 20, and ±50 ppm depending on the degree of their oscillation frequency variations.
★2) Basically, the R×5C338A are configured to cause frequency variations on the order of ±5 to ±10ppm at normal temperature.
★3) Time count precision as referred to in the above flow chart is applicable to normal temperature and actually affected by the temperature characteristics and other properties of crystal oscillators.

Course (A)

When the time count precision of each real-time clock is not to be adjusted, the crystal oscillator intended for use with that real-time clock may have any C_L value requiring no presetting. The crystal oscillator may be subject to frequency variations which are selectable within the allowable range of time count precision. Several crystal oscillators and real-time clocks should be used to find the center frequency of the crystal oscillators by the method described in "2.2 Measurement of Oscillation Frequency" and then calculate an appropriate oscillation adjustment value by the method described in "2.4 Oscillation Adjustment Circuit" for writing this value to the R×5C338A.

Course (B)

When the time count precision of each real-time clock is to be adjusted within the oscillation frequency variations of the crystal oscillator plus the frequency variations of the real-time clock ICs, it becomes necessary to correct deviations in the time count of each real-time clock by the method described in "2.4 Oscillation Adjustment Circuit". Such oscillation adjustment provides crystal oscillators with a wider range of allowable settings of their oscillation frequency variations and their C_L values. The real-time clock IC and the crystal oscillator intended for use with that real-time clock IC should be used to find the center frequency of the crystal oscillator by the method described in "2.2 Measurement of Oscillation Frequency" and then confirm the center frequency thus found to fall within the range adjustable by the oscillation adjustment circuit before adjusting the oscillation frequency of the oscillation circuit. At normal temperature, the oscillation frequency of the oscillator circuit can be adjusted by up to approximately ±1.5ppm.

Course (C)

Course (C) together with Course (D) requires adjusting the time count precision of each real-time clock as well as the frequency of 32.768-kHz clock pulses output from the 32KOUT pin. Normally, the oscillation frequency of the crystal oscillator intended for use with the real-time clocks should be adjusted by adjusting the oscillation stabilizing capacitors C_G and C_D connected to both ends of the crystal oscillator. The R×5C338A, which incorporate the C_G and the C_D, require adjusting the oscillation frequency of the crystal oscillator through its C_L value.

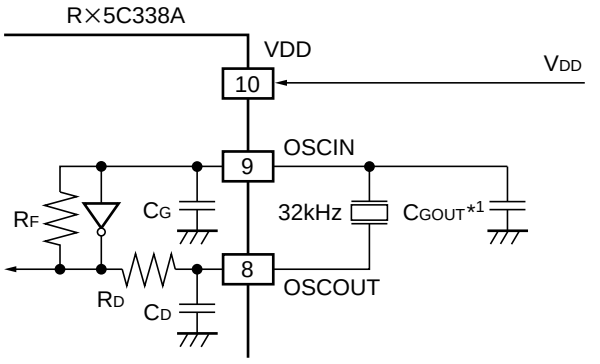
Generally, the relationship between the C_L value and the C_G and C_D values can be represented by the following equation:

$$C_L = \frac{C_G \times C_D}{C_G + C_D} + C_S$$

where "C_S" represents the floating capacity of the printed circuit board

The crystal oscillator intended for use with the R×5C338A is recommended to have the C_L value on the order of 6 to 8pF. Its oscillation frequency should be measured by the method described in "2.2 Measurement of Oscillation Frequency". Any crystal oscillator found to have an excessively high or low oscillation frequency (causing a time count gain or loss, respectively) should be replaced with another one having a smaller and greater C_L value, respectively until another one having an optimum C_L value is selected. In this case, the bit settings disabling the oscillation adjustment circuit (see "2.4 Oscillation Adjustment Circuit") should be written to the oscillation adjustment register.

Another advisable way to select a crystal oscillator having an optimum C_L value is to contact the manufacturer of the crystal oscillator intended for use with the R×5C338A.
Incidentally, the high oscillation frequency of the crystal oscillator can also be adjusted by adding an external oscillation stabilization capacitor C_{GOUT} as illustrated in the diagram below.



*1) The C_{GOUT} should have a capacitance ranging from 0 to 15pF.

Course (D)
It is necessary to select the crystal oscillator in the same manner as in Course (C) as well as correct errors in the time count of each real-time clock in the same manner as in Course (B) by the method described in "2.4 Oscillation Adjustment Circuit".

2.4 Oscillation Adjustment Circuit

The oscillation adjustment circuit can be used to correct a time count gain or loss with high precision by varying the number of 1-second clock pulses once per 20 seconds. When such oscillation adjustment is not to be made, the oscillation adjustment circuit can be disabled by writing the settings of "*, 0, 0, 0, 0, 0, *" ("*" representing "0" or "1") to the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits in the oscillation adjustment circuit. Conversely, when such oscillation adjustment is to be made, an appropriate oscillation adjustment value can be calculated by the equation below for writing to the oscillation adjustment circuit.

2.4-1 When Oscillation Frequency *1 is Higher than Target Frequency *2 (There is a Time Count Gain)

$$\text{Oscillation adjustment value}^{*3} = \frac{(\text{Oscillation frequency} - \text{Target frequency} + 0.1)}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\fallingdotseq (\text{Oscillation frequency} - \text{Target frequency}) \times 10 + 1$$

*1) Oscillation frequency: Frequency of clock pulses output from the 32KOUT pin at normal temperature in the manner described in "2.2 Measurement of Oscillation Frequency".

*2) Target frequency: Desired frequency to be set. Generally, a 32.768-kHz crystal oscillator has such temperature characteristics as to have the highest oscillation frequency at normal temperature. Consequently, the crystal oscillator is recommended to have target frequency settings on the order of 32.768 to 32.76810kHz (+3.05ppm relative to 32.768kHz). Note that the target frequency differs depending on the environment or location where the equipment incorporating the real-time clocks is expected to be operated.

*3) Oscillation adjustment value: Value that is to be finally written to the F_0 to F_6 bits in the oscillation adjustment register and is represented in 7-bit coded decimal notation.

2.4-2 When Oscillation Frequency is Equal to Target Frequency (There is Neither a Time Count Gain nor a Time Count Loss)

Writing the oscillation adjustment value setting of "0", "+1", "–64", or "–63" to the oscillation adjustment register disables the oscillation adjustment circuit.

2.4-3 When Oscillation Frequency is Lower than Target Frequency (There is a Time Count Loss)

$$\text{Oscillation adjustment value}^{*3} = \frac{(\text{Oscillation frequency} - \text{Target frequency})}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\fallingdotseq (\text{Oscillation frequency} - \text{Target frequency}) \times 10$$

Oscillation adjustment value calculations are exemplified below.

(1) For an oscillation frequency of 32768.85Hz and a target frequency of 32768.05Hz:

Oscillation adjustment value = $(32768.85 - 32768.05 + 0.1) / (32768.85 \times 3.051 \times 10^{-6}) \fallingdotseq (32768.85 - 32768.05) \times 10 + 1$

$\fallingdotseq 9.001 = 9$

In this instance, write the settings of "0, 0, 0, 1, 0, 0, 1" to the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits in the oscillation adjustment register. Thus, an appropriate oscillation adjustment value in the presence of any time count gain represents a distance from 01h.

(2) For an oscillation frequency of 32763.95Hz and a target frequency of 32768.05Hz:

Oscillation adjustment value = $(32763.95 - 32768.05) / (32763.95 \times 3.051 \times 10^{-6}) \fallingdotseq (32763.95 - 32768.05) \times 10$

$= -41.015 \fallingdotseq -41$

To represent an oscillation adjustment value of –41 in 7-bit coded decimal notation, subtract 41(29h) from 128(80h) to obtain 57h. In this instance, write the settings of "1, 0, 1, 0, 1, 1, 1" in the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits in the oscillation adjustment register. Thus, an appropriate oscillation adjustment value in the presence of any time count loss represents a distance from 80h.

Oscillation adjustment involves an adjustment differential of approximately ±1.5ppm from the target frequency at normal temperature.

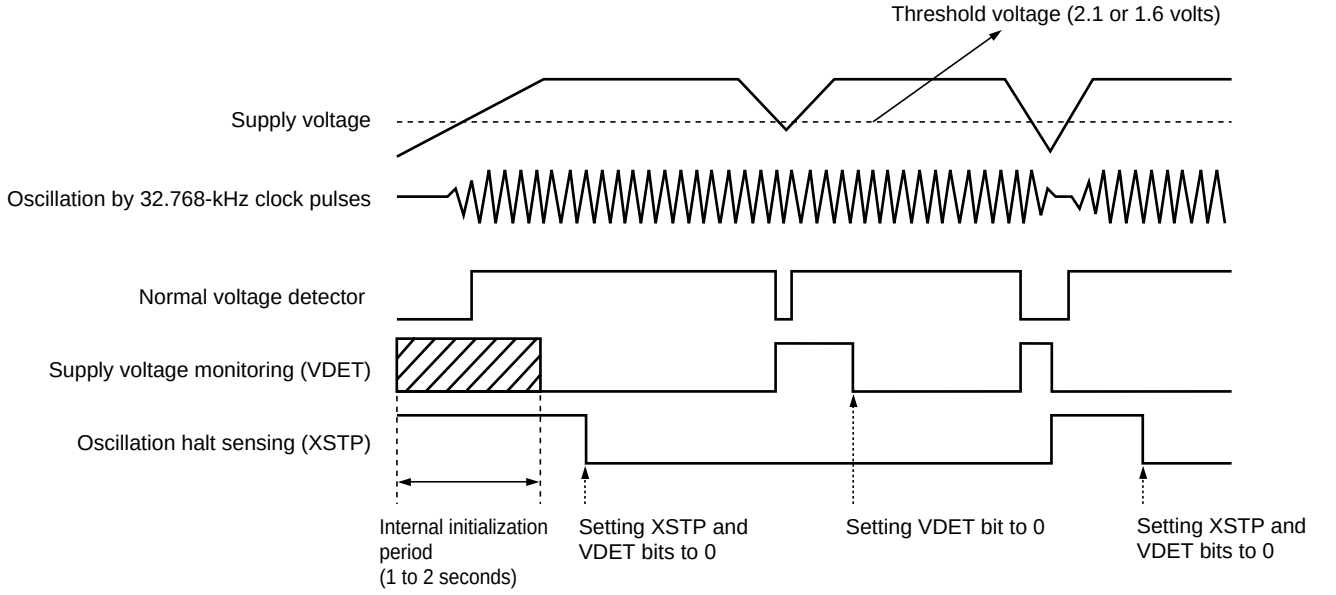
Notes

1) Oscillation adjustment does not affect the frequency of 32.768-kHz clock pulses output from the 32KOUT pin.
2) Oscillation adjustment value range: When the oscillation frequency is higher than the target frequency (causing a time count gain), an appropriate time count gain ranges from –3.05ppm to –189.2ppm with the settings of "0, 0, 0, 0, 0, 1, 0" to "0, 1, 1, 1, 1, 1, 1" written to the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits in the oscillation adjustment register, thus allowing correction of a time count gain of up to +189.2ppm.
   Conversely, when the oscillation frequency is lower than the target frequency (causing a time count loss), an appropriate time count gain ranges from +3.05ppm to +189.2ppm with the settings of "1, 1, 1, 1, 1, 1, 1" to "1, 0, 0, 0, 0, 1, 0" written to the F_6, F_5, F_4, F_3, F_2, F_1, and F_0 bits in the oscillation adjustment register, thus allowing correction of a time count loss of up to –189.2ppm.

3. Oscillation Halt Sensing and Supply Voltage Monitoring

The oscillation halt sensing circuit is configured to record a halt in the oscillation of 32.768-kHz clock pulses. The supply voltage monitoring circuit is configured to record a drop in supply voltage below a threshold voltage of 2.1 or 1.6 volts. For these functions, the real-time clock has two flag bits (i.e. the XSTP bit for the former and the VDET bit for the latter) in which 1 is set once and this setting is maintained until 0 is written.
When the XSTP bit is set to 1 for the oscillation halt sensing circuit, the VDET bit is reset to 0 for the supply voltage monitoring circuit. The relationship between the XSTP and VDET bits is shown in the table below.
The Oscillation halt sensing circuit operates only when the CE pin is Low. The sensing result is maintained after the CE pin changes from "L" to "H" (See "6.4 Connection of CE Pin").

XSTP	VDET	Conditions of supply voltage and oscillation
0	0	No drop in supply voltage below threshold voltage and no halt in oscillation
0	1	Drop in supply voltage below threshold voltage and no halt in oscillation
1	*	Halt on oscillation



When the XSTP bit is set to 1 in the control register 2, the (0), F6 to F0, WALE, DALE, $\overline{12}$/24, $\overline{CLEN2}$, TEST, CT2, CT1, CT0, VDSL, VDET, SCRATCH, $\overline{CLEN1}$, CTFG, WAFG, and DAFG bits are reset to 0 in the oscillation adjustment register, the control register 1, and the control register 2. When the CE pin is "H" at power on from 0 volts, the XSTP bit is undefined, and the above bits are undefined (See "6.4 Connection of CE Pin"). The XSTP bit is also set to 1 at power-on from 0 volts. Note that the XSTP bit may be locked to 0 and the internal register broken upon instantaneous power-down.

Considerations in Using Oscillation Halt Sensing Circuit

Be sure to prevent the oscillation halt sensing circuit from malfunctioning by preventing the following:

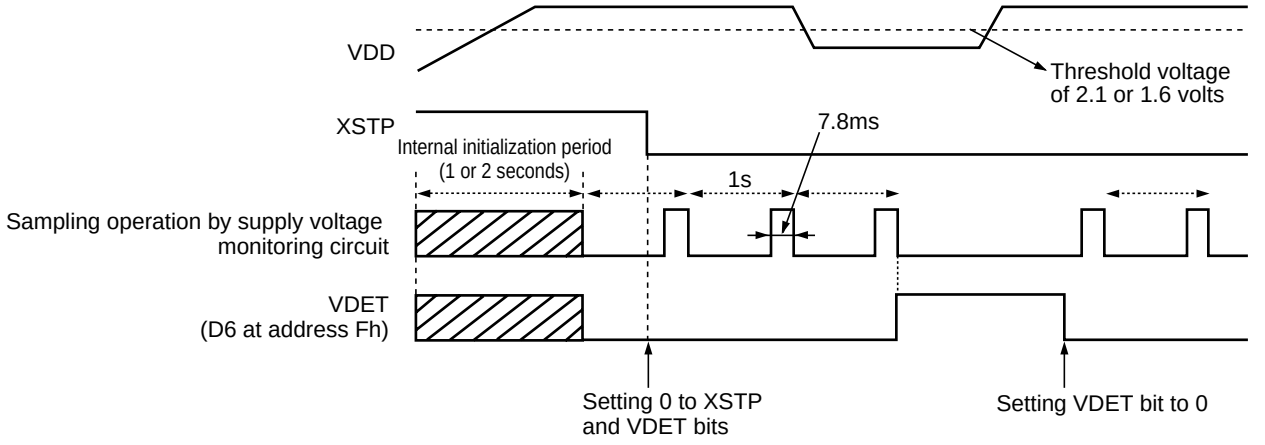
1) Instantaneous power-down on the V_{DD}
2) Condensation on the crystal oscillator
3) On-board noise to the crystal oscillator
4) Applying to individual pins voltage exceeding their respective maximum ratings

In particular, note that the XSTP bit may fail to be set to 1 in the presence of any applied supply voltage as illustrated below in such events as backup battery installation. Further, give special considerations to prevent excessive chattering to power supply.



< Supply Voltage Sensing Circuit >

The supply voltage monitoring circuit is configured to conduct a sampling operation during an interval of 7.8ms per second to check for a drop in supply voltage below a threshold voltage of 2.1 or 1.6 volts for the VDSL bit setting of 0 (the default setting) or 1, respectively, in the control register 2, thus minimizing supply current requirements as illustrated in the timing chart below. This circuit suspends a sampling operation once the VDET bit is set to 1 in the control register 2.



<Precautions for Using Voltage Monitoring Circuit>

After writing to the second counter, reset a VDET flag (writing 0) once for defining a value of VDET flag.

4. Alarm and Periodic Interrupt

The R×5C338A incorporate the alarm circuit and the periodic interrupt circuit that are configured to generate alarm signals and periodic interrupt signals, respectively, for output from the $\overline{\text{INTR}}$ pin as described below.

1) Alarm Circuit

The alarm interrupt circuit is configured to generate alarm signals for output from the $\overline{\text{INTR}}$, which is driven low (enabled) upon the occurrence of a match between current time read by the time counters (the day-of-week, hour, and minute counters) and alarm time preset by the alarm registers (the Alarm_W registers intended for the day-of-week, hour, and minute digit settings and the Alarm_D registers intended for the hour and minute digit settings).

2) Periodic Interrupt Circuit

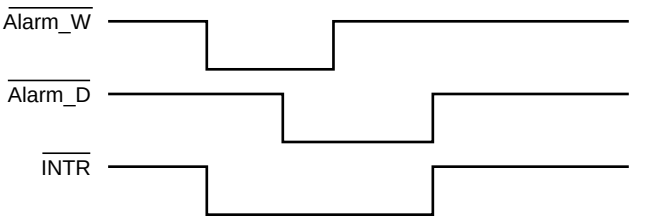
The periodic interrupt circuit is configured to generate either clock pulses in the pulse mode or interrupt signals in the level mode for output from the $\overline{\text{INTR}}$ pin depending on the CT_2, CT_1, and CT_0 bit settings in the control register 1.

The above two types of interrupt signals are monitored by the flag bits (i.e. the WAFG, DAFG, and CTFG bits in the control register 2) and enabled or disabled by the enable bits (i.e. the WALE, DALE, CT_2, CT_1, and CT_0 bits in the control register 1) as listed in the table below.

	Flag bits	Enable bits
Alarm signals (under control of Alarm_W registers)	WAFG bit (D1 at Address Fh)	WALE bit (D7 at Address Eh)
Alarm signals (under control of Alarm_D registers)	DAFG bit (D0 at Address Fh)	DALE bit (D6 at Address Eh)
Periodic interrupt signals	CTFG bit (D2 at Address Fh)	CT_2, CT_1, and CT_0 bits (D2 to D0 at Address Eh) (these bit settings of 0 disable the periodic interrupt circuit)

- At power-on, when the WALE, DALE, CT_2, CT_1, and CT_0 bits are set to 0 in the control register 1, the $\overline{\text{INTR}}$ pin is driven high (disabled).
- When two or more types of interrupt signals are output simultaneously from the $\overline{\text{INTR}}$ pin, the output from the $\overline{\text{INTR}}$ pin becomes an OR waveform of their negative logic.

Example: Combined Output of Alarm Interrupt Signals from the $\overline{\text{INTR}}$ pin Under Control of $\overline{\text{Alarm_D}}$ and $\overline{\text{Alarm_W}}$ Registers

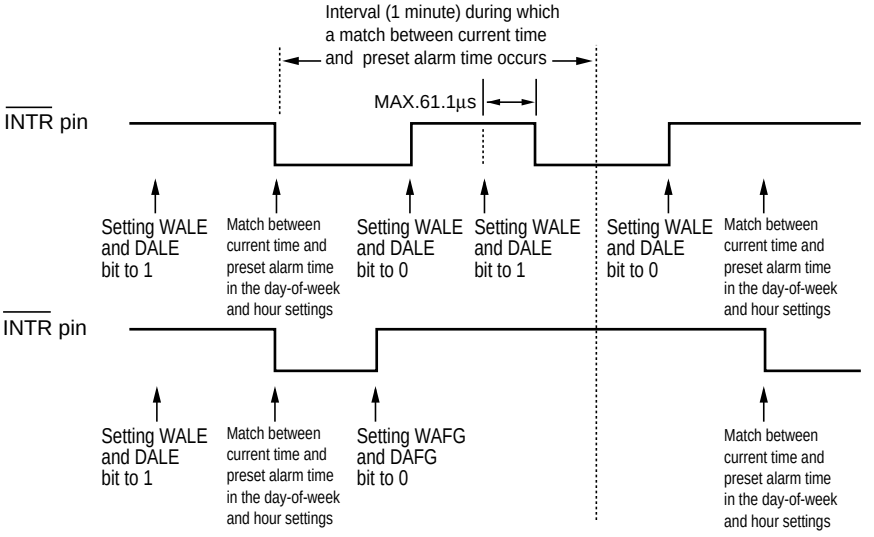


In this event, which type of interrupt signal is output from the $\overline{\text{INTR}}$ pin can be confirmed by reading the WAFG, DAFG, and CTFG bit settings in the control register 2.

4.1 Alarm Interrupt

The alarm circuit is controlled by the enable bits (i.e. the WALE and DALE bits in the control register 1) and the flag bits (i.e. the WAFG and DAFG bits in the control register 2). The enable bits can be used to enable this circuit when set to 1 and to disable it when set to 0. When intended for reading, the flag bits can be used to monitor alarm interrupt signals. When intended for writing, the flag bits will cause no event when set to 1 and will drive high (disable) the alarm circuit when set to 0.
The enable bits will not be affected even when the flag bits are set to 0. In this event, therefore, the alarm circuit will continue to function until it is driven low (enabled) upon the next occurrence of a match between current time and preset alarm time.

The alarm function can be set by presetting desired alarm time in the alarm registers (the Alarm_W registers for the day-of-week digit settings and both the Alarm_W registers and the Alarm_D registers for the hour and minute digit settings) with the WALE and DALE bits once set to 0 and then to 1 in the control register 1. Note that the WALE and DALE bits should be once set to 0 in order to disable the alarm circuit upon the coincidental occurrence of a match between current time and preset alarm time in the process of setting the alarm function.



4.2 Periodic Interrupt

Setting of the periodic selection bits (CT_2 to CT_0) enables periodic interrupt to the CPU. There are two waveform modes: pulse mode and level mode. In the pulse mode, the output has a waveform duty cycle of around 50%. In the level mode, the output is cyclically driven low and, when the CTFG bit is set to 0, the output is set to high (OFF).

Waveform Mode, Cycle and Falling Timing

CT_2	CT_1	CT_0	Description		
			Waveform mode	Cycle and falling timing	
0	0	0	—	Off ("H")	(Default setting)
0	0	1	—	Fixed at low ("L")	
0	1	0	Pulse Mode*1	2Hz (Duty cycle of 50%)	
0	1	1	Pulse Mode*1	1Hz (Duty cycle of 50%)	
1	0	0	Level Mode*2	Once per 1 second (Synchronized with second counter increment)	
1	0	1	Level Mode*2	Once per minute (at 00 seconds of every minute)	
1	1	0	Level Mode*2	Once per hour (at 00 minutes and 00 seconds of every hour)	
1	1	1	Level Mode*2	Once per month (at 00 hours, 00 minutes, and 00 seconds of first day of every month)	

1) Pulse Mode : 2-Hz and 1-Hz clock pulses are output in synchronization with the increment of the second counter as illustrated in the timing chart on the next page.

2) Level Mode : periodic interrupt signals are output with selectable interrupt cycle settings of 1 second, 1 minute, 1 hour, and 1 month. The increment of the second counter is synchronized with the falling edge of periodic interrupt signals. For example, periodic interrupt signals with an interrupt cycle setting of 1 second are output in synchronization with the increment of the second counter as illustrated in the timing chart on the next page.

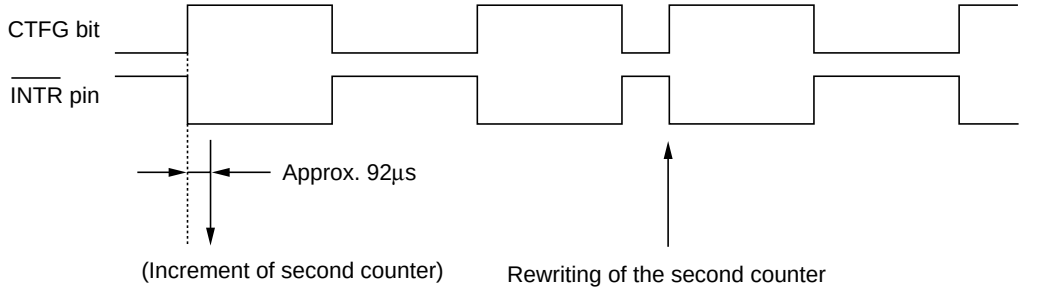
3) When the oscillation adjustment circuit is used, the interrupt cycle will fluctuate once per 20 seconds as follows:

Pulse Mode : the "L" period of output pulses will increment or decrement by a maximum of ±3.784ms.
For example, 1-Hz clock pulses will have a duty cycle of 50 ±0.3784%.

Level Mode : a periodic interrupt cycle of 1 second will increment or decrement by a maximum of ±3.784ms.

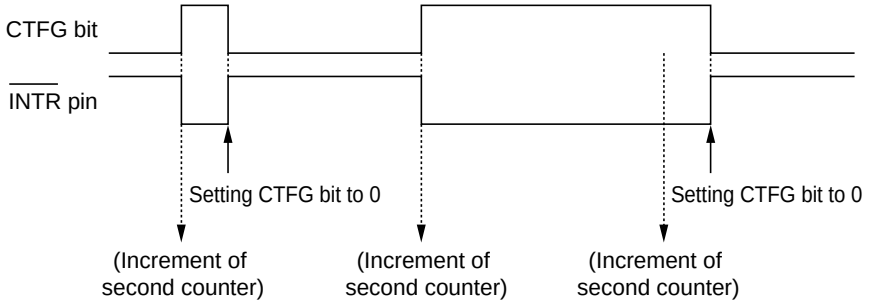
Relation Between the Mode Waveform and the CTFG Bit

• Pulse mode



*) In the pulse mode, the increment of the second counter is delayed by approximately 92 µs from the falling edge of clock pulses. Consequently, time readings immediately after the falling edge of clock pulses may appear to lag behind the time counts of the real-time clocks by approximately 1 second. Rewriting the second counter will reset the other time counters of less than 1 second, driving the INTR pin low.

• Level mode

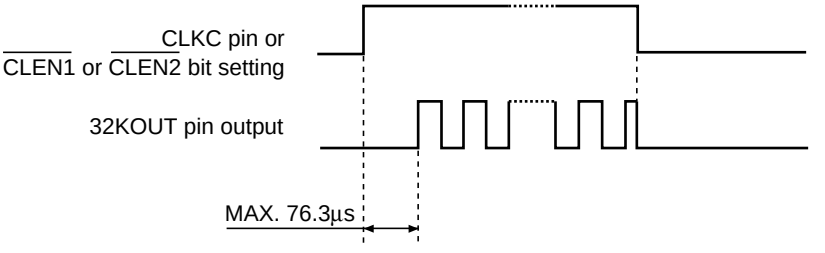


5. 32-kHz Clock Output

32.768-kHz clock pulses are output from the 32KOUT pin when either the CLEN1 bit in the control register 2 or the CLEN2 bit in the control register 1 is set to 0 when the CLKC pin is set to high. If the conditions described above are not satisfied, the output is set to high.

CLEN1 (D3 at Address Fh)	CLEN2 (D4 at Address Eh)	CLKC pin output	32KOUT pin output (CMOS output)
1	1	*	"L"
*	*	0	
0 (Default)	*	1	Clock pulses
*	0 (Default)	1	

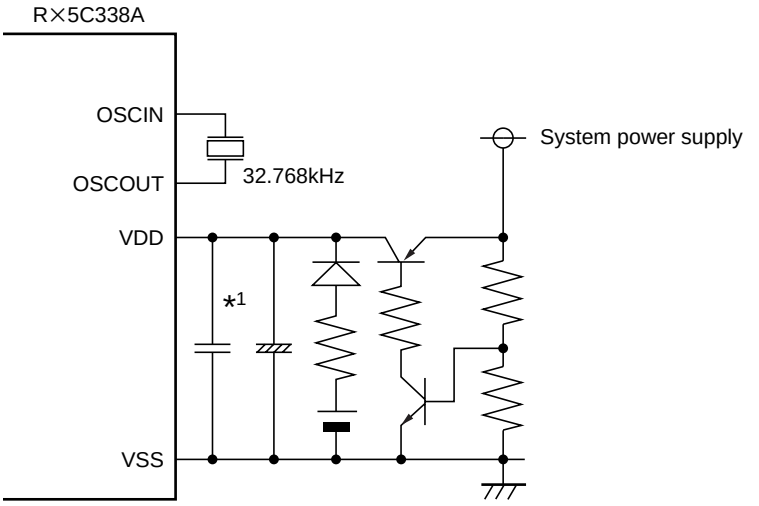
The 32KOUT pin output is synchronized with the CLEN1, CLEN2 bit, and CLKC pin settings as illustrated in the timing chart below.



6. Typical Applications

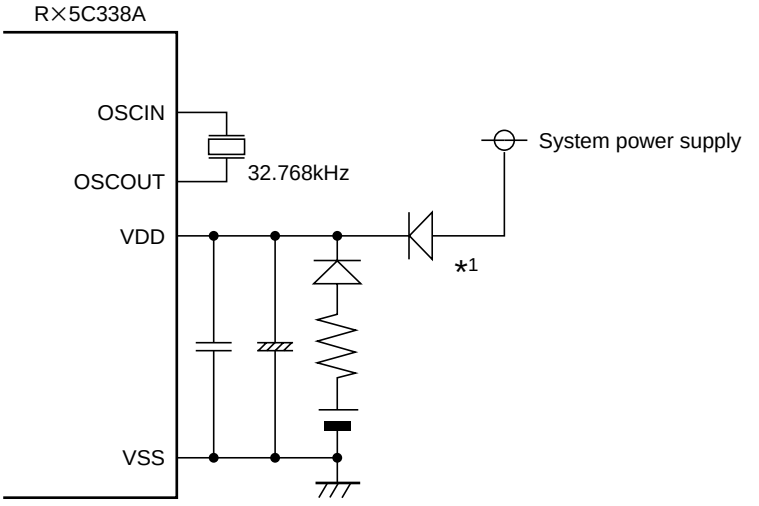
6.1 Typical Power Circuit Configurations

Sample circuit configuration 1



*1) Install bypass capacitors for high-frequency and low-frequency applications in parallel in close vicinity to the R×5C338A.

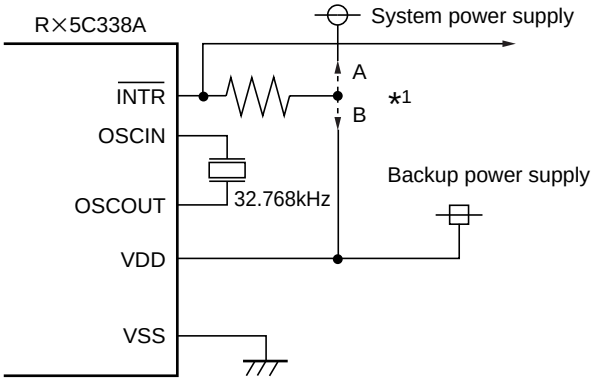
Sample circuit configuration 2



*1) When using an OR diode as a power supply for the R×5C338A , ensure that voltage exceeding the absolute maximum rating of V_{DD}+0.3 volts is not applied the SO and 32KOUT pins.

6.2 Connection of $\overline{\text{INTR}}$ Pin

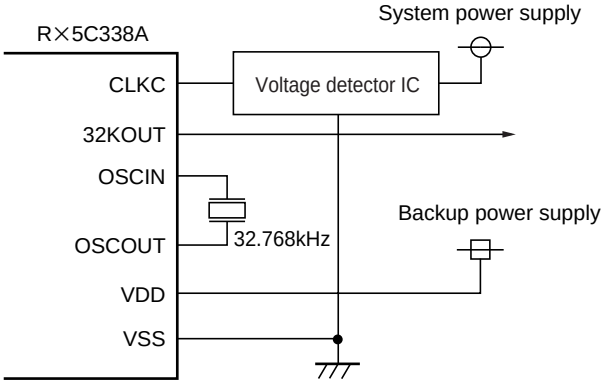
The $\overline{\text{INTR}}$ pin follows the N-channel open drain output logic and contains no protective diode on the power supply side. As such, it can be connected to a pull-up resistor of up to 5.5 volts regardless of supply voltage.

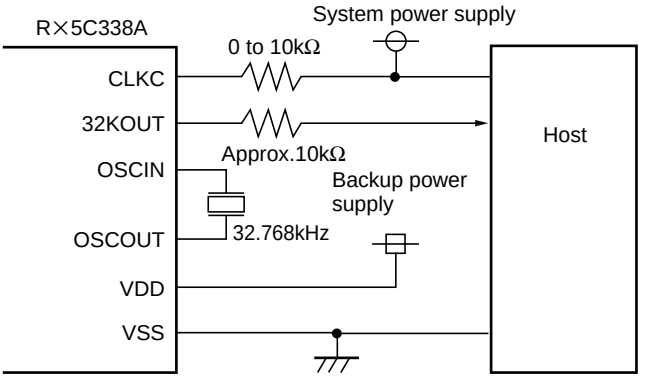


*1) Depending on whether the $\overline{\text{INTR}}$ pin is to be used during battery backup, it should be connected to a pull-up resistor at the following different positions:
1) Position A in the left diagram when it is not to be used during battery backup.
2) Position B in the left diagram when it is to be used during battery backup.

6.3 Connection of 32KOUT Pin

As the 32KOUT pin is CMOS output, the voltages of the R×5C338A and any devices to be connected should be the same. When the device is powered down, the 32KOUT output should be disabled.
When the CLKC pin is connected to the system power supply through the pull-up resistor, the pull-up resistor should be 0Ω to 10kΩ, and the 32KOUT pin should be connect to the host through the resistor (approx. 10kΩ).

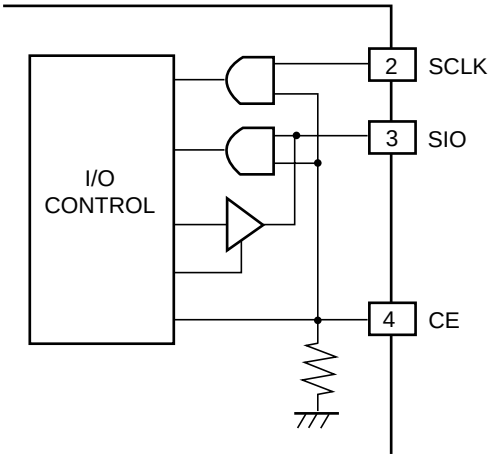


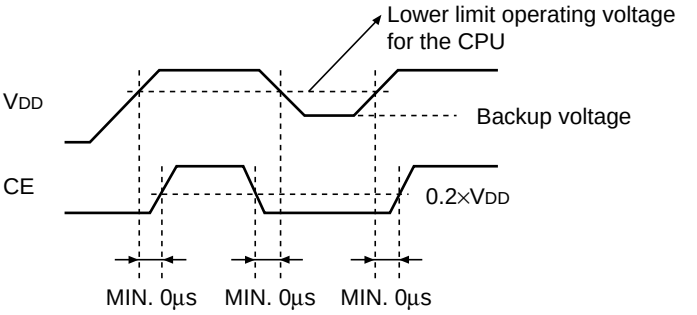


6.4 Connection of CE Pin

Observe the following precautions when you connect the CE pin.

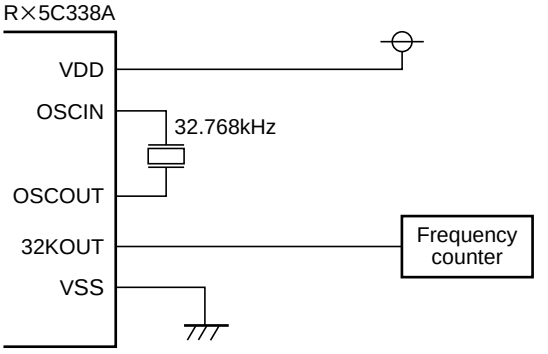
1) The CE pin is configured to enable the oscillation halt sensing circuit only when driven low. As such, it should be driven low or open at power-on from 0 volts.
2) The CE pin should also be driven low or open immediately upon the host going down (see "1.5 Considerations in Reading and Writing Time Count Data").
3) The reading function should be disrupted when the CE signal goes to "low" during read cycle. While, the upper 4 bits of the data might be written to the inner shift register when the CE signal goes to "low" during write cycle. (Because the writing function is executed 4 bits by 4 bits.) In either case, after the CE signal returns to "High", no trouble will occur in the next read or write cycle.





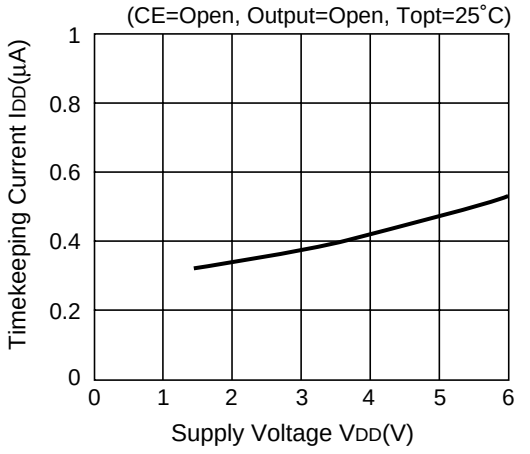
7. Typical Characteristics

• Test Circuit

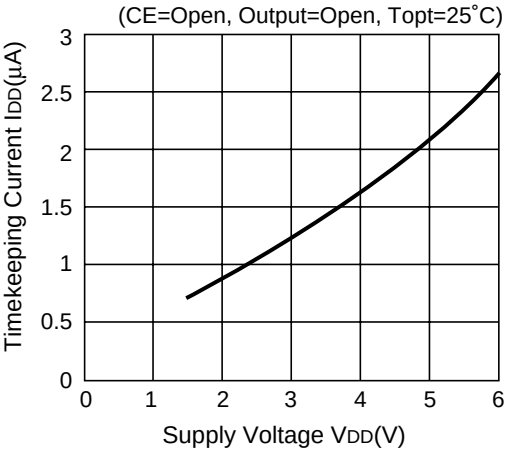


X'tal : 32.768kHz
(R_1=30kΩ TYP.)
(C_L=6pF to 8pF)
Topt : 25°C
Output pins : Open

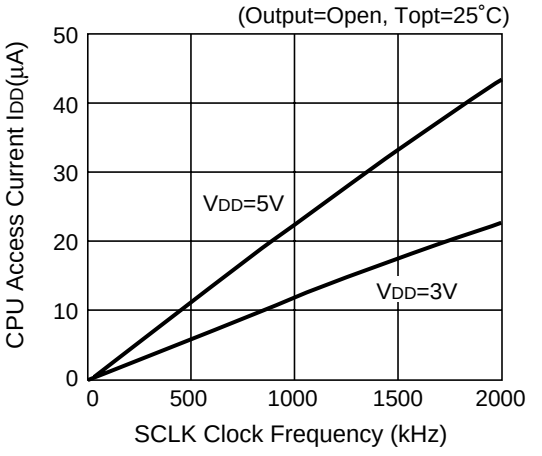
7.1 Timekeeping Current vs. Supply Voltage (with no 32-kHz clock output)



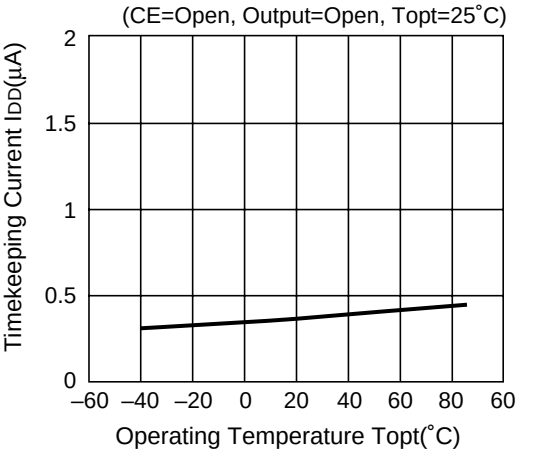
7.2 Timekeeping Current vs. Supply Voltage (with 32-kHz clock output)



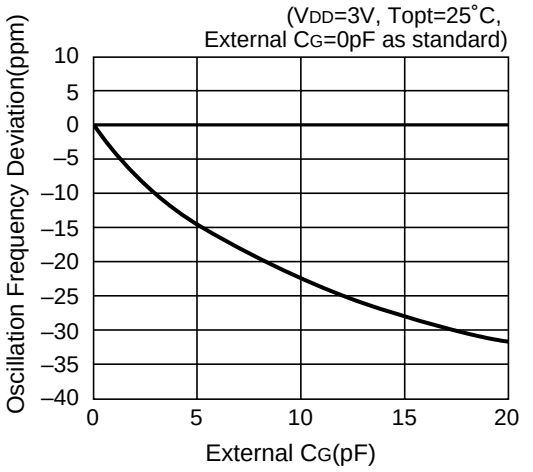
7.3 CPU Access Current vs. SCLK Clock Frequency



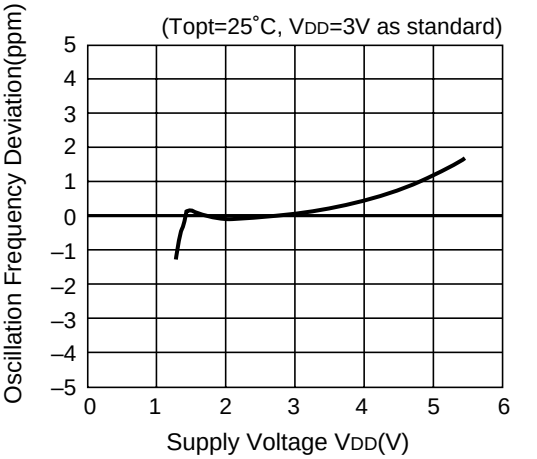
7.4 Timekeeping Current vs. Operating Temperature (with no 32-kHz clock output)



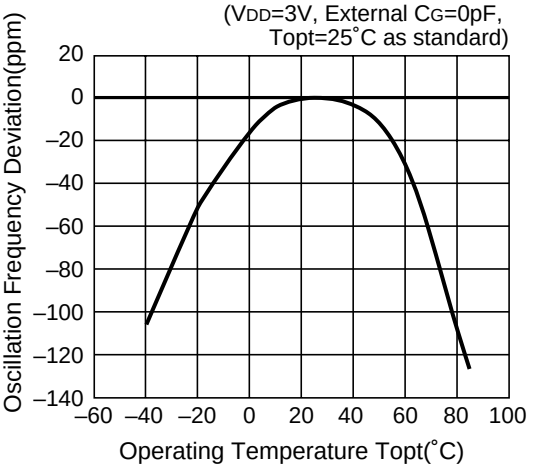
7.5 Oscillation Frequency Deviation vs. External C_G



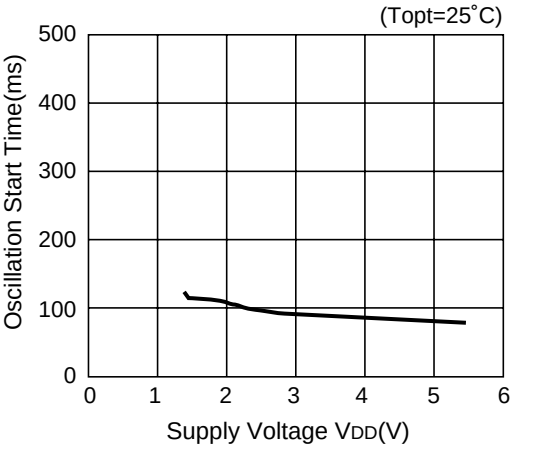
7.6 Oscillation Frequency Deviation vs. Supply Voltage



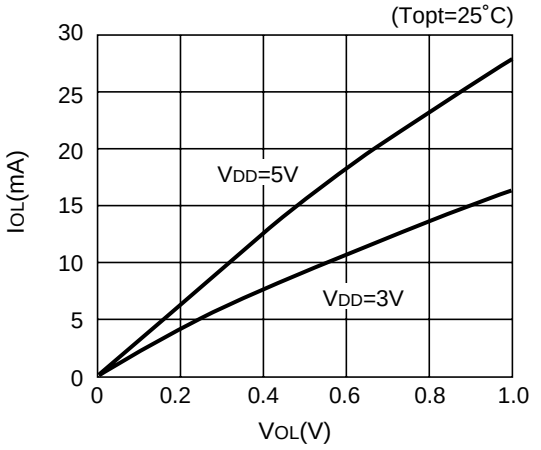
7.7 Oscillation Frequency Deviation vs. Operating Temperature



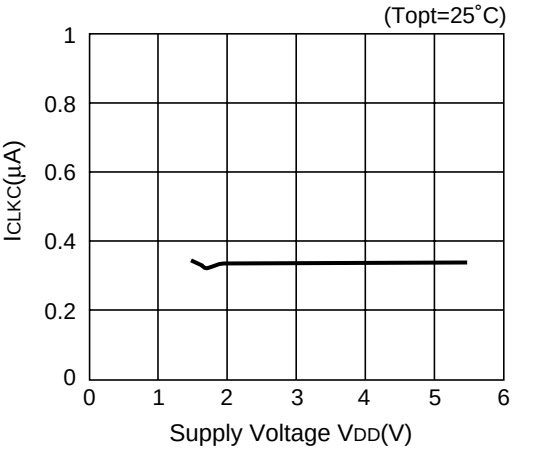
7.8 Oscillation Start Time vs. Supply Voltage



7.9 V_{OL} vs. I_{OL} ($\overline{\text{INTR}}$ Pin)

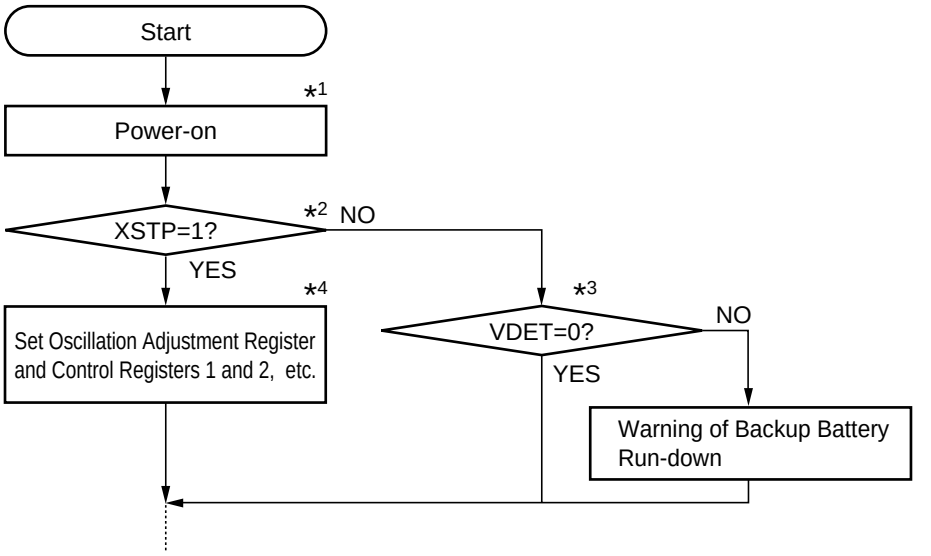


7.10 Input Current to CLKC Pin vs. Supply Voltage



8. Typical Software-based Operations

8.1 Initialization at Power-on



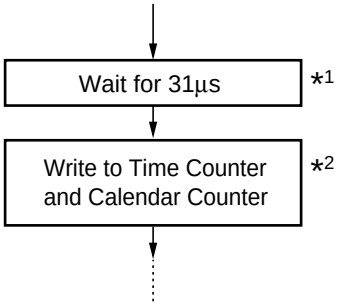
*1) After power-on from 0 volts, the start of oscillation and the process of internal initialization require a time span on the order of 1 to 2 seconds, so that access should be done after the lapse of this time span or more.

*2) The XSTP bit setting of 0 in the control register 1 indicates power-on from backup battery and not from 0 volt. The XSTP bit may fail to be set to 1 in the presence of any excessive chattering in power supply in such events as installing backup battery. Should there be any possibility of this failure occurring, it is recommended to initialize the R×5C338A regardless of the current XSTP bit setting. For further details, see "3. Oscillation Halt Sensing and Supply Voltage Monitoring".

*3) This step is not required when the supply voltage monitoring circuit is not used.
When using this circuit, note as follows.
After writing to the second counter, reset a VDET flag (writing 0) once for defining a value of VDET flag.

*4) This step involves ordinary initialization including the oscillation adjustment register and interrupt cycle settings.

8.2 Writing of Time and Calendar Data

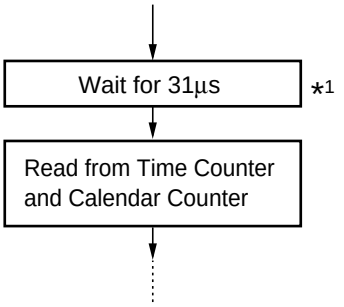


*1) This step of waiting is detailed in "1.5 Considerations in Reading and Writing Time Data".

*2) Any writing to the second counter will reset divider units lower than the second digits.
After writing to the second counter, reset a VDET flag (writing 0) once for defining a value of VDET flag.

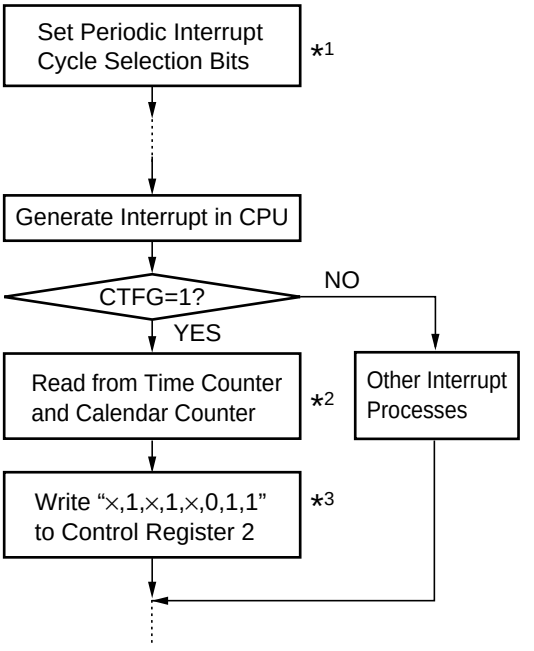
8.3 Reading Time and Calendar Data

8.3-1 Ordinary Process of Reading Time and Calendar Data



*1) This step of waiting is detailed in “1.5 Considerations in Reading and Writing Time Data”.

8.3-2 Basic Process of Reading Time and Calendar Data Synchronized with Periodic Interrupt



*1) This step is intended to select the level mode as a waveform mode for the periodic interrupt function.

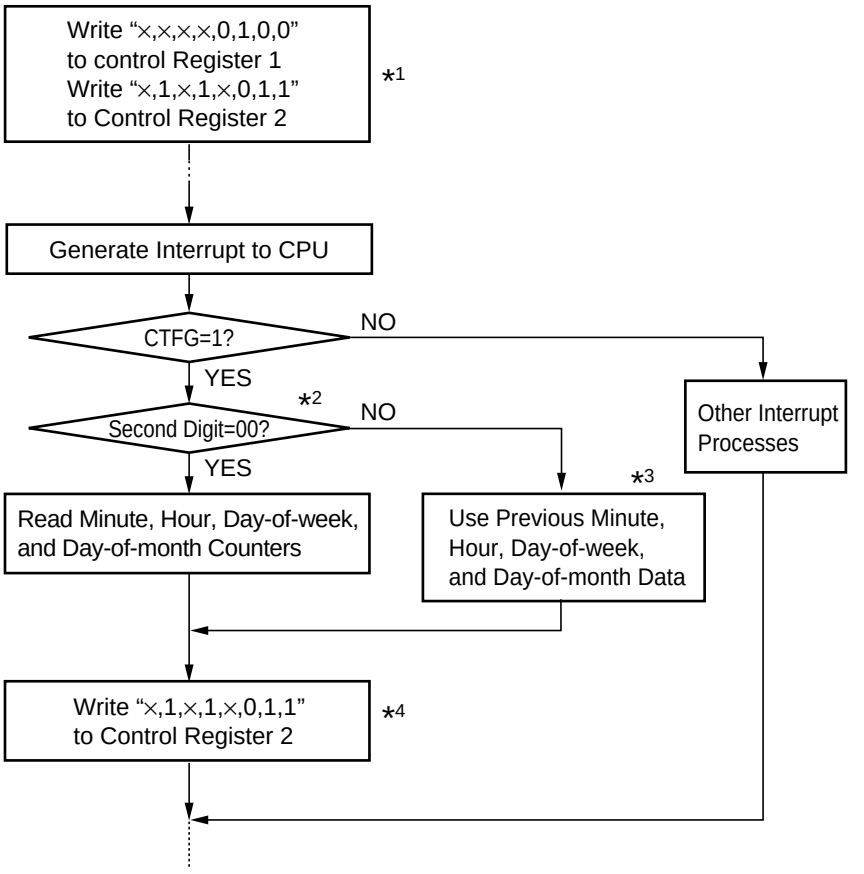
*2) If this step is completed within 1 second, the step of waiting described in “8.3-1 Ordinary Process of Reading Time and Calendar Data” above need not be conducted. This step is detailed in “1.5 Considerations in Reading and Writing Time Data”.

*3) This step is intended to set the CTFG bit to 0 in the control register 2 to cancel an interrupt to the CPU.

8.3-3 Applied Process of Reading Time and Calendar Data Synchronized with Periodic Interrupt Function

Time data need not be read from all the time counters when used for such ordinary purposes as time count indication. This applied process can be used to read time and calendar data with substantial reductions in the load involved in such reading.

For Time Indication in "Day-of-month, Day-of-week, Hour, Minute, and Second" Format:



*1) This step is intended to select the level mode as a waveform mode for the periodic interrupt function.

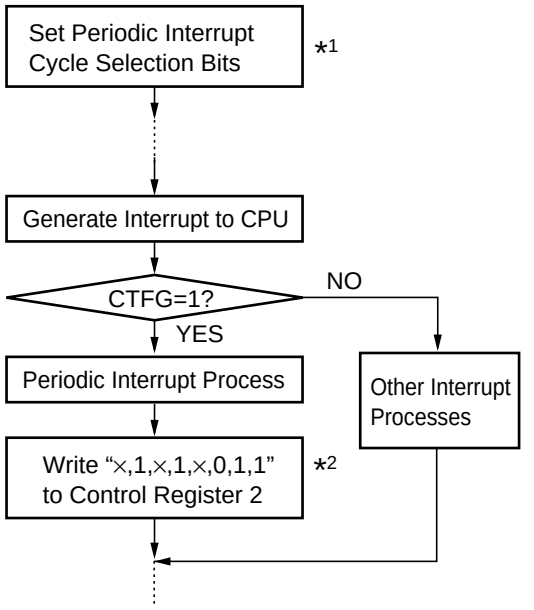
*2) If this step is completed within 1 second, the step of waiting described in "8.3-1 Ordinary Process of Reading Time and Calendar Data" above need not be conducted. This step is detailed in "1.5 Considerations in Reading and Writing Time Data".

*3) This step is intended to read time data from all the time counters only in the first session of reading time data after writing time data.

*4) This step is intended to set the CTFG bit to 0 in the control register 2 to cancel an interrupt to the CPU.

8.4 Interrupt Process

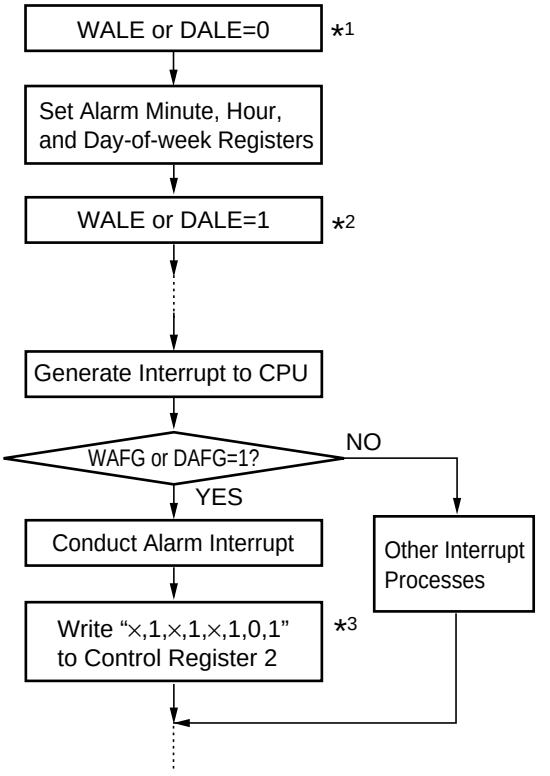
8.4-1 Periodic Interrupt



*1) This step is intended to select the level mode as a waveform mode for the periodic interrupt function.

*2) This step is intended to set the CTFG bit to 0 in the control register 2 to cancel an interrupt to the CPU.

8.4-2 Alarm Interrupt



*1) This step is intended to once disable the alarm interrupt circuit by setting the WALE and DALE bits to 0 in anticipation of the coincidental occurrence of a match between current time and preset alarm time in the process of setting the alarm interrupt function.

*2) This step is intended to enable the alarm interrupt function after completion of all alarm interrupt settings.

*3) This step is intended to once cancel the alarm interrupt function by writing the settings of "×,1,×,1,×,1,0,1" and "×,1,×,1,×,1,1,0" to the Alarm_W registers and the Alarm_D registers, respectively.

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