



*ConnectCore™ 9P 9215, Wi-9P  
9215, and 3G 9P 9215*

*Hardware Reference*

90000879\_R

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# Using this Guide

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This guide provides information about the Digi ConnectCore 9P 9215 Family of embedded core modules.

## Conventions used in this guide

This table describes the typographic conventions used in this guide:

| This convention    | Is used for                                          |
|--------------------|------------------------------------------------------|
| <i>italic type</i> | Emphasis, new terms, variables, and document titles. |
| monospaced type    | Filenames, pathnames, and code examples.             |

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# About the Module

## C H A P T E R 1

The ConnectCore 9P 9215 Family of modules delivers powerful network-enabled core processor solutions with up to 16 MB of NOR flash, up to 32 MB SDRAM, a rich set of integrated peripherals, and superior design flexibility.

At the heart of the modules is a Digi 32-bit ARM9-based Digi NS9215 processor running at 150 MHz. Key features include 10/100 Mbit Ethernet, two on-chip Flexible Interface Modules (FIMs), 256-bit AES accelerator, power management modes with dynamic clock scaling, and a rich set of on-chip peripherals. Based on Digi 802.11 baseband technology, the ConnectCore Wi-9P 9215 also provides an additional 802.11a/b/g interface with enterprise-grade WPA2/802.11i support.

The ConnectCore 3G 9P 9215 module allows you to instantly add intelligent cellular communication to your products.

Built on leading Qualcomm Gobi 3000 technology, the module delivers a pre-certified embedded cellular connectivity solution without the traditional carrier/network limitations. Selecting cellular network technology and carriers is now a matter of software configuration and service provisioning, any time.

The unique FIMs on the Digi NS9215 processor are two independent 300 MHz DRP165X processor cores that allow customers to dynamically select application-specific interfaces in software. The growing list of supported interfaces includes UART, SD/SDIO, CAN bus, USB-device low-speed, 1-Wire®, USB device low-speed, parallel bus interface, and others.

Utilizing the Digi NET+™ ARM processor and secure 802.11a/b/g WLAN technology, the family of ConnectCore 9P 9215 modules offers the industry's only network-enabled core module with true long-term product availability to meet the extended life cycle requirements of embedded product designs.

For further information about the Digi NS9215, see the Digi NS9215 Hardware Reference Manual.

### About the Software

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The ConnectCore 9P 9215 Family of modules comes in distinct flavors of software: Embedded Development Firmware; or the Digi Plug-and-Play Firmware (ConnectCore Wi-9P 9215 only.)

The Embedded Development Firmware is used for the NET+OS<sup>®</sup> or Digi Embedded Linux Development systems. These modules require a developer to load system software, compile and debug their applications using the Digi ESP<sup>™</sup> Development Environment. In this environment, applications are developed in ANSI C and use the various libraries and services to create custom applications, with resolution down to the device driver.

In the Digi Plug-and-Play Firmware, the firmware is fixed. These modules require either some minor configuration or the loading and launching of Python applications that alter the general behavior of the system. In this environment, fast turn around and minimal development should be expected, however, the level of customization is limited to the Python API and/or the configuration methods.

The information within this chapter is broken down into two sections based on software type. For embedded NET+OS or Digi Embedded Linux users see page 14; for Digi Plug-and-Play Firmware users see page 41.

# Digi Embedded Linux and NET+OS

This section describes the features and functionality of modules utilizing embedded NET+OS or Digi Embedded Linux Development Environments only. If you are using a module that utilizes Digi Plug-and-Play Firmware see page 41.

Once you have read through all of the embedded NET+OS / Digi Embedded Linux related sections, proceed to Chapter 2.

## Module pinout

The module has two 80 pin connectors, X1 and X2. The following tables describe each pin, its properties, and its use on the Development Board.

### Pinout legend: Type

- I      Input
- O      Output
- I/O    Input or output
- P      Power

### X1 pinout

| X1 pin number | Type | Module Functionality | Comments                                                                          |
|---------------|------|----------------------|-----------------------------------------------------------------------------------|
| 1             | P    | GND                  |                                                                                   |
| 2             | P    | GND                  |                                                                                   |
| 3             | I    | RSTIN#               | 10k pull-up on module                                                             |
| 4             | O    | SRESET#              | Output of the reset controller<br>push pull with 470R current limiting resistor   |
| 5             | O    | RSTOUT#              | Output of logical AND function between NS9215<br>RESET_DONE and NS9215 RESET_OUT# |
| 6             | I    | TCK                  | JTAG - 10k pull-up on module                                                      |
| 7             | I    | TMS                  | JTAG - 10k pull-up on module                                                      |
| 8             | I    | TDI                  | JTAG - 10k pull-up on module                                                      |
| 9             | O    | TDO                  | JTAG - 10k pull-up on module                                                      |
| 10            | I    | TRST#                | JTAG - 2k2 pull-down on module                                                    |
| 11            | O    | RTCK                 | JTAG - Optional                                                                   |
| 12            | I    | OCD_EN#              | 10k pull-up on module                                                             |
| 13            | I    | LITTLE# / BIG ENDIAN | 2k2 series resistor on module                                                     |

| X1 pin number | Type | Module Functionality | Comments                                                                          |
|---------------|------|----------------------|-----------------------------------------------------------------------------------|
| 14            | I    | WLAN_DISABLE#        | Normally connected to X2-15                                                       |
| 15            | I    | SW_CONF0             | 2k2 series resistor on module                                                     |
| 16            | I    | SW_CONF1             | 2k2 series resistor on module                                                     |
| 17            | I    | SW_CONF2             | 2k2 series resistor on module                                                     |
| 18            | I    | SW_CONF3             | 2k2 series resistor on module                                                     |
| 19            | O    | LED_WWAN#            | Reserved                                                                          |
| 20            | P    | GND                  |                                                                                   |
| 21            | I/O  | BD0                  | Buffered Data - only active when either CS0# or CS2# is active<br>NS9215 D[31:16] |
| 22            | I/O  | BD1                  |                                                                                   |
| 23            | I/O  | BD2                  |                                                                                   |
| 24            | I/O  | BD3                  |                                                                                   |
| 25            | I/O  | BD4                  |                                                                                   |
| 26            | I/O  | BD5                  |                                                                                   |
| 27            | I/O  | BD6                  |                                                                                   |
| 28            | I/O  | BD7                  |                                                                                   |
| 29            | I/O  | BD8                  |                                                                                   |
| 30            | I/O  | BD9                  |                                                                                   |
| 31            | I/O  | BD10                 |                                                                                   |
| 32            | I/O  | BD11                 |                                                                                   |
| 33            | I/O  | BD12                 |                                                                                   |
| 34            | I/O  | BD13                 |                                                                                   |
| 35            | I/O  | BD14                 |                                                                                   |
| 36            | I/O  | BD15                 |                                                                                   |
| 37            | P    | GND                  |                                                                                   |
| 38            | O    | BA0                  | Buffered Address always active                                                    |
| 39            | O    | BA1                  |                                                                                   |
| 40            | O    | BA2                  |                                                                                   |
| 41            | O    | BA3                  |                                                                                   |
| 42            | O    | BA4                  |                                                                                   |
| 43            | O    | BA5                  |                                                                                   |
| 44            | O    | BA6                  |                                                                                   |
| 45            | O    | BA7                  |                                                                                   |

| X1 pin number | Type | Module Functionality | Comments                                             |
|---------------|------|----------------------|------------------------------------------------------|
| 46            | O    | BA8                  |                                                      |
| 47            | O    | BA9                  |                                                      |
| 48            | O    | BA10                 |                                                      |
| 49            | O    | BA11                 |                                                      |
| 50            | O    | BA12                 |                                                      |
| 51            | O    | BA13                 |                                                      |
| 52            | O    | BA14                 |                                                      |
| 53            | O    | BA15                 |                                                      |
| 54            | O    | BA16                 |                                                      |
| 55            | O    | GND                  |                                                      |
| 56            | O    | EXT_OE#              |                                                      |
| 57            | O    | EXT_WE#              |                                                      |
| 58            | O    | EXT_CSO#             |                                                      |
| 59            | O    | EXT_CS2#             |                                                      |
| 60            | O    | BE2#                 | NS9215 BE2#                                          |
| 61            | O    | BE3#                 | NS9215 BE3#                                          |
| 62            | I    | EXT_WAIT#            | 10k pull-up on module                                |
| 63            | O    | EXT_CLK#             | Connected over a 22R resistor to NS9215 CLK_OUT1 pin |
| 64            | P    | GND                  |                                                      |
| 65            | I    | ETH_TPIN             |                                                      |
| 66            | O    | ETH_ACTIVITY#        | Low active signal with 330R resistor on module       |
| 67            | I    | ETH_TPIP             |                                                      |
| 68            | O    | ETH_LINK#            | Low active signal with 330R resistor on module       |
| 69            | O    | ETH_TPON             |                                                      |
| 70            | O    | ETH_TPOP             |                                                      |
| 71            | P    | GND                  |                                                      |
| 72            | P    | USB_VBUS             | Power / See Note 1                                   |
| 73            | I    | USB_OC#              | See Note 1                                           |
| 74            | I/O  | USB_P                | See Note 1                                           |
| 75            | I/O  | USB_N                | See Note 1                                           |
| 76            | O    | USB_PWR#             | See Note 1                                           |
| 77            | I    | Reserved             |                                                      |

| X1 pin number | Type | Module Functionality | Comments                                                                                |
|---------------|------|----------------------|-----------------------------------------------------------------------------------------|
| 78            | P    | VRTC                 | Backup Battery for RTC, for 3V cell.<br>Can be left floating, if RTC backup not needed. |
| 79            | P    | VLIO                 | Mobile: Power from Li-Ion Battery (2.5V-5.5V)<br>Non-Mobile: connected to 3.3V          |
| 80            | P    | GND                  |                                                                                         |

**Note 1:** ConnectCore 3G 9P 9215 USB circuit only.

## X2 pinout

The following table shows the GPIO multiplexing capabilities for the Embedded Development Firmware module.

| X2 pin number | Type | Module Functionality                        | I/O Multiplexing                                         | Comments                                                                                                                                      |
|---------------|------|---------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 1             | P    | GND                                         |                                                          |                                                                                                                                               |
| 2             | P    | GND                                         |                                                          |                                                                                                                                               |
| 3             | I/O  | DCDA#<br>SPI_EN#<br>GPIO0<br>XBEE_ON_SLEEP# | DCDA#<br>DMA0_DONE<br>PIC_0_GEN_IO[0]<br>GPIO0<br>SPI_EN |                                                                                                                                               |
| 4             | I/O  | CTSA#<br>GPIO1                              | CTSA#<br>EIRQ0<br>PIC_0_GEN_IO[1]<br>GPIO1               | EIRQ0 - Reserved on wireless variant                                                                                                          |
| 5             | I/O  | DSRA#<br>GPIO2<br>XBEE_RESET#               | DSRA#<br>EIRQ1<br>PIC_0_GEN_IO[2]<br>GPIO2               |                                                                                                                                               |
| 6             | I/O  | RXDA<br>SPI_RXD<br>GPIO3                    | RXDA<br>DMA0_PDEN<br>PIC_0_GEN_IO[3]<br>GPIO3<br>SPI_RX  |                                                                                                                                               |
| 7             | I/O  | RIA#<br>ERIQ2<br>GPIO4                      | RIA#<br>EIRQ2<br>Timer6_in<br>GPIO4<br>SPI_CLK           | <b>Note:</b> This pin is used to force execution of a backup image for NET+OS, and should not be pulled down at start-up if used with NET+OS. |

| X2 pin number | Type | Module Functionality       | I/O Multiplexing                                                      | Comments                             |
|---------------|------|----------------------------|-----------------------------------------------------------------------|--------------------------------------|
| 8             | I/O  | RTSA#<br>SPI_CLK<br>GPIO5  | RTSA#<br>RS485CTLA<br>EIRQ3<br>Timer6_Out<br>GPIO5<br>SPI_CLK         |                                      |
| 9             | I/O  | DTRA#<br>GPIO6<br>SLEEP_RQ | DTRA#<br>TXCLKA<br>DMA0_REQ<br>Timer7_In<br>GPIO6<br>PIC_DBG_DATA_OUT |                                      |
| 10            | I/O  | TXDA<br>SPI_TXD<br>GPIO7   | TXDA<br>Timer8_In<br>Timer7_Out<br>GPIO7<br>SPI_TX                    |                                      |
| 11            | I/O  | DCDC#<br>TXCLKC<br>GPIO8   | DCDC#<br>DMA1_DONE<br>Timer8_Out<br>GPIO8<br>SPIB_EN                  |                                      |
| 12            | I/O  | CTSC#<br>GPIO9             | CTSC#<br>I2C_SCK<br>EIRQ0<br>GPIO9<br>PIC_DBG_DATA_IN                 | EIRQ0 - Reserved on wireless variant |
| 13            | I/O  | DSRC#<br>GPIO10            | DSRC#<br>QDCI<br>EIRQ1<br>GPIO10<br>PIC_DBG_CLK                       |                                      |
| 14            | I/O  | RXDC<br>GPIO11             | RXDC<br>DMA1_DP<br>EIRQ2<br>GPIO11<br>SPI_RXboot                      |                                      |

| X2 pin number | Type | Module Functionality      | I/O Multiplexing                                                      | Comments                                                                                                                                                        |
|---------------|------|---------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15            | I/O  | RIC#<br>RXCLKC<br>GPIO12  | RIC#<br>RXCLKC<br>I2C_SDA<br>RST_DONE<br>GPIO12<br>SPI_CLK            | When booting, NS9215 RIC# signal is default configured as Output, RST_DONE. To avoid input/output conflicts, put a series resistor on this signal if necessary. |
| 16            | I/O  | RTSC#<br>RXCLKC<br>GPIO13 | RTSC#<br>QDCQ<br>Ext Timer Event Out Ch 9<br>GPIO13<br>SPI_CLKboot    |                                                                                                                                                                 |
| 17            | I/O  | DTRC#<br>TXCLKC<br>GPIO14 | DTRC#<br>TXCLKC<br>DMA1_REQ<br>PIC_0_CAN_RXD<br>GPIO14<br>SPI_TXDboot |                                                                                                                                                                 |
| 18            | I/O  | TXDC<br>GPIO15            | TXDC<br>Timer9_In<br>PIC_0_CAN_TXD<br>GPIO15<br>SPI_ENboot            |                                                                                                                                                                 |
| 19            | I/O  | DCDB#<br>GPIO51           | DCDB#<br>PIC_0_BUS_1[8]<br>PIC_1_BUS_1[8]<br>GPIO51                   |                                                                                                                                                                 |
| 20            | I/O  | CTSB#<br>GPIO52           | CTSB#<br>PIC_0_BUS_1[9]<br>PIC_1_BUS_1[9]<br>GPIO52                   |                                                                                                                                                                 |
| 21            | I/O  | DSRB#<br>GPIO53           | DSRB#<br>PIC_0_BUS_1[10]<br>PIC_1_BUS_1[10]<br>GPIO53                 |                                                                                                                                                                 |
| 22            | I/O  | RXDB<br>GPIO54            | RXDB<br>PIC_0_BUS_1[11]<br>PIC_1_BUS_1[11]<br>GPIO54                  |                                                                                                                                                                 |

| X2 pin number | Type | Module Functionality | I/O Multiplexing                                                   | Comments |
|---------------|------|----------------------|--------------------------------------------------------------------|----------|
| 23            | I/O  | RIB#<br>GPIO55       | RIB#<br>PIC_0_BUS_1[12]<br>PIC_1_BUS_1[12]<br>GPIO55               |          |
| 24            | I/O  | RTSB#<br>GPIO56      | RTSB#<br>RS485CTLB<br>PIC_0_BUS_1[13]<br>PIC_1_BUS_1[13]<br>GPIO56 |          |
| 25            | I/O  | DTRB#<br>GPIO57      | TXCLKB<br>DTRB#<br>PIC_0_BUS_1[14]<br>PIC_1_BUS_1[14]<br>GPIO57    |          |
| 26            | I/O  | TXDB<br>GPIO58       | TXDB<br>PIC_0_BUS_1[15]<br>PIC_1_BUS_1[15]<br>GPIO58               |          |
| 27            | I/O  | DCDD#<br>GPIO59      | DCDD#<br>PIC_0_BUS_1[16]<br>PIC_1_BUS_1[16]<br>GPIO59              |          |
| 28            | I/O  | CTSD#<br>GPIO60      | CTSD#<br>PIC_0_BUS_1[17]<br>PIC_1_BUS_1[17]<br>GPIO60              |          |
| 29            | I/O  | DSRD#<br>GPIO61      | DSRD#<br>PIC_0_BUS_1[18]<br>PIC_1_BUS_1[18]<br>GPIO61              |          |
| 30            | I/O  | RXDDD<br>GPIO62      | RXDD<br>PIC_0_BUS_1[19]<br>PIC_1_BUS_1[19]<br>GPIO62               |          |
| 31            | I/O  | RID#<br>GPIO63       | RID#<br>PIC_0_BUS_1[20]<br>PIC_1_BUS_1[20]<br>GPIO63               |          |

| X2 pin number | Type | Module Functionality | I/O Multiplexing                                                   | Comments |
|---------------|------|----------------------|--------------------------------------------------------------------|----------|
| 32            | I/O  | RTSD#<br>GPIO64      | RTSD#<br>RS485CTLD<br>PIC_0_BUS_1[21]<br>PIC_1_BUS_1[21]<br>GPIO64 |          |
| 33            | I/O  | DTRD#<br>GPIO65      | TXCLKD<br>DTRD#<br>PIC_0_BUS_1[22]<br>PIC_1_BUS_1[22]<br>GPIO65    |          |
| 34            | I/O  | TXDD<br>GPIO66       | TXDD<br>PIC_0_BUS_1[23]<br>PIC_1_BUS_1[23]<br>GPIO66               |          |
| 35            | I/O  | GPIO67               | PIC_0_CLK[1]<br>PIC_0_CLK[0]<br>EIRQ3<br>GPIO67                    |          |
| 36            | I/O  | GPIO68               | PIC_0_GEN_IO[0]<br>PIC_1_GEN_IO[0]<br>PIC_1_CAN_RXD<br>GPIO68      |          |
| 37            | I/O  | GPIO69               | PIC_0_GEN_IO[1]<br>PIC_1_GEN_IO[1]<br>PIC_1_CAN_TXD<br>GPIO69      |          |
| 38            | I/O  | GPIO70               | PIC_0_GEN_IO[2]<br>PIC_1_GEN_IO[2]<br>PWM0<br>GPIO70               |          |
| 39            | I/O  | GPIO71               | PIC_0_GEN_IO[3]<br>PIC_1_GEN_IO[3]<br>PWM1<br>GPIO71               |          |
| 40            | I/O  | GPIO72               | PIC_0_GEN_IO[4]<br>PIC_1_GEN_IO[4]<br>PWM2<br>GPIO72               |          |

| X2 pin number | Type | Module Functionality    | I/O Multiplexing                                          | Comments |
|---------------|------|-------------------------|-----------------------------------------------------------|----------|
| 41            | I/O  | GPIO73                  | PIC_0_GEN_IO[5]<br>PIC_1_GEN_IO[5]<br>PWM3<br>GPIO73      |          |
| 42            | I/O  | GPIO74                  | PIC_0_GEN_IO[6]<br>PIC_1_GEN_IO[6]<br>Timer0_In<br>GPIO74 |          |
| 43            | I/O  | GPIO75                  | PIC_0_GEN_IO[7]<br>PIC_1_GEN_IO[7]<br>Timer1_In<br>GPIO75 |          |
| 44            | I/O  | GPIO76                  | PIC_0_CTL_IO[0]<br>PIC_1_CTL_IO[0]<br>Timer2_In<br>GPIO76 |          |
| 45            | I/O  | GPIO77                  | PIC_0_CTL_IO[1]<br>PIC_1_CTL_IO[1]<br>Timer3_In<br>GPIO77 |          |
| 46            | I/O  | GPIO78                  | PIC_0_CTL_IO[2]<br>PIC_1_CTL_IO[2]<br>Timer4_In<br>GPIO78 |          |
| 47            | I/O  | GPIO79                  | PIC_0_CTL_IO[3]<br>PIC_1_CTL_IO[3]<br>Timer5_In<br>GPIO79 |          |
| 48            | I/O  | GPIO80                  | PIC_0_BUS_0[0]<br>PIC_1_BUS_0[0]<br>Timer6_In<br>GPIO80   |          |
| 49            | I/O  | USER_BUTTON1#<br>GPIO81 | PIC_0_BUS_0[1]<br>PIC_1_BUS_0[1]<br>Timer7_In<br>GPIO81   |          |
| 50            | I/O  | USER_LED1#<br>GPIO82    | PIC_0_BUS_0[2]<br>PIC_1_BUS_0[2]<br>Timer8_In<br>GPIO82   |          |

| X2 pin number | Type | Module Functionality    | I/O Multiplexing                                            | Comments |
|---------------|------|-------------------------|-------------------------------------------------------------|----------|
| 51            | I/O  | GPIO83                  | PIC_0_BUS_0[3]<br>PIC_1_BUS_0[3]<br>Timer9_In<br>GPIO83     |          |
| 52            | I/O  | USER_BUTTON2#<br>GPIO84 | PIC_0_BUS_0[4]<br>PIC_1_BUS_0[4]<br>Timer0_Out<br>GPIO84    |          |
| 53            | I/O  | USER_LED2#<br>GPIO85    | PIC_0_BUS_0[5]<br>PIC_1_BUS_0[5]<br>Timer1_Out<br>GPIO85    |          |
| 54            | I/O  | GPIO86                  | PIC_0_BUS_0[6]<br>PIC_1_BUS_0[6]<br>Timer2_Out<br>GPIO86    |          |
| 55            | I/O  | GPIO87                  | PIC_0_BUS_0[7]<br>PIC_1_BUS_0[7]<br>Timer3_Out<br>GPIO87    |          |
| 56            | I/O  | GPIO93                  | PIC_0_BUS_0[13]<br>PIC_1_BUS_0[13]<br>Timer9_Out<br>GPIO93  |          |
| 57            | I/O  | GPIO94                  | PIC_0_BUS_0[14]<br>PIC_1_BUS_0[14]<br>QDCI<br>GPIO94        |          |
| 58            | I/O  | GPIO95                  | PIC_0_BUS_0[15]<br>PIC_1_BUS_0[15]<br>QDCQ<br>GPIO95        |          |
| 59            | I/O  | CAN0_RXD<br>GPIO96      | PIC_0_BUS_1[0]<br>PIC_1_BUS_1[0]<br>PIC_0_CAN_RXD<br>GPIO96 |          |
| 60            | I/O  | CAN0_TXD<br>GPIO97      | PIC_0_BUS_1[1]<br>PIC_1_BUS_1[1]<br>PIC_0_CAN_TXD<br>GPIO97 |          |

| X2 pin number | Type | Module Functionality  | I/O Multiplexing                                            | Comments                                                |
|---------------|------|-----------------------|-------------------------------------------------------------|---------------------------------------------------------|
| 61            | I/O  | CAN1_RXD<br>GPIO98    | PIC_0_BUS_1[2]<br>PIC_1_BUS_1[2]<br>PIC_1_CAN_RXD<br>GPIO98 |                                                         |
| 62            | I/O  | CAN1_TXD<br>GPIO99    | PIC_0_BUS_1[3]<br>PIC_1_BUS_1[3]<br>PIC_1_CAN_TXD<br>GPIO99 |                                                         |
| 63            | I/O  | GPIO100               | PIC_0_BUS_1[4]<br>PIC_1_BUS_1[4]<br>PWM4<br>GPIO100         |                                                         |
| 64            | I/O  | EIRQ3#<br>GPIO101     | PIC_0_BUS_1[5]<br>PIC_1_BUS_1[5]<br>EIRQ3<br>GPIO101        |                                                         |
| 65            | I/O  | I2C_SCL<br>GPIO102    | PIC_0_BUS_1[6]<br>PIC_1_BUS_1[6]<br>I2C_SCL<br>GPIO102      | 4k7 pull-up on module                                   |
| 66            | I/O  | I2C_SDA<br>GPIO103    | PIC_0_BUS_1[7]<br>PIC_1_BUS_1[7]<br>I2C_SDA<br>GPIO103      | 4k7 pull-up on module                                   |
| 67            | I    | ADC_IN0               | VIN0_ADC                                                    |                                                         |
| 68            | I    | ADC_IN1               | VIN1_ADC                                                    |                                                         |
| 69            | I    | ADC_IN2               | VIN2_ADC                                                    |                                                         |
| 70            | I    | ADC_IN3               | VIN3_ADC                                                    |                                                         |
| 71            | I    | ADC_IN4               | VIN4_ADC                                                    |                                                         |
| 72            | I    | ADC_IN5               | VIN5_ADC                                                    |                                                         |
| 73            | I    | ADC_IN6               | VIN6_ADC                                                    |                                                         |
| 74            | I    | ADC_IN7               | VIN7_ADC                                                    |                                                         |
| 75            | P    | VSS_ADC               |                                                             | Connected on module to AGND through 0Ω resistor         |
| 76            | P    | VREF_ADC              |                                                             | 100nF decoupling capacitor between VREF_ADC and VSS_ADC |
| 77            | P    | V <sub>DD</sub> +3.3V |                                                             |                                                         |

| X2 pin number | Type | Module Functionality  | I/O Multiplexing | Comments |
|---------------|------|-----------------------|------------------|----------|
| 78            | P    | V <sub>DD</sub> +3.3V |                  |          |
| 79            | P    | GND                   |                  |          |
| 80            | P    | GND                   |                  |          |

## Configuration pins — CPU

None of the 64 GPIO pins on connector X2 disturb CPU boot strap functions. The boot strap functions are controlled by address signals. A user can not disturb boot strap functions from the outside if the module configuration signals, described below, are correctly configured.

### Default module CPU configuration

The user has access to six configuration signals:

- LITTLE#/BIG\_ ENDIAN which allows the user to select the endianness of the module
- OCD\_EN# which allows the user to activate on-chip debugging
- SW\_CONF [3:0] which are reserved for the user; the user software can read out these signals through the GEN ID register (@ 0xA090\_0210).

## Configuration pins — Module

The ConnectCore 9P 9215 Family of modules support the following JTAG signals: TCK, TMS, TDI, TDO, TRST#, and RTCK. Selection can be made between ARM debug mode and boundary scan mode with the signal OCD\_EN#.

### Identification of the module

In order to make it easier for software to recognize a module and especially a hardware variant of the module, a specific bit field made of 4 bits has been reserved on the module. This bit field can be read out through GEN ID register and corresponds to A[12:9]. These configuration signals use the internal CPU pull-up resistor and can be pulled down through external population option 2k2 resistors.

In the same way, 3 bits are available on the module to identify the SDRAM configuration scheme. These bits correspond to A[19:17]. It is impossible for the user to disturb either the variant specific or SDRAM configuration specific bits from outside.

In addition, the ConnectCore 9P 9215 Family of modules have reserved 4 bits for special platform identification. This bit field can be read out through GEN ID register and corresponds to A[16:13]. Configuration of these signals is done through the SW\_CONF pins. SW\_CONF0 is connected to A13 through a 2k2 series resistor, and so on for the further SW\_CONF pins. Therefore, this bit can be set high by leaving the

corresponding SW\_CONF pin unconnected and set low by connecting the corresponding SW\_CONF pin directly low.

These pins are available for user defined application or platform specific software configurations.

## Module pin configuration

| Signal name        | Function                                                                                                                  | PU/PD  | Comment                                                                                         |
|--------------------|---------------------------------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------------|
| LITTLE#/BIG_ENDIAN | Set module endianness. 0 module boots in little endian mode. 1 module boots in big endian mode.                           | PU     | Signal LITTLE#/BIG_ENDIAN is connected to GPIO_A3/A27 through a 2k2 series resistor.            |
| OCD_EN#            | JTAG / Boundary scan function select<br>0 ARM debug mode, BISTEN# set to high<br>1 Boundary scan mode, BISTEN# set to low | PU 10K |                                                                                                 |
| SW_CONF0           | This pin is a user/application defined software configuration pin.                                                        |        | Connected to A13 through a 2k2 series resistor.<br>Read bit 4 of GEN ID register (@0xA0900210). |
| SW_CONF1           | This pin is a user/application defined software configuration pin.                                                        |        | Connected to A14 through a 2k2 series resistor.<br>Read bit 5 of GEN ID register (@0xA0900210). |
| SW_CONF2           | This pin is a user/application defined software configuration pin.                                                        |        | Connected to A15 through a 2k2 series resistor.<br>Read bit 6 of GEN ID register (@0xA0900210). |
| SW_CONF3           | This pin is a user/application defined software configuration pin.                                                        |        | Connected to A16 through a 2k2 series resistor.<br>Read bit 7 of GEN ID register (@0xA0900210). |

## Clock generation

### Clock frequencies

Hardware strapping determines the initial powerup PLL settings. The table below summarizes the default clock frequencies for the ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 modules:

#### Hardware strapping:

"PLL reference clock divider setting:

A[4:0] = 0x1D (0b11101)

NR = 5

"PLL output divider setting:

A[6:5] = 0x3 (0b11)

OD = 0

"PLL bypass setting:

A[7] = 0x1 (0b1)

Normal operation

#### PLL frequency formula:

$PLL\ V_{co} = (RefClk / NR + 1) * (NF + 1)$

$ClkOut = PLL\ V_{co} / (OD + 1)$

RefClk (Crystal) = 29.4912MHz

NF = 0x3C (reset value - can only be changed by software).

$PLL\ V_{co} = (29.4912 / 6) * 61 = 299.8272\ MHz$

$ClkOut = 299.8272\ MHz$

#### Resulting clock settings:

PIC clock = 299.8272 MHz

CPU clock = 299.8272 MHz / 2 = 149.9136 MHz

AHB clock = 149.9136 MHz / 2 = 74.9568 MHz

## Changing the CPU speed

After power-up, software can change the PLL settings by writing to the PLL configuration register (@ 0xA090\_0188).

**Important:** When PLL parameters are changed, a reset is provided for the PLL to stabilize. Applications using this feature need to be aware that the SDRAM contents will be lost. See reset behavior in the table below.

| Reset Behavior               | RESET<br>_n pin | SRESET<br>_n pin | PLL Config<br>Reg. Update | Watchdog<br>Time-Out<br>Reset |
|------------------------------|-----------------|------------------|---------------------------|-------------------------------|
| SPI boot                     | YES             | YES              | YES                       | YES                           |
| Strapping PLL                | YES             | NO               | NO                        | NO                            |
| Other strappings (Endianess) | YES             | NO               | NO                        | NO                            |
| GPIO configuration           | YES             | NO               | NO                        | NO                            |
| Other (ASIC) registers       | YES             | YES              | YES                       | YES                           |
| SDRAM keeps its contents     | NO              | YES              | NO                        | YES                           |

## Boot process

The ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 modules boot directly from NOR flash. The start-up code is located at address 0x00000000 during the boot process. When the system is booted, the SDRAM is remapped to address 0x00000000 and NOR Flash to 0x50000000 by modifying the address map in the AHB decoder.

## Chip selects

The module has eight chip selects: four for dynamic memory and four for static memory. Each chip select has a 256MB range.

**Chip select memory map**

| Name     | CPU Sig. name | Pin | Address range         | Size [Mb] | Usage          | Comments                    |
|----------|---------------|-----|-----------------------|-----------|----------------|-----------------------------|
| SDM_CS0# | CS1#          | D6  | 0x00000000–0x0FFFFFFF | 256       | SDRAM bank 0   | First bank on module        |
| SDM_CS1# | CS3#          | B5  | 0x10000000–0x1FFFFFFF | 256       | not used       |                             |
| SDM_CS2# | CS5#          | A4  | 0x20000000–0x2FFFFFFF | 256       | not used       |                             |
| SDM_CS3# | CS7#          | B4  | 0x30000000–0x3FFFFFFF | 256       | not used       |                             |
| EXT_CS0# | CS0#          | C6  | 0x40000000–0x4FFFFFFF | 256       | external, CS0# |                             |
| INT_CS1# | CS2#          | B6  | 0x50000000–0x5FFFFFFF | 256       | NOR-Flash      | Program memory on module    |
| EXT_CS2# | CS4#          | C5  | 0x60000000–0x6FFFFFFF | 256       | external, CS2# |                             |
| INT_CS3# | CS6#          | A3  | 0x70000000–0x7FFFFFFF | 256       | internal, CS3# | Reserved for internal usage |

## SDRAM banks

The modules provide connection to 1 SDRAM chip, connected to CS1# (SDM\_CS0#). The other SDRAM chip selects are not used. The standard module has one of these SDRAM onboard: 1Mx16x4-banks. A13 is the highest address connected. BA0 and BA1 are connected to A21 and A22, respectively.

## Multiplexed GPIO pins

The 108 GPIO pins (including address bits A24 through A27) available on the module connector are multiplexed with other functions, such as:

- UART
- SPI
- Ethernet
- DMA
- I<sup>2</sup>C port
- Timers and interrupt inputs
- Memory bus data

### Pin notes

- GPIO [15:0] has five multiplex modes.
- GPIO [103:16] and GPIO\_A [3:0] have four multiplex modes.
- Using a pin as GPIO may result in the loss of some functionalities. Certain functions are duplicated to enhance the likelihood of the pin being used without sacrificing other vital functions.
- Using original and (dup) functions in parallel is not recommended.
- Default function of GPIOs after CPU power-up is function 03, except GPIO12 (function 02-reset\_done) and GPIO [31:16] (function 00 - DATA[15:0]).

### GPIO multiplex table

In the GPIO multiplex table below,

- the default function is written in bold,
- # means low active signal,
- (dup) means the function is available multiple times.

| Port name, Function 03 | Alternate function 00 | Alternate function 01 | Alternate function 02 | Alternate function 04 (only GPIO00 ...GPIO15) | On module, default used as |
|------------------------|-----------------------|-----------------------|-----------------------|-----------------------------------------------|----------------------------|
| GPIO0                  | DCDA#                 | DMA0_DONE             | PIC_0_GEN_IO[0]       | SPI_EN# (dup)                                 | DCDA# / SPI_EN#            |
| GPIO1                  | CTSA#                 | EIRQ0                 | PIC_0_GEN_IO[1]       | EIRQ0 - Reserved on wireless variant          | CTSA#                      |
| GPIO2                  | DSRA#                 | EIRQ1                 | PIC_0_GEN_IO[2]       | Reserved                                      | DSRA#                      |
| GPIO3                  | RXDA#                 | DMA0_PDEN             | PIC_0_GEN_IO[3]       | SPI_RXD (dup)                                 | RXDA / SPI_RXD             |
| GPIO4                  | RIA#                  | EIRQ2                 | Timer6_In             | SPI_CLK (dup)                                 | RIA# / SPI_CLK             |
| GPIO5                  | RTSA# / 485CTLA       | EIRQ3                 | Timer6_Out            | SPI_CLK (dup)                                 | RTSA#                      |

| Port name, Function 03 | Alternate function 00   | Alternate function 01 | Alternate function 02                       | Alternate function 04 (only GPIO00 ...GPIO15) | On module, default used as    |
|------------------------|-------------------------|-----------------------|---------------------------------------------|-----------------------------------------------|-------------------------------|
| GPIO6                  | TXCLKA / DTRA#          | DMA0_REQ              | Timer7_In                                   | PIC_DBG_DATA_OUT                              | DTRA#                         |
| GPIO7                  | TXDA                    | Timer8_In             | Timer7_Out                                  | SPI_TXD (dup)                                 | TXDA / SPI_TXD                |
| GPIO8                  | DCDC# / TXCLKC          | DMA1_DONE             | Timer8_Out                                  | SPI_EN# (dup)                                 | DCDC#                         |
| GPIO9                  | CTSC#                   | I2C_SCL               | EIRQ0 (dup)<br>Reserved on wireless variant | PIC_DBG_DATA_IN                               | CTSC#                         |
| GPIO10                 | DSRC#                   | QDCI                  | EIRQ1 (dup)                                 | PIC_DBG_CLK                                   | DSRC#                         |
| GPIO11                 | RXDC#                   | DMA1_PDEN             | EIRQ2 (dup)                                 | SPI_RXD (boot)                                | RXDC                          |
| GPIO12                 | RXCLKC / RIC#           | I2C_SDA               | RESET_DONE                                  | SPI_CLK (dup)                                 | RIC# <sup>1</sup>             |
| GPIO13                 | RXCLKC / RTSC# / 485CTL | QDCQ                  | Timer9_out                                  | SPI_CLK (boot)                                | RXCLKC / RTSC#                |
| GPIO14                 | TXCLKC / DTRC#          | DMA1_REQ              | PIC_0_CAN_RXD                               | SPI_TXD (boot)                                | TXCLKC                        |
| GPIO15                 | TXDC                    | Timer9_In             | PIC_0_CAN_TXD                               | SPI_EN# (boot)                                | TXDC                          |
| GPIO16                 | D0                      | DCDB#                 | EIRQ0 (dup)<br>Reserved on wireless variant |                                               | Reserved for upper data lines |
| GPIO17                 | D1                      | CTSB#                 | EIRQ1 (dup)                                 |                                               | Reserved for upper data lines |
| GPIO18                 | D2                      | DSRB#                 | EIRQ2 (dup)                                 |                                               | Reserved for upper data lines |
| GPIO19                 | D3                      | RXDB                  | EIRQ3 (dup)                                 |                                               | Reserved for upper data lines |
| GPIO20                 | D4                      | RIB#                  | DMA0_DONE (dup)                             |                                               | Reserved for upper data lines |
| GPIO21                 | D5                      | RTSB# / 485CTLB       | DMA0_PDEN (dup)                             |                                               | Reserved for upper data lines |
| GPIO22                 | D6                      | TXCLKB / DTRB#        | DMA1_DONE (dup)                             |                                               | Reserved for upper data lines |
| GPIO23                 | D7                      | TXDB                  | PIC_1_CAN_RXD                               |                                               | Reserved for upper data lines |
| GPIO24                 | D8                      | DCDD#                 | PIC_1_CAN_TXD                               |                                               | Reserved for upper data lines |
| GPIO25                 | D9                      | CTSD#                 | RESET_DONE (dup)                            |                                               | Reserved for upper data lines |
| GPIO26                 | D10                     | DSRD#                 | PIC_1_GEN_IO[0]                             |                                               | Reserved for upper data lines |

| Port name, Function 03 | Alternate function 00 | Alternate function 01 | Alternate function 02 | Alternate function 04 (only GPIO00 ...GPIO15) | On module, default used as    |
|------------------------|-----------------------|-----------------------|-----------------------|-----------------------------------------------|-------------------------------|
| GPIO27                 | D11                   | RXDD                  | PIC_1_GEN_IO[1]       |                                               | Reserved for upper data lines |
| GPIO28                 | D12                   | RID#                  | PIC_1_GEN_IO[2]       |                                               | Reserved for upper data lines |
| GPIO29                 | D13                   | RTSD# / 485CTLD       | PIC_1_GEN_IO[3]       |                                               | Reserved for upper data lines |
| GPIO30                 | D14                   | TXCLKD / DTRD#        | Reserved              |                                               | Reserved for upper data lines |
| GPIO31                 | D15                   | TXDD                  | Reserved              |                                               | Reserved for upper data lines |
| GPIO32                 | MII_MDC               | PIC_0_GEN_IO[0]       | Reserved              |                                               | MII Interface                 |
| GPIO33                 | MII_TXC               | PIC_0_GEN_IO[1]       | Reserved              |                                               | MII Interface                 |
| GPIO34                 | MII_RXC               | PIC_0_GEN_IO[2]       | Reserved              |                                               | MII Interface                 |
| GPIO35                 | MII_MDIO              | PIC_0_GEN_IO[3]       | Reserved              |                                               | MII Interface                 |
| GPIO36                 | MII_RXDV              | PIC_0_GEN_IO[4]       | Reserved              |                                               | MII Interface                 |
| GPIO37                 | MII_RXER              | PIC_0_GEN_IO[5]       | Reserved              |                                               | MII Interface                 |
| GPIO38                 | MII_RXD0              | PIC_0_GEN_IO[6]       | Reserved              |                                               | MII Interface                 |
| GPIO39                 | MII_RXD1              | PIC_0_GEN_IO[7]       | Reserved              |                                               | MII Interface                 |
| GPIO40                 | MII_RXD2              | PIC_1_GEN_IO[0]       | Reserved              |                                               | MII Interface                 |
| GPIO41                 | MII_RXD3              | PIC_1_GEN_IO[1]       | Reserved              |                                               | MII Interface                 |
| GPIO42                 | MII_TXEN              | PIC_1_GEN_IO[2]       | Reserved              |                                               | MII Interface                 |
| GPIO43                 | MII_TXER              | PIC_1_GEN_IO[3]       | Reserved              |                                               | MII Interface                 |
| GPIO44                 | MII_TXD0              | PIC_1_GEN_IO[4]       | Reserved              |                                               | MII Interface                 |
| GPIO45                 | MII_TXD1              | PIC_1_GEN_IO[5]       | Reserved              |                                               | MII Interface                 |
| GPIO46                 | MII_TXD2              | PIC_1_GEN_IO[6]       | Reserved              |                                               | MII Interface                 |
| GPIO47                 | MII_TXD3              | PIC_1_GEN_IO[7]       | Reserved              |                                               | MII Interface                 |
| GPIO48                 | MII_COL               | Reserved              | Reserved              |                                               | MII Interface                 |
| GPIO49                 | MII_CRS               | Reserved              | Reserved              |                                               | MII Interface                 |
| GPIO50                 | MII_PHY_Int           | PIC_1_CLK (I)         | PIC_1_CLK(0)          |                                               | MII Interface                 |
| GPIO51                 | DCDB# (dup)           | PIC_0_BUS_1[8]        | PIC_1_BUS_1[8]        |                                               | DCDB#                         |
| GPIO52                 | CTSB# (dup)           | PIC_0_BUS_1[9]        | PIC_1_BUS_1[9]        |                                               | CTSB#                         |
| GPIO53                 | DSRB# (dup)           | PIC_0_BUS_1[10]       | PIC_1_BUS_1[10]       |                                               | DSRB#                         |
| GPIO54                 | RXDB (dup)            | PIC_0_BUS_1[11]       | PIC_1_BUS_1[11]       |                                               | RXDB                          |

| Port name, Function 03 | Alternate function 00      | Alternate function 01 | Alternate function 02 | Alternate function 04 (only GPIO00 ...GPIO15) | On module, default used as |
|------------------------|----------------------------|-----------------------|-----------------------|-----------------------------------------------|----------------------------|
| GPIO55                 | RIB# (dup)                 | PIC_0_BUS_1[12]       | PIC_1_BUS_1[12]       |                                               | RIB#                       |
| GPIO56                 | RTSB# / 485CTLB (dup)      | PIC_0_BUS_1[13]       | PIC_1_BUS_1[13]       |                                               | RTSB#                      |
| GPIO57                 | TXCLKB (dup) / DTRB# (dup) | PIC_0_BUS_1[14]       | PIC_1_BUS_1[14]       |                                               | DTRB#                      |
| GPIO58                 | TXDB (dup)                 | PIC_0_BUS_1[15]       | PIC_1_BUS_1[15]       |                                               | TXDB                       |
| GPIO59                 | DCDD# (dup)                | PIC_0_BUS_1[16]       | PIC_1_BUS_1[16]       |                                               | DCDD#                      |
| GPIO60                 | CTSD# (dup)                | PIC_0_BUS_1[17]       | PIC_1_BUS_1[17]       |                                               | CTSD#                      |
| GPIO61                 | DSRD# (dup)                | PIC_0_BUS_1[18]       | PIC_1_BUS_1[18]       |                                               | DSRD#                      |
| GPIO62                 | RXDD (dup)                 | PIC_0_BUS_1[19]       | PIC_1_BUS_1[19]       |                                               | RXDD                       |
| GPIO63                 | RID# (dup)                 | PIC_0_BUS_1[20]       | PIC_1_BUS_1[20]       |                                               | RID#                       |
| GPIO64                 | RTSD# / 485CTLD (dup)      | PIC_0_BUS_1[21]       | PIC_1_BUS_1[21]       |                                               | RTSD#                      |
| GPIO65                 | TXCLKD (dup) / DTRD# (dup) | PIC_0_BUS_1[22]       | PIC_1_BUS_1[22]       |                                               | DTRD#                      |
| GPIO66                 | TXDD (dup)                 | PIC_0_BUS_1[23]       | PIC_1_BUS_1[23]       |                                               | TXDD                       |
| GPIO67                 | PIC_0_CLK (I)              | PIC_0_CLK (O)         | EIRQ3 (dup)           |                                               | PIC_0_CLK                  |
| GPIO68                 | PIC_0_GEN_IO[0]            | PIC_1_GEN_IO[0]       | PIC_1_CAN_RXD         |                                               | PIC_0_GEN_IO[0]            |
| GPIO69                 | PIC_0_GEN_IO[1]            | PIC_1_GEN_IO[1]       | PIC_1_CAN_TXD         |                                               | PIC_0_GEN_IO[1]            |
| GPIO70                 | PIC_0_GEN_IO[2]            | PIC_1_GEN_IO[2]       | PWM0                  |                                               | PIC_0_GEN_IO[2]            |
| GPIO71                 | PIC_0_GEN_IO[3]            | PIC_1_GEN_IO[3]       | PWM1                  |                                               | PIC_0_GEN_IO[3]            |
| GPIO72                 | PIC_0_GEN_IO[4]            | PIC_1_GEN_IO[4]       | PWM2                  |                                               | PIC_0_GEN_IO[4]            |
| GPIO73                 | PIC_0_GEN_IO[5]            | PIC_1_GEN_IO[5]       | PWM3                  |                                               | PIC_0_GEN_IO[5]            |
| GPIO74                 | PIC_0_GEN_IO[6]            | PIC_1_GEN_IO[6]       | Timer0_In             |                                               | PIC_0_GEN_IO[6]            |
| GPIO75                 | PIC_0_GEN_IO[7]            | PIC_1_GEN_IO[7]       | Timer1_In             |                                               | PIC_0_GEN_IO[7]            |
| GPIO76                 | PIC_0_CTL_IO[0]            | PIC_1_CTL_IO[0]       | Timer2_In             |                                               | PIC_0_CTL_IO[0]            |
| GPIO77                 | PIC_0_CTL_IO[1]            | PIC_1_CTL_IO[1]       | Timer3_In             |                                               | PIC_0_CTL_IO[1]            |
| GPIO78                 | PIC_0_CTL_IO[2]            | PIC_1_CTL_IO[2]       | Timer4_In             |                                               | PIC_0_CTL_IO[2]            |
| GPIO79                 | PIC_0_CTL_IO[3]            | PIC_1_CTL_IO[3]       | Timer5_In             |                                               | PIC_0_CTL_IO[3]            |
| GPIO80                 | PIC_0_BUS_0[0]             | PIC_1_BUS_0[0]        | Timer6_In (dup)       |                                               | Timer6_In                  |
| GPIO81                 | PIC_0_BUS_0[1]             | PIC_1_BUS_0[1]        | Timer7_In (dup)       |                                               | Timer7_In                  |
| GPIO82                 | PIC_0_BUS_0[2]             | PIC_1_BUS_0[2]        | Timer8_In (dup)       |                                               | Timer8_In                  |
| GPIO83                 | PIC_0_BUS_0[3]             | PIC_1_BUS_0[3]        | Timer9_In (dup)       |                                               | Timer9_In                  |

| Port name, Function 03 | Alternate function 00 | Alternate function 01 | Alternate function 02 | Alternate function 04 (only GPIO00 ...GPIO15) | On module, default used as           |
|------------------------|-----------------------|-----------------------|-----------------------|-----------------------------------------------|--------------------------------------|
| GPIO84                 | PIC_0_BUS_0[4]        | PIC_1_BUS_0[4]        | Timer0_Out            |                                               | Timer0_Out                           |
| GPIO85                 | PIC_0_BUS_0[5]        | PIC_1_BUS_0[5]        | Timer1_Out            |                                               | Timer1_Out                           |
| GPIO86                 | PIC_0_BUS_0[6]        | PIC_1_BUS_0[6]        | Timer2_Out            |                                               | Timer2_Out                           |
| GPIO87                 | PIC_0_BUS_0[7]        | PIC_1_BUS_0[7]        | Timer3_Out            |                                               | Timer3_Out                           |
| GPIO88                 | PIC_0_BUS_0[8]        | PIC_1_BUS_0[8]        | Timer4_Out            |                                               | User LED 0 => LED 1 (on module)      |
| GPIO89                 | PIC_0_BUS_0[9]        | PIC_1_BUS_0[9]        | Timer5_Out            |                                               | User LED 1 => LED 2 (on module)      |
| GPIO90                 | PIC_0_BUS_0[10]       | PIC_1_BUS_0[10]       | Timer6_Out (dup)      |                                               | GPIO reserved on module              |
| GPIO91                 | PIC_0_BUS_0[11]       | PIC_1_BUS_0[11]       | Timer7_Out (dup)      |                                               | Reserved NAND_R/B#                   |
| GPIO92                 | PIC_0_BUS_0[12]       | PIC_1_BUS_0[12]       | Timer8_Out (dup)      |                                               | GPIO reserved on module              |
| GPIO93                 | PIC_0_BUS_0[13]       | PIC_1_BUS_0[13]       | Timer9_Out (dup)      |                                               | Timer9_Out                           |
| GPIO94                 | PIC_0_BUS_0[14]       | PIC_1_BUS_0[14]       | QDCI (dup)            |                                               | QDCI                                 |
| GPIO95                 | PIC_0_BUS_0[15]       | PIC_1_BUS_0[15]       | QDCQ (dup)            |                                               | QDCQ                                 |
| GPIO96                 | PIC_0_BUS_1[0]        | PIC_1_BUS_1[0]        | PIC_0_CAN_RXD         |                                               | PIC_0_CAN_RXD                        |
| GPIO97                 | PIC_0_BUS_1[1]        | PIC_1_BUS_1[1]        | PIC_0_CAN_TXD         |                                               | PIC_0_CAN_TXD                        |
| GPIO98                 | PIC_0_BUS_1[2]        | PIC_1_BUS_1[2]        | PIC_1_CAN_RXD         |                                               | PIC_1_CAN_RXD                        |
| GPIO99                 | PIC_0_BUS_1[3]        | PIC_1_BUS_1[3]        | PIC_1_CAN_TXD         |                                               | PIC_1_CAN_TXD                        |
| GPIO100                | PIC_0_BUS_1[4]        | PIC_1_BUS_1[4]        | PWM4                  |                                               | PWM4                                 |
| GPIO101                | PIC_0_BUS_1[5]        | PIC_1_BUS_1[5]        | EIRQ3 (dup)           |                                               | EIRQ3                                |
| GPIO102                | PIC_0_BUS_1[6]        | PIC_1_BUS_1[6]        | I2C_SCL (dup)         |                                               | I2C_SCL                              |
| GPIO103                | PIC_0_BUS_1[7]        | PIC_1_BUS_1[7]        | I2C_SDA (dup)         |                                               | I2C_SDA                              |
| GPIO_A0                | A24                   | I2C_SCL dupe          | EIRQ0 (dup)           |                                               | EIRQ0 - Reserved on wireless variant |
| GPIO_A1                | A25                   | I2C_SDA dupe          | EIRQ1 (dup)           |                                               | Reserved EIRQ1 - USB                 |
| GPIO_A2                | A26                   | CS0_WE#               | EIRQ2 (dup)           |                                               | GPIO reserved on module              |
| GPIO_A3                | A27                   | CS0_OE#               | UART_REFCLK           |                                               | Little/Big Endian                    |

<sup>1</sup> Put a series resistor on the Development Board in this case to avoid input/output conflict between RESET\_DONE (output/boot default) and RIC# (input/configuration default).

## Module LEDs

The ConnectCore 9P 9215 Family of modules have two on module LEDs: LE1 and LE2. For each module variant, the default use varies:

- **ConnectCore 9P 9215:** LE1 will flash a repeating blink pattern in a major system failure; for example, a processor execution or power-on self test failure.
- **ConnectCore Wi-9P 9215:** To indicate WLAN-related information, such as association status and network activity.

### ConnectCore 9P 9215 LEDs

| ID  | Connects to | Default | Description                                   |
|-----|-------------|---------|-----------------------------------------------|
| LE1 | GPIO88      | Off     | Setting to output logic “0” turns on the LED. |
| LE2 | GPIO89      | Off     | Setting to output logic “0” turns on the LED. |

### ConnectCore Wi-9P 9215 LEDs

| ID  | Color  | LED              | Blink pattern | Status / Activity                                               |
|-----|--------|------------------|---------------|-----------------------------------------------------------------|
| LE1 | Green  | Link integrity   | On            | The unit is associated to an access point (infrastructure mode) |
|     |        |                  | Slow          | The unit is in ad-hoc mode                                      |
|     |        |                  | Quick         | The unit is scanning for a network                              |
| LE2 | Yellow | Network activity | Blinking      | Network traffic is received or transmitted                      |
|     |        |                  | Off           | Network is idle                                                 |

**Note:** The network activity LED is used for diagnostic purposes during boot-up.

## External interrupts

The ConnectCore 9P 9215 Family of modules provide access to four external interrupts signals, which are multiplexed with other functions on the GPIO pins.

| External interrupt | GPIO multiplexing | Other functions,<br>1st position | Comments                                                                                                    |
|--------------------|-------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------|
| EIRQ0              | GPIO1             | X2.4                             | EIRQ0 is used in ConnectCore Wi-9P 9215 as radio chip interrupt and is not available for use.               |
|                    | GPIO9             | X2.12                            |                                                                                                             |
|                    | GPIO16            |                                  |                                                                                                             |
|                    | GPIO_A0           |                                  |                                                                                                             |
| EIRQ1              | GPIO2             | X2.5                             |                                                                                                             |
|                    | GPIO10            | X2.13                            |                                                                                                             |
|                    | GPIO17            |                                  |                                                                                                             |
|                    | GPIO_A1           |                                  |                                                                                                             |
| EIRQ2              | GPIO4             | X2.7                             |                                                                                                             |
|                    | GPIO11            | X2.14                            |                                                                                                             |
|                    | GPIO18            |                                  |                                                                                                             |
|                    | GPIO_A2           |                                  |                                                                                                             |
| EIRQ3              | GPIO5             | X2.8                             | EIRQ3# is used on the Development Board to implement I <sup>2</sup> C I/O expander interrupt functionality. |
|                    | GPIO67            | X2.35                            |                                                                                                             |
|                    | GPIO101           | X2.64                            |                                                                                                             |
|                    | GPIO19            |                                  |                                                                                                             |

## Interfaces

### 10/100 Mbps Ethernet port

The Digi NS9215 processor's 10/100 Mbps Ethernet MAC allows a glueless connection of a 3.3V MII PHY chip that generates the physical Ethernet signals.

The module has a MII PHY chip in a 56-pin QFN package on board. By default, the module does not have a transformer or Ethernet connector; the Development Board must provide these parts. However, it's possible to populate a specific RJ45 connector with magnetics on the module. The appropriate RJ-45 is Midcom MIC2412A-5108W-LF3.

A PHY clock of 25 MHz is generated in the PHY chip with a 25 MHz crystal.

GPIO90 is controlling the PHY RESET# signal. This GPIO has a 2k2 pull-down resistor to GND populated on the module. GPIO90 must be asserted high before PHY can be used. When not used, the PHY can be put in low-power mode by asserting GPIO90 low.

The PHY address on the MII bus is 0x7 (0b00111).

In addition to providing access to the Ethernet signals coming out of the PHY, the module also supports two status LEDs: ETH\_ACTIVITY# and ETH\_LINK#.

### UART

The ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 modules provide up to four UART ports, used in asynchronous mode:

- Port A = GPIO0 through GPIO7
- Port B = GPIO51 through GPIO58
- Port C = GPIO8 through GPIO15
- Port D = GPIO59 through GPIO66

The module supports baud rates up to 1.8432 Mbps in asynchronous mode. Each UART has a 64-byte TX and RX FIFO available.

### SPI

The following interfaces are only available on the ConnectCore 9P 9215 and ConnectCore Wi-9P 9215.

The module provides one SPI port which can be used in either master or slave mode.

- Master: 33.33 Mbps
- Slave: 7.50 Mbps

The SPI module is made of four signals: RXD, TXD, CLK and CS#.

## **I<sup>2</sup>C bus**

The I<sup>2</sup>C bus is completely free on the module - no EEPROM and no RTC - since the RTC is in the processor.

The I<sup>2</sup>C clock is max 400kHz.

I<sup>2</sup>C signals are provided on the module with 4k7 pull-up resistors.

## **RTC**

The RTC is integrated in the processor and has its own 32.768 KHz clock crystal.

- When powered by VBAT, an RTC unit will function until VBAT (X1.78) reaches a threshold of 2.3 - 2.4V - then the internal unit switches off.
- The battery current without +3.3V power applied is up to 40μA. The current is used to power the RTC, 32.768kHz oscillator and 64-byte internal RAM.
- When the Development Board ships from the factory the battery is disabled. To enable the battery, place a jumper on the Development Board at J2.

## **WLAN**

In addition to the wired Ethernet interface, the ConnectCore Wi-9P 9215 module also offers an integrated dual-diversity 802.11a/b/g interface with data rates up to 54 Mbps. Two U.FL antenna connectors are provided on the module.

## **ADC**

The ADC on the module provides 12-bit resolution / 1 MHz conversion capabilities, single-ended 8:1 multiplexed inputs, rail-to-rail input range, 12-bit output (DMA/direct), and external reference.

## **FIM**

The Flexible Interface Modules (FIM) are based on two independent 8-bit DRPIC1655X cores running at 300 MHz maximum core clock (4x NS9215 bus speed) with 192-byte data and 2 KB program SRAM. The FIMs allow the flexible software-based selection of Digi-provided application specific hardware interfaces such as UART, SD/SDIO, 1-Wire, CAN bus, and others.

## **External Address/Data Bus**

The modules provide a 17-bit address and 16-bit data bus with 2 external chip selects for peripheral connections.

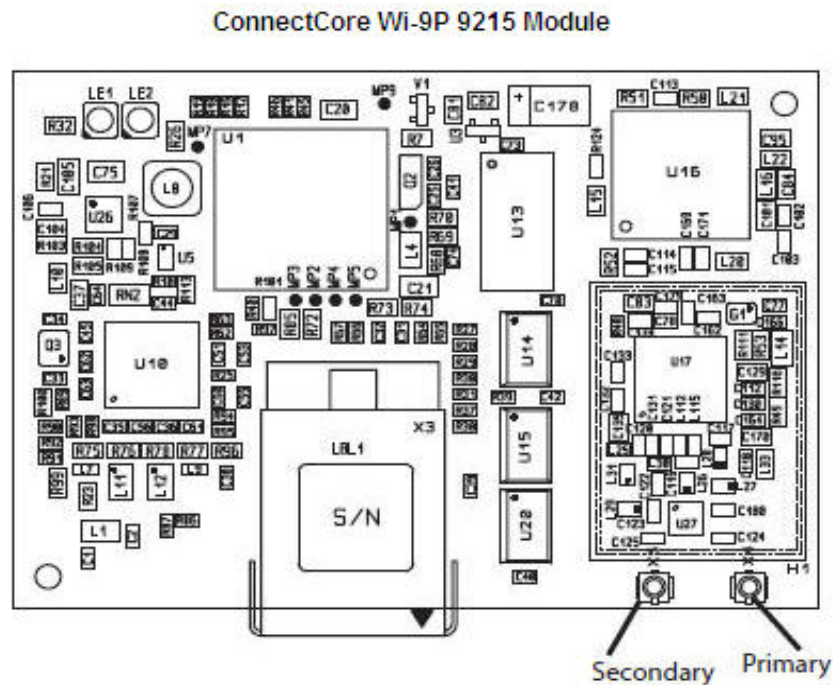
## Antenna

**Note:** When disconnecting U.FL connectors, the use of a U.FL plug extraction tool (Hirose P/N U.FL-LP-N-2 or U.FL-LP(V)-N-2) is strongly recommended to avoid damage to the U.FL connectors on the ConnectCore Wi-9P 9215 module.

To mate U.FL connectors, the mating axes of both connectors must be aligned. The "click" will confirm a fully mated connection.

Do not attempt insertion at an extreme angle.

## ConnectCore Wi-9P 9215 WLAN



For the ConnectCore Wi-9P 9215, connect antennas to the primary and secondary connectors.

The module uses the same antennas to transmit and receive the 802.11b/g RF signal. An antenna switch is required to isolate the transmit signal from the receive signal. The antenna switch works by alternately connecting the antennas to either the transceiver PA transmit output or the transceiver receive input. To support this antenna sharing scheme, the module operates in half-duplex mode; receive and transmit operations do not occur at the same time.

## WLAN Antenna Switch

The antenna switch is a digitally controlled 2.4 GHz, 50 ohm, multi-function solid state switch, controlled by software.

The receive port can be switched between antenna 1 or antenna 2.

The transmit port can be switched between antenna 1 or antenna 2.

The switch can handle >28dBm of signal on the transmit port. The insertion loss of the antenna switch is <0.5dB and the receive to transmit port isolation is >23dB.

## Power

### Power supply

The module has +3.3V and VLIO supply pins.

VLIO can be connected either to a Li-Ion battery (2.5V - 5.5V) in a mobile application, or it can be connected directly to +3.3V. Connecting VLIO to a battery causes efficiency to be gained without an additional voltage regulator.

### Internal voltage

The internal 1.8V core voltage is generated through a high-efficiency synchronous step-down converter, which uses VLIO as input voltage. The core voltage regulator can provide up to 600mA.

## Digi Plug-and-Play Firmware

This section describes the features and functionality of modules utilizing Digi Plug-and-Play Firmware only. If you are using a module that utilizes the embedded NET+OS or Linux software see page 14.

Once you have read through all the Digi Plug-and-Play Firmware related sections, proceed to Chapter 2.

**Note:** Digi Plug-and-Play Firmware is only available for the ConnectCore Wi-9P 9215.

### Module pinout

The module has two 80 pins connectors, X1 and X2. The next tables describe each pin, its properties, and its use on the Development Board.

#### Pinout legend: Type

|     |                 |
|-----|-----------------|
| I   | Input           |
| O   | Output          |
| I/O | Input or output |
| P   | Power           |

#### X1 pinout

| X1 pin number | Type | Module functionality | Comments                                                                          |
|---------------|------|----------------------|-----------------------------------------------------------------------------------|
| 1             | P    | GND                  |                                                                                   |
| 2             | P    | GND                  |                                                                                   |
| 3             | I    | RSTIN#               | 10k pull-up on module                                                             |
| 4             | O    | SRESET#              | Output of the reset controller<br>push pull with 470R current limiting resistor   |
| 5             | O    | RSTOUT#              | Output of logical AND function between NS9215<br>RESET_DONE and NS9215 RESET_OUT# |
| 6             | I    | TCK                  | Not Connected, Reserved                                                           |
| 7             | I    | TMS                  | Not Connected, Reserved                                                           |
| 8             | I    | TDI                  | Not Connected, Reserved                                                           |
| 9             | O    | TDO                  | Not Connected, Reserved                                                           |
| 10            | I    | TRST#                | Not Connected, Reserved                                                           |
| 11            | O    | RTCK                 | Not Connected, Reserved                                                           |
| 12            | I    | OCD_EN#              | Not Connected, Reserved                                                           |

| X1 pin number | Type | Module functionality | Comments                                                                                                                                                                           |
|---------------|------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13            | I    | LITTLE# / BIG ENDIAN | Not Connected, Reserved                                                                                                                                                            |
| 14            | I    | WLAN_DISABLE#        | For ConnectCore Wi-9P 921 low active WLAN Disable signal.<br>For ConnectCore 3G 9P 9215 normally connected to X2-15.                                                               |
| 15            | I    | SW_CONF0             | 2k2 series resistor on module                                                                                                                                                      |
| 16            | I    | SW_CONF1             | 2k2 series resistor on module                                                                                                                                                      |
| 17            | I    | SW_CONF2             | 2k2 series resistor on module                                                                                                                                                      |
| 18            | I    | SW_CONF3             | 2k2 series resistor on module                                                                                                                                                      |
| 19            | O    | (WLAN_LED#)          | Active low signal coming from low-active WLAN signal.<br>This signal comes directly from the Piper chip without series resistor.<br>Not connected, for the ConnectCore 3G 9P 9215. |
| 20            | P    | GND                  |                                                                                                                                                                                    |
| 21            | I/O  | BD0                  | Not Connected, Reserved                                                                                                                                                            |
| 22            | I/O  | BD1                  | Not Connected, Reserved                                                                                                                                                            |
| 23            | I/O  | BD2                  | Not Connected, Reserved                                                                                                                                                            |
| 24            | I/O  | BD3                  | Not Connected, Reserved                                                                                                                                                            |
| 25            | I/O  | BD4                  | Not Connected, Reserved                                                                                                                                                            |
| 26            | I/O  | BD5                  | Not Connected, Reserved                                                                                                                                                            |
| 27            | I/O  | BD6                  | Not Connected, Reserved                                                                                                                                                            |
| 28            | I/O  | BD7                  | Not Connected, Reserved                                                                                                                                                            |
| 29            | I/O  | BD8                  | Not Connected, Reserved                                                                                                                                                            |
| 30            | I/O  | BD9                  | Not Connected, Reserved                                                                                                                                                            |
| 31            | I/O  | BD10                 | Not Connected, Reserved                                                                                                                                                            |
| 32            | I/O  | BD11                 | Not Connected, Reserved                                                                                                                                                            |
| 33            | I/O  | BD12                 | Not Connected, Reserved                                                                                                                                                            |
| 34            | I/O  | BD13                 | Not Connected, Reserved                                                                                                                                                            |
| 35            | I/O  | BD14                 | Not Connected, Reserved                                                                                                                                                            |
| 36            | I/O  | BD15                 | Not Connected, Reserved                                                                                                                                                            |
| 37            | P    | GND                  |                                                                                                                                                                                    |
| 38            | O    | BA0                  | Not Connected, Reserved                                                                                                                                                            |
| 39            | O    | BA1                  | Not Connected, Reserved                                                                                                                                                            |
| 40            | O    | BA2                  | Not Connected, Reserved                                                                                                                                                            |
| 41            | O    | BA3                  | Not Connected, Reserved                                                                                                                                                            |
| 42            | O    | BA4                  | Not Connected, Reserved                                                                                                                                                            |

| X1 pin number | Type | Module functionality | Comments                                                                   |
|---------------|------|----------------------|----------------------------------------------------------------------------|
| 43            | O    | BA5                  | Not Connected, Reserved                                                    |
| 44            | O    | BA6                  | Not Connected, Reserved                                                    |
| 45            | O    | BA7                  | Not Connected, Reserved                                                    |
| 46            | O    | BA8                  | Not Connected, Reserved                                                    |
| 47            | O    | BA9                  | Not Connected, Reserved                                                    |
| 48            | O    | BA10                 | Not Connected, Reserved                                                    |
| 49            | O    | BA11                 | Not Connected, Reserved                                                    |
| 50            | O    | BA12                 | Not Connected, Reserved                                                    |
| 51            | O    | BA13                 | Not Connected, Reserved                                                    |
| 52            | O    | BA14                 | Not Connected, Reserved                                                    |
| 53            | O    | BA15                 | Not Connected, Reserved                                                    |
| 54            | O    | BA16                 | Not Connected, Reserved                                                    |
| 55            | O    | GND                  |                                                                            |
| 56            | O    | EXT_OE#              | Not Connected, Reserved                                                    |
| 57            | O    | EXT_WE#              | Not Connected, Reserved                                                    |
| 58            | O    | EXT_CSO#             | Not Connected, Reserved                                                    |
| 59            | O    | EXT_CS2#             | Not Connected, Reserved                                                    |
| 60            | O    | BE2#                 | Not Connected, Reserved                                                    |
| 61            | O    | BE3#                 | Not Connected, Reserved                                                    |
| 62            | I    | EXT_WAIT#            | Not Connected, Reserved                                                    |
| 63            | O    | EXT_CLK#             | Not Connected, Reserved                                                    |
| 64            | P    | GND                  |                                                                            |
| 65            | I    | ETH_TPIN             |                                                                            |
| 66            | O    | ETH_ACTIVITY#        | Low active signal with 330R resistor on module                             |
| 67            | I    | ETH_TPIP             |                                                                            |
| 68            | O    | ETH_LINK#            | Low active signal with 330R resistor on module                             |
| 69            | O    | ETH_TPON             |                                                                            |
| 70            | O    | ETH_TPOP             |                                                                            |
| 71            | P    | GND                  |                                                                            |
| 72            | P    |                      | Reserved for the ConnectCore 3G 9P 9215: +3.3V additional power supply pin |
| 73            | I    | USB_OC#              | Reserved for the ConnectCore 3G 9P 9215: USB_OC# over current input        |

| X1 pin number | Type | Module functionality | Comments                                                                                |
|---------------|------|----------------------|-----------------------------------------------------------------------------------------|
| 74            | I/O  | USB_P                | Reserved for the ConnectCore 3G 9P 9215: USB_P OTG channel                              |
| 75            | I/O  | USB_N                | Reserved for the ConnectCore 3G 9P 9215: USB_N OTG channel                              |
| 76            | O    | USB_PWR#             | Reserved for the ConnectCore 3G 9P 9215: USB_PWR#                                       |
| 77            | I    | Reserved             |                                                                                         |
| 78            | P    | VRTC                 | Backup Battery for RTC, for 3V cell.<br>Can be left floating, if RTC backup not needed. |
| 79            | P    | VLIO                 | Mobile: Power from Li-Ion Battery (2.5V-5.5V)<br>Non-Mobile: connected to 3.3V          |
| 80            | P    | GND                  |                                                                                         |

## X2 pinout

The following table shows the GPIO multiplexing capabilities for the Digi Plug-and-Play Firmware module:

| X2 pin number | Type | Module Functionality                        | I/O Multiplexing      | Comments              |
|---------------|------|---------------------------------------------|-----------------------|-----------------------|
| 1             | P    |                                             | GND                   |                       |
| 2             | P    |                                             | GND                   |                       |
| 3             | I/O  | DCDA#<br>SPI_EN#<br>GPIO0<br>XBEE_ON_SLEEP# | GPIO0<br>DCDA         | See Note 1            |
| 4             | I/O  | CTSA#<br>GPIO1                              | GPIO1<br>CTSA         | See Note 1            |
| 5             | I/O  | DSRA#<br>GPIO2<br>XBEE_RESET#               | GPIO2<br>DSRA         | See Note 1            |
| 6             | I/O  | RXDA<br>SPI_RXD<br>GPIO3                    | GPIO3<br>RXDA         | See Note 1            |
| 7             | I/O  | RIA#<br>ERIQ2<br>GPIO4                      | GPIO4<br>RIA<br>EIRQ2 | See Note 1 and Note 4 |

| X2 pin number | Type | Module Functionality       | I/O Multiplexing | Comments   |
|---------------|------|----------------------------|------------------|------------|
| 8             | I/O  | RTSA#<br>SPI_CLK<br>GPIO5  | GPIO5<br>RTSA    | See Note 1 |
| 9             | I/O  | DTRA#<br>GPIO6<br>SLEEP_RQ | GPIO6<br>DTRA    | See Note 1 |
| 10            | I/O  | TXDA<br>SPI_TXD<br>GPIO7   | GPIO7<br>TXDA    | See Note 1 |
| 11            | I/O  | DCDC#<br>TXCLKC<br>GPIO8   | GPIO8<br>DCDC    | See Note 2 |
| 12            | I/O  | CTSC#<br>GPIO9             | GPIO9<br>CTSC    | See Note 2 |
| 13            | I/O  | DSRC#<br>GPIO10            | GPIO10<br>DSRC   | See Note 2 |
| 14            | I/O  | RXDC<br>GPIO11             | GPIO11<br>RXDC   | See Note 1 |
| 15            | I/O  | RIC#<br>RXCLKC<br>GPIO12   | GPIO12<br>RIC    | See Note 3 |
| 16            | I/O  | RTSC#<br>RXCLKC<br>GPIO13  | GPIO13<br>RTSC   | See Note 2 |
| 17            | I/O  | DTRC#<br>TXCLKC<br>GPIO14  | GPIO14<br>DTRC   | See Note 1 |
| 18            | I/O  | TXDC<br>GPIO15             | GPIO15<br>TXDC   | See Note 2 |
| 19            | I/O  | DCDB#<br>GPIO51            | GPIO51<br>DCDB   | See Note 1 |
| 20            | I/O  | CTSB#<br>GPIO52            | GPIO52<br>CTSB   | See Note 1 |
| 21            | I/O  | DSRB#<br>GPIO53            | GPIO53<br>DSRB   | See Note 1 |
| 22            | I/O  | RXDB<br>GPIO54             | GPIO54<br>RXDB   | See Note 1 |

| X2 pin number | Type | Module Functionality | I/O Multiplexing         | Comments              |
|---------------|------|----------------------|--------------------------|-----------------------|
| 23            | I/O  | RIB#<br>GPIO55       | GPIO55<br>RIAB           | See Note 1            |
| 24            | I/O  | RTSB#<br>GPIO56      | GPIO56<br>RTSB           | See Note 1            |
| 25            | I/O  | DTRB#<br>GPIO57      | GPIO57<br>DTRB           | See Note 1            |
| 26            | I/O  | TXDB<br>GPIO58       | GPIO58<br>TXDB           | See Note 1            |
| 27            | I/O  | DCDD#<br>GPIO59      | GPIO59<br>DCDD           | See Note 1            |
| 28            | I/O  | CTSD#<br>GPIO60      | GPIO60<br>CTSD           | See Note 1            |
| 29            | I/O  | DSRD#<br>GPIO61      | GPIO61<br>DSRD           | See Note 1            |
| 30            | I/O  | RXDDD<br>GPIO62      | GPIO62<br>RXDD           | See Note 1            |
| 31            | I/O  | RID#<br>GPIO63       | GPIO63<br>RIAD           | See Note 1            |
| 32            | I/O  | RTSD#<br>GPIO64      | GPIO64<br>RTSD           | See Note 1            |
| 33            | I/O  | DTRD#<br>GPIO65      | GPIO65<br>DTRD           | See Note 1            |
| 34            | I/O  | TXDD<br>GPIO66       | GPIO66<br>TXDD           | See Note 1            |
| 35            | I/O  | GPIO67               | GPIO67                   | See Note 1            |
| 36            | I/O  | GPIO68               | GPIO68<br>FIM_UART_0_TXD | See Note 1 and Note 5 |
| 37            | I/O  | GPIO69               | GPIO6<br>FIM_UART_0_RXD  | See Note 1 and Note 5 |
| 38            | I/O  | GPIO70               | GPIO7<br>FIM_UART_0_RTS  | See Note 1 and Note 5 |
| 39            | I/O  | GPIO71               | GPIO71<br>FIM_UART_0_CTS | See Note 1 and Note 5 |
| 40            | I/O  | GPIO72               | GPIO72<br>FIM_UART_1_TXD | See Note 1 and Note 5 |
| 41            | I/O  | GPIO73               | GPIO73<br>FIM_UART_1_RXD | See Note 1 and Note 5 |

| X2 pin number | Type | Module Functionality    | I/O Multiplexing         | Comments                                                |
|---------------|------|-------------------------|--------------------------|---------------------------------------------------------|
| 42            | I/O  | GPIO74                  | GPIO74<br>FIM_UART_1_RTS | See Note 1 and Note 5                                   |
| 43            | I/O  | GPIO75                  | GPIO75<br>FIM_UART_1_CTS | See Note 1 and Note 5                                   |
| 44            | I/O  | GPIO76                  | GPIO76                   | See Note 1                                              |
| 45            | I/O  | GPIO77                  | GPIO77                   | See Note 1                                              |
| 46            | I/O  | GPIO78                  | GPIO78                   | See Note 1                                              |
| 47            | I/O  | GPIO79                  | GPIO79                   | See Note 1                                              |
| 48            | I/O  | GPIO80                  | GPIO80                   | See Note 1                                              |
| 49            | I/O  | USER_BUTTON1#<br>GPIO81 | GPIO81                   | This pin is reserved as a soft reset input, active low. |
| 50            | I/O  | USER_LED1#<br>GPIO82    | GPIO82                   | See Note 1                                              |
| 51            | I/O  | GPIO83                  | GPIO83                   |                                                         |
| 52            | I/O  | USER_BUTTON2#<br>GPIO84 | GPIO84                   | See Note 1                                              |
| 53            | I/O  | USER_LED2#<br>GPIO85    | GPIO85                   |                                                         |
| 54            | I/O  | GPIO86                  | GPIO86                   |                                                         |
| 55            | I/O  | GPIO87                  | GPIO87                   |                                                         |
| 56            | I/O  | GPIO93                  | GPIO93                   |                                                         |
| 57            | I/O  | GPIO94                  | GPIO94                   |                                                         |
| 58            | I/O  | GPIO95                  | GPIO95                   |                                                         |
| 59            | I/O  | CAN0_RXD<br>GPIO96      | CAN_RX0                  | See Note 5                                              |
| 60            | I/O  | CAN0_TXD<br>GPIO97      | CAN_TX0                  | See Note 5                                              |
| 61            | I/O  | CAN1_RXD<br>GPIO98      | CAN_RX1                  | See Note 5                                              |
| 62            | I/O  | CAN1_TXD<br>GPIO99      | CAN_TX1                  | See Note 5                                              |
| 63            | I/O  | GPIO100                 | GPIO100                  | See Note 1                                              |
| 64            | I/O  | EIRQ3#<br>GPIO101       | GPIO101                  | See Note 1                                              |
| 65            | I/O  | I2C_SCL<br>GPIO102      | GPIO102                  | 4k7 pull-up on module                                   |

| X2 pin number | Type | Module Functionality | I/O Multiplexing | Comments                |
|---------------|------|----------------------|------------------|-------------------------|
| 66            | I/O  | I2C_SDA<br>GPIO103   | GPIO103          | 4k7 pull-up on module   |
| 67            | I    | ADC_IN0              | VIN0_ADC         | Not Connected, Reserved |
| 68            | I    | ADC_IN1              | VIN1_ADC         | Not Connected, Reserved |
| 69            | I    | ADC_IN2              | VIN2_ADC         | Not Connected, Reserved |
| 70            | I    | ADC_IN3              | VIN3_ADC         | Not Connected, Reserved |
| 71            | I    | ADC_IN4              | VIN4_ADC         | Not Connected, Reserved |
| 72            | I    | ADC_IN5              | VIN5_ADC         | Not Connected, Reserved |
| 73            | I    | ADC_IN6              | VIN6_ADC         | Not Connected, Reserved |
| 74            | I    | ADC_IN7              | VIN7_ADC         | Not Connected, Reserved |
| 75            | P    | AGND_ADC             | VSS_ADC          | Not Connected, Reserved |
| 76            | P    | VRED_ADC             | VREF_ADC         | Not Connected, Reserved |
| 77            | P    | AGND_ADC             | 3.3V             |                         |
| 78            | P    | VREF_ADC             | 3.3V             |                         |
| 79            | P    |                      | GND              |                         |
| 80            | P    |                      | GND              |                         |

**Note 1:** This pin is defined in the table of the “Multiplexed GPIO Pins” section on page 51.

**Note 2:** For the ConnectCore 3G 9P 9215, the following pins are outputs with fixed functionality, and can be used to drive LEDs:

X2-11: Cellular link activity output.

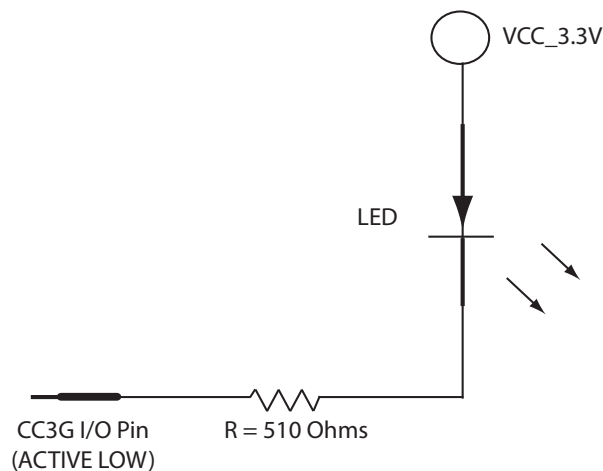
X2-12: Cellular 3G connectivity indicator.

X2-13: Cellular signal strength (1st bar).

X2-16: Cellular signal strength (2nd bar).

X2-18: Cellular signal strength (3rd bar).

These signals are “ACTIVE LOW” and are intended to be used with LEDs to indicate cellular states. It is recommended to connect these IO pins in a “sinking circuit” as indicated in the figure on the next page:



**Note 3:** For the ConnectCore 3G 9P 9215, this pin is the cellular disable output and should be tied directly to CELL\_DISABLE\_N, pin X1-14.

**Note 4:** EIRQ2 is default configured to support the Wake-up button on the Development Board.

**Note 5:** See the “FIM” section on page 56 for more information.

## Configuration pins — Module

### Module pin configuration Dipswitch S4

| Signal name        | Function                  | PU/PD  | Comment                                                                              |
|--------------------|---------------------------|--------|--------------------------------------------------------------------------------------|
| LITTLE#/BIG_ENDIAN | Must be set to BIG_ENDIAN | PU     | Signal LITTLE#/BIG_ENDIAN is connected to GPIO_A3/A27 through a 2k2 series resistor. |
| OCD_EN#            | Not used                  | PU 10K | Not Connected, Reserved                                                              |
| SW_CONF0           | See Note 1                |        | Connected to A13 through a 2k2 series resistor.                                      |
| SW_CONF1           | See Note 1                |        | Connected to A14 through a 2k2 series resistor.                                      |
| SW_CONF2           | See Note 1                |        | Connected to A15 through a 2k2 series resistor.                                      |
| SW_CONF3           | See Note 1                |        | Connected to A16 through a 2k2 series resistor.                                      |

**Note 1:** This pin is defined in the "Connector X2 Pins Available for a Python Application" section, which describes how the setting of this strapping will affect the capabilities of various I/O pins.

### Connector X2 Pins Available for a Python Application

The connector X2 GPIO pins are referenced in Python as the pin number on the X2 connector, not the GPIO number. For example, GPIO67 is connected to connector X2 pin 35. To control GPIO67, you will reference it using "X2\_35".

The ConnectCore 3G 9P 9215 module can be strapped to enable zero to three serial ports. The ConnectCore Wi-9P 9215 and the ConnectCore 9P 9215 modules can be strapped to enable zero to four serial ports. Serial port strapping is defined by the SW\_CONF0, SW\_CONF1, SW\_CONF2 and SW\_CONF3 switch settings on Dipswitch S4 which is next to the JTAG connector. The default is to have two serial ports enabled (Port B and Port D).

If Port A is defined as a serial port, it cannot be used by ZigBee. ZigBee is only available under the following conditions:

1. Port A is not strapped to be a serial port.
2. ZigBee is enabled.

Use Dipswitch S4 to configure the number of serial ports that are enabled. Changes to Dipswitch S4 are only sensed after a hard reset.

| SW_CONF0 | SW_CONF1 | SW_CONF2 | SW_CONF3 | Number of Serial Ports Enabled     |
|----------|----------|----------|----------|------------------------------------|
| OFF      | ON       | ON       | ON       | 0                                  |
| ON       | OFF      | ON       | ON       | 1 - Port B                         |
| ON       | ON       | ON       | ON       | 2 - Port B, Port D (factory)       |
| OFF      | OFF      | ON       | ON       | 3 - Port B, Port D, Port A         |
| ON       | ON       | OFF      | ON       | 4 - Port B, Port D, Port A, Port C |

Four serial ports are only available on the ConnectCore 9P 9215 and ConnectCore Wi-9P 9215.

Serial Port A must not be strapped as a serial port if Wake-up functionality is used. See the “External Interrupts” section on page 54 for more information.

The fewer serial ports enabled, the more GPIO pins available for a Python application.

**Available GPIO pins per number of serial ports enabled**

| Product                                        | 0 Serial Ports | 1 Serial Port | 2 Serial Ports | 3 Serial Ports | 4 Serial Ports |
|------------------------------------------------|----------------|---------------|----------------|----------------|----------------|
| ConnectCore 3G 9P 9215                         | 42             | 34            | 26             | 18             | N/A            |
| ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 | 50             | 42            | 34             | 26             | 18             |

If you are migrating to the ConnectCore 3G 9P 9215 from the ConnectCore Wi-9P 9215 or the ConnectCore 9P 9215, connector pins "X2\_11" - "X2\_18" will no longer be accessible. If you are migrating from the ConnectCore 3G 9P 9215 to the ConnectCore Wi-9P 9215 or the ConnectCore 9P 9215, connector pins "X2\_11" - "X2\_18" will now be accessible.

## Multiplexed GPIO Pins

The table below shows the available GPIOs available through the GPIO Python API.

The first column in the table lists the pin on the module connector. The second column lists the GPIO available when configured for zero serial ports. The third column for one port, and so on.

Some pins have dual purpose, such as GPIO68, which could also be used for EXT\_SIM\_VCC. So if the external SIM function is being used, GPIO68 is not available.

| Module Pin (Python Name) | 0 Serial Ports | 1 Serial Port | 2 Serial Ports | 3 Serial Ports | 4 Serial Ports | Comments                                                                               |
|--------------------------|----------------|---------------|----------------|----------------|----------------|----------------------------------------------------------------------------------------|
| X2-3                     | GPIO0          | GPIO0         | GPIO0          | DCDA           | DCDA           | If XBEE is enabled this signal is not available. Instead, it is used as XBEE_ON_SLEEP. |
| X2-4                     | GPIO1          | GPIO1         | GPIO1          | CTSA           | CTSA           | If XBEE is enabled this signal is not available. Instead, it is used as XBEE_CTS.      |
| X2-5                     | GPIO2          | GPIO2         | GPIO2          | DSRA           | DSRA           | If XBEE is enabled this signal is not available. Instead, it is used as XBEE_DSR.      |
| X2-6                     | GPIO3          | GPIO3         | GPIO3          | RXDA           | RXDA           | If XBEE is enabled this signal is not available. Instead, it is used as XBEE_RXD.      |
| X2-7                     | GPIO4          | GPIO4         | GPIO4          | RIA            | RIA            | If XBEE is enabled this signal is not available. Instead, it is used as XBEE_RI.       |
| X2-8                     | GPIO5          | GPIO5         | GPIO5          | RTSA           | RTSA           | If XBEE is enabled this signal is not available. Instead, it is used as XBEE_RTS.      |

| Module Pin (Python Name) | 0 Serial Ports | 1 Serial Port | 2 Serial Ports | 3 Serial Ports | 4 Serial Ports | Comments                                                                          |
|--------------------------|----------------|---------------|----------------|----------------|----------------|-----------------------------------------------------------------------------------|
| X2-9                     | GPIO6          | GPIO6         | GPIO6          | DTRA           | DTRA           | If XBEE is enabled this signal is not available. Instead, it is used as XBEE_DTR. |
| X2-10                    | GPIO7          | GPIO7         | GPIO7          | TXDA           | TXDA           | If XBEE is enabled this signal is not available. Instead, it is used as XBEE_TXD. |
| X2-11                    | GPIO8          | GPIO8         | GPIO8          | GPIO8          | DCDC           | Cellular link activity output for ConnectCore 3G 9P 9215.                         |
| X2-12                    | GPIO9          | GPIO9         | GPIO9          | GPIO9          | CTSC           | Cellular 3G connectivity indicator for ConnectCore 3G 9P 9215.                    |
| X2-13                    | GPIO10         | GPIO10        | GPIO10         | GPIO10         | DSRC           | Cellular signal strength (1st bar) for ConnectCore 3G 9P 9215.                    |
| X2-14                    | GPIO11         | GPIO11        | GPIO11         | GPIO11         | RXDC           | Not available for ConnectCore 3G 9P 9215.                                         |
| X2-15                    | GPIO12         | GPIO12        | GPIO12         | GPIO12         | RIC            | Not available for ConnectCore 3G 9P 9215.                                         |
| X2-16                    | GPIO13         | GPIO13        | GPIO13         | GPIO13         | RTSC           | Cellular signal strength (2nd bar) for ConnectCore 3G 9P 9215.                    |
| X2-17                    | GPIO14         | GPIO14        | GPIO14         | GPIO14         | DTRC           | Not available for ConnectCore 3G 9P 9215.                                         |
| X2-18                    | GPIO15         | GPIO15        | GPIO15         | GPIO15         | TXDC           | Cellular signal strength (3rd bar) for ConnectCore 3G 9P 9215.                    |
| X2-19                    | GPIO51         | DCDB          | DCDB           | DCDB           | DCDB           |                                                                                   |
| X2-20                    | GPIO52         | CTSB          | CTSB           | CTSB           | CTSB           |                                                                                   |
| X2-21                    | GPIO53         | DSRB          | DSRB           | DSRB           | DSRB           |                                                                                   |
| X2-22                    | GPIO54         | RXDB          | RXDB           | RXDB           | RXDB           |                                                                                   |
| X2-23                    | GPIO55         | RIB           | RIB            | RIB            | RIB            |                                                                                   |
| X2-24                    | GPIO56         | RTSB          | RTSB           | RTSB           | RTSB           |                                                                                   |
| X2-25                    | GPIO57         | DTRB          | DTRB           | DTRB           | DTRB           |                                                                                   |
| X2-26                    | GPIO58         | TXDB          | TXDB           | TXDB           | TXDB           |                                                                                   |
| X2-27                    | GPIO59         | GPIO59        | DCDD           | DCDD           | DCDD           |                                                                                   |
| X2-28                    | GPIO60         | GPIO60        | CTSD           | CTSD           | CTSD           |                                                                                   |
| X2-29                    | GPIO61         | GPIO61        | DSRD           | DSRD           | DSRD           |                                                                                   |
| X2-30                    | GPIO62         | GPIO62        | RXDD           | RXDD           | RXDD           |                                                                                   |
| X2-31                    | GPIO63         | GPIO63        | RID            | RID            | RID            |                                                                                   |

| Module Pin<br>(Python Name) | 0 Serial Ports | 1 Serial Port | 2 Serial Ports | 3 Serial Ports | 4 Serial Ports | Comments     |
|-----------------------------|----------------|---------------|----------------|----------------|----------------|--------------|
| X2-32                       | GPIO64         | GPIO64        | RTSD           | RTSD           | RTSD           |              |
| X2-33                       | GPIO65         | GPIO65        | DTRD           | DTRD           | DTRD           |              |
| X2-34                       | GPIO66         | GPIO66        | TXDD           | TXDD           | TXDD           |              |
| X2-35                       | GPIO67         | GPIO67        | GPIO67         | GPIO67         | GPIO67         |              |
| X2-36                       | GPIO68         | GPIO68        | GPIO68         | GPIO68         | GPIO68         |              |
| X2-37                       | GPIO69         | GPIO69        | GPIO69         | GPIO69         | GPIO69         |              |
| X2-38                       | GPIO70         | GPIO70        | GPUO70         | GPIO70         | GPIO70         |              |
| X2-39                       | GPIO71         | GPIO71        | GPIO71         | GPIO71         | GPIO71         |              |
| X2-40                       | GPIO72         | GPIO72        | GPIO72         | GPIO72         | GPIO72         |              |
| X2-41                       | GPIO73         | GPIO73        | GPIO73         | GPIO73         | GPIO73         |              |
| X2-42                       | GPIO74         | GPIO74        | GPIO74         | GPIO74         | GPIO74         |              |
| X2-43                       | GPIO75         | GPIO75        | GPIO75         | GPIO75         | GPIO75         |              |
| X2-44                       | GPIO76         | GPIO76        | GPIO76         | GPIO76         | GPIO76         |              |
| X2-45                       | GPIO77         | GPIO77        | GPIO77         | GPIO77         | GPIO77         |              |
| X2-46                       | GPIO78         | GPIO78        | GPIO78         | GPIO78         | GPIO78         |              |
| X2-47                       | GPIO79         | GPIO79        | GPIO79         | GPIO79         | GPIO79         |              |
| X2-48                       | GPIO80         | GPIO80        | GPIO80         | GPIO80         | GPIO80         |              |
| X2-50                       | GPIO82         | GIO82         | GPIO82         | GPIO82         | GPIO82         | User LED1    |
| X2-52                       | GPIO84         | GPIO84        | GPIO84         | GPIO84         | GPIO84         | User button2 |
| X2-63                       | GPIO100        | GPIO100       | GPIO100        | GPIO100        | GPIO100        |              |
| X2-64                       | GPIO101        | GPIO101       | GPIO101        | GPIO101        | GPIO101        |              |

## Module LEDs

The ConnectCore 9P 9215, the ConnectCore Wi-9P 9215 and ConnectCore 3G 9P 9215 modules have two on module LEDs: LE1 and LE2. During startup, LE1 will flash a repeating blink pattern for a major system failure; for example, a processor exception or power on self test failure. If startup is successful, you will see three blinks.

After startup, LE1 is available at the Python programming layer, via the `user_led_set()` function if you are using the ConnectCore 9P 9215 or the ConnectCore 3G 9P 9215 module.

After startup, LE1 and LE2 are used as follows for the ConnectCore Wi-9P 9215.

| ID  | Color  | LED              | Blink Pattern | Status/Activity                                                 |
|-----|--------|------------------|---------------|-----------------------------------------------------------------|
| LE1 | Green  | Link Integrity   | On            | The unit is associated to an access point (infrastructure mode) |
|     |        |                  | Slow          | The unit is in ad-hoc mode                                      |
|     |        |                  | Quick         | The unit is scanning for a network                              |
| LE2 | Yellow | Network Activity | Blinking      | Network traffic is received or transmitted                      |
|     |        |                  | Off           | Network is idle                                                 |

## External Interrupts

The Wake-up button can be used to exit from power-save mode. Serial Port A must NOT be strapped as a serial port if Wake-up functionality is used. EIRQ2 is default configured to support the Wake-up button on the Development Board.

## Interfaces

### 10/100 Mbps Ethernet port

The Digi NS9215 processor's 10/100 Mbps Ethernet MAC allows a glueless connection of a 3.3V MII PHY chip that generates the physical Ethernet signals.

The module has a MII PHY chip in a 56-pin QFN package on board. By default, the module does not have a transformer or Ethernet connector; the base board must provide these parts. However, it's possible to populate a specific RJ45 connector with magnetics on the module. The appropriate RJ-45 is Midcom MIC2412A-5108W-LF3.

A PHY clock of 25 MHz is generated in the PHY chip with a 25 MHz crystal.

GPIO90 is controlling the PHY RESET# signal. This GPIO has a 2k2 pull-down resistor to GND populated on the module. GPIO90 must be asserted high before PHY can be used. When not used, the PHY can be put in low-power mode by asserting GPIO90 low.

The PHY address on the MII bus is 0x7 (0b00111).

The module does not only provide access to the Ethernet signals coming out of the PHY, but supports also two status LEDs: ETH\_ACTIVITY# and ETH\_LINK#.

### UART

The ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 modules provide up to four UART ports, the ConnectCore 3G 9P 9215 module provides up to three UART ports, used in asynchronous mode:

- Port A = X2\_3 to X2\_10
- Port B = X2\_19 to X2\_26
- Port C = X2\_11 to X2\_18 (Not available on the ConnectCore 3G 9P 9215)
- Port D = X2\_27 to X2\_34

The module supports baud rates up to 1.8432 Mbps in asynchronous mode. Each UART has a 64-byte TX and RX FIFO available.

For Python applications, the following table shows a cross reference with Python logical programmatic com port (i.e. "com0") to the physical com port (i.e. "Serial Port B").

**Port to Open in Python Applications**

| Product                                        | Serial Port A | Serial Port B | Serial Port C | Serial Port D | FIM 0  | FIM 1  |
|------------------------------------------------|---------------|---------------|---------------|---------------|--------|--------|
| ConnectCore 3G 9P 9215                         | "com2"        | "com0"        | N/A           | "com1"        | "com3" | "com4" |
| ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 | "com2"        | "com0"        | "com3"        | "com1"        | "com4" | "com5" |

## RTC

The RTC is integrated in the processor and has its own 32.768 KHz clock crystal.

- When powered by VBAT, RTC unit will function until VBAT (X1.78) reaches a threshold of 2.3 - 2.4V - then the internal unit switches off.
- The battery current without +3.3V power applied is up to 40µA. The current is used to power the RTC, 32.768kHz oscillator and 64-byte internal RAM.
- When the Development Board ships from the factory the battery is disabled. To enable the battery, place a jumper on the Development Board at J2.

## WLAN

In addition to the wired Ethernet interface, the ConnectCore Wi-9P 9215 module also offers an integrated dual-diversity 802.11a/b/g interface with data rates up to 54 Mbps. Two U.FL antenna connectors are provided on the module.

## WWAN

The ConnectCore 3G 9P 9215 offers 3G connection technologies by using the Qualcomm Gobi PCIe module.

## FIM

The Flexible Interface Modules (FIM) are based on two independent 8-bit DRPIC1655X cores running at 300 MHz maximum core clock (4x NS9215 bus speed) with 192-byte data and 2 KB program SRAM. The FIMs allow the flexible software-based selection of Digi-provided application specific hardware interfaces such as UART, SD/SDIO, 1-Wire, CAN bus, and others.

To use the FIMS (Flexible Interface Modules) for CAN bus or additional serial ports, you will be using the FIM Application Kit. The FIM application kit is not supplied with the development kit. You need to purchase "Product: Application Kit - FIM". There are two available FIMs that can be used in combinations of CAN bus and serial port(s).

The FIM Application Kit provides interfaces to test the different firmware implemented on the FIMs of the ConnectCore 3G 9P 9215, ConnectCore Wi-9P 9215 and ConnectCore 9P 9215 modules. The FIMs are 8-bit microcontrollers embedded in the main microcontroller of the modules.

The current implementation does not support dual CAN bus. CAN bus is only supported on FIM0, and can only be accessed using Python. Both Serial FIM0 and Serial FIM1 can be used for additional serial ports. The ports can only be accessed using Python. For more detailed information, see the links below:

- FIM Application Kit Quick Start Guide:  
[http://ftp1.digi.com/support/documentation/90001076\\_A.pdf](http://ftp1.digi.com/support/documentation/90001076_A.pdf)

- FIM Application Kit Hardware Reference Manual:  
[http://ftp1.digi.com/support/documentation/90001074\\_A.pdf](http://ftp1.digi.com/support/documentation/90001074_A.pdf)
- FIM Application Kit Schematics:  
[http://ftp1.digi.com/support/documentation/90001104\\_A.pdf](http://ftp1.digi.com/support/documentation/90001104_A.pdf)

### USB Host

The ConnectCore 3G 9P 9215 has a high speed USB Host controller, capable of handling external mass storage devices (i.e., USB Flash Drivers) or a Digi Watchport Camera.

### Antenna

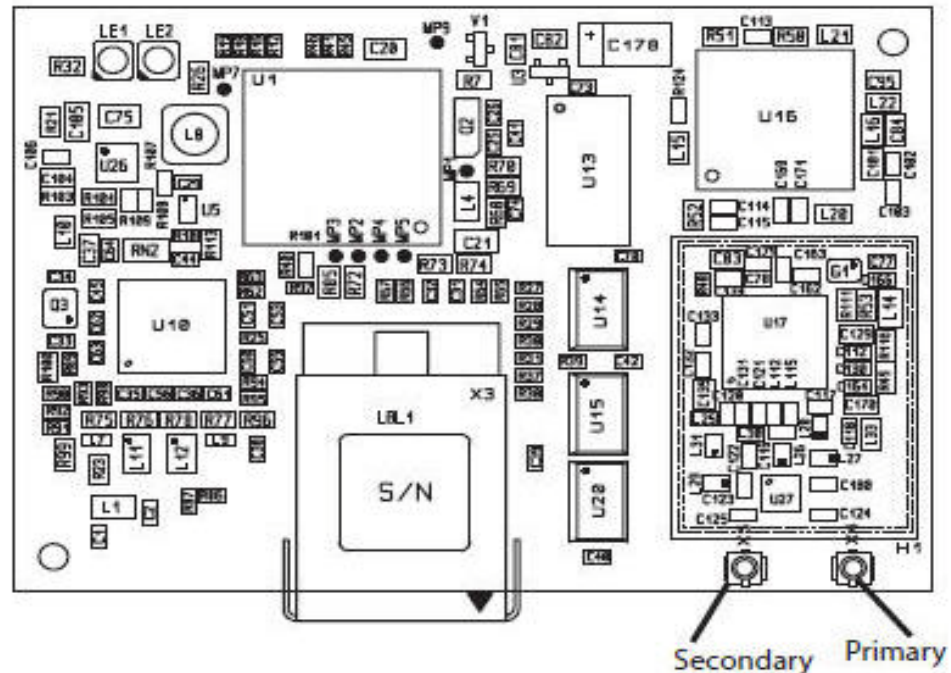
**Note:** When disconnecting U.FL connectors, the use of U.FL plug extraction tool (Hirose P/N U.FL-LP-N-2 or U.FL-LP(V)-N-2) is strongly recommended to avoid damage to the U.FL connectors on the ConnectCore Wi-9P 9215 and ConnectCore 3G 9P 9215 modules.

To mate U.FL connectors, the mating axes of both connectors must be aligned. The "click" will confirm fully mated connection.

Do not attempt insertion at an extreme angle.

## ConnectCore Wi-9P 9215 WLAN

### ConnectCore Wi-9P 9215 Module



For the ConnectCore Wi-9P 9215, connect antennas to the primary and secondary connectors.

The module uses the same antennas to transmit and receive the 802.11b/g RF signal. An antenna switch is required to isolate the transmit signal from the receive signal. The antenna switch works by alternately connecting the antennas to either the transceiver PA transmit output or the transceiver receive input. To support this antenna sharing scheme, the module operates in half-duplex mode; receive and transmit operations do not occur at the same time.

### WLAN Antenna Switch

The antenna switch is a digitally controlled 2.4 GHz, 50 ohm, multi-function solid state switch, controlled by software.

The receive port can be switched between antenna 1 or antenna 2.

The transmit port can be switched between antenna 1 or antenna 2.

The switch can handle >28dBm of signal on the transmit port. The insertion loss of the antenna switch is <0.5dB and the receive to transmit port isolation is >23dB.

### ConnectCore 3G 9P 9215 WWAN

The ConnectCore 3G 9P 9215 Development Board and module contains several RF connectors, as well as the two connectors located on the Gobi 3000 module (refer to the diagrams on the following page).

**Cellular RF Path:** The cellular RF path is established when the Gobi 3000 module MAIN connector is cabled directly to the back of the ConnectCore 3G 9P 9215 J2 connector. The cellular antenna is connected to J2.

**Note:** This is how the module is certified and any deviation from this configuration will require re-certification.)

**GPS RF Path:** The GPS RF path has two possible configurations, based on the GPS antenna: Active and Passive. Digi supplies an Active antenna.

When using an active GPS antenna, the Gobi 3000 module AUX connector is cabled to the ConnectCore 3G 9P 9215 X30 connector, and the ConnectCore 3G 9P 9215 X29 connector is cabled to the Development Board Cellular Secondary connector X31. When an Active GPS antenna is connected to the Development Board at J7, GPS traffic is then available to the module.

When using a Passive GPS antenna, the Gobi 3000 AUX connector could be cabled directly to the Development Board Cellular Secondary connector X31. A Passive GPS antenna is connected at J7.

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- 
- 
- 
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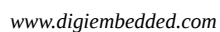


### X30 (GPS) from Gobi AUX

### X29 (GPS)

**J2 (WWAN)**

## 60



### Power

#### Power supply

The module has +3.3V and VLIO supply pins.

VLIO can be connected either to a Li-Ion battery (2.5V - 5.5V) in a mobile application, or it can be connected directly to +3.3V. Connecting VLIO to a battery causes efficiency to be gained without an additional voltage regulator.

#### Internal voltage

The internal 1.8V core voltage is generated through a high-efficiency synchronous step-down converter, which uses VLIO as input voltage. The core voltage regulator can provide up to 600mA.

# About the Development Board

## C H A P T E R 2

The ConnectCore 9P 9215 Development Board supports the onnectCore 9P 9215 Family of modules. This chapter describes the components of the Development Board and explains how to configure the board for your requirements.

The Development Board has two 4x20 pin connectors that are 1:1 copies of the module pins.

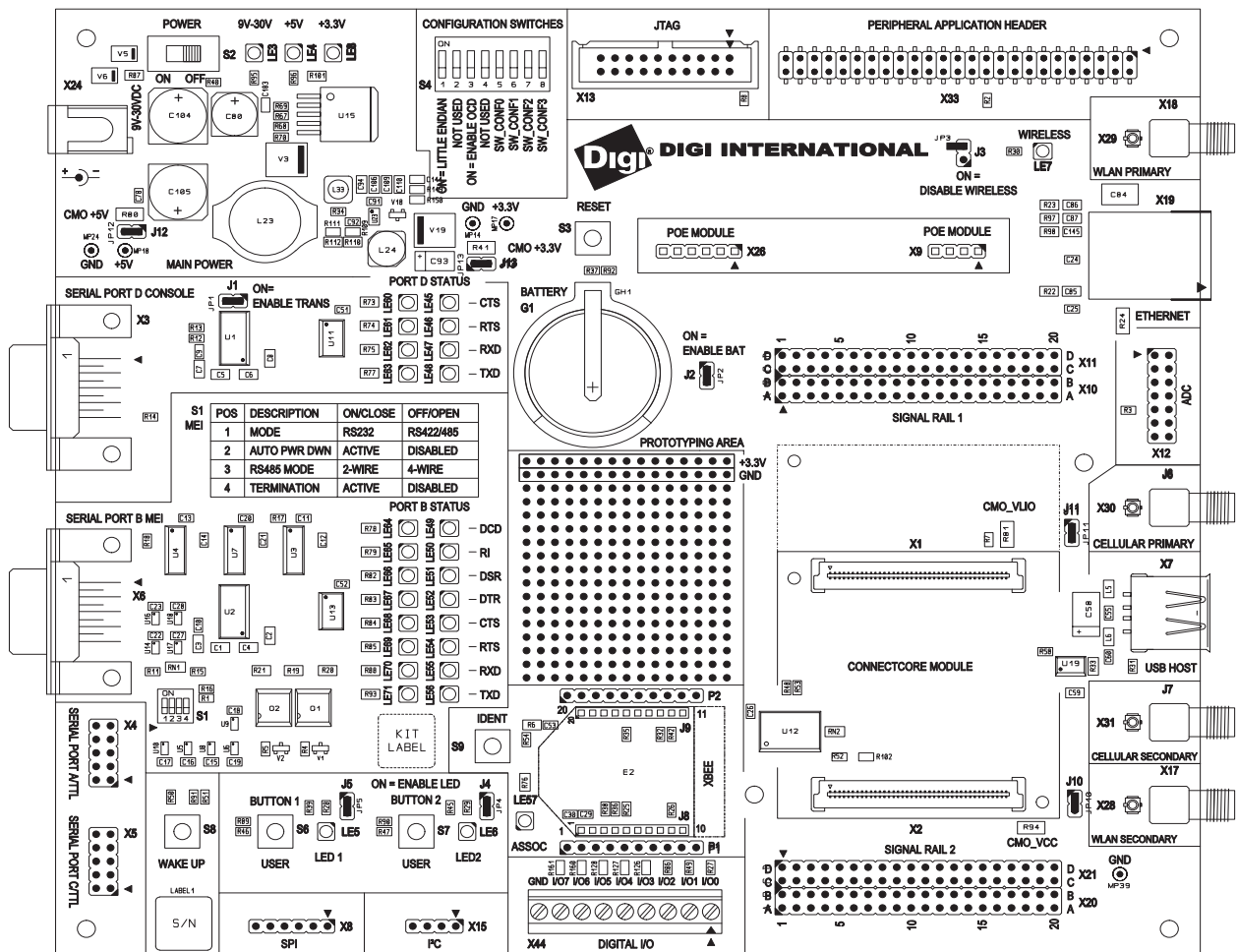
### What's on the Development Board?

- RJ-45 Ethernet connector
- Four RP-SMA antenna connectors.
  - Connection to module via U.FL connectors
- Four serial interface connectors:
  - 1 x UART B MEI (RS232/RS4xx) with status LEDs on SUB-D 9-pin connector (X6)
  - 1 x UART D RS232 with status LEDs, on SUB-D 9-pin connector (X3)
  - 1 x UART C with TTL levels shared with HDLC signals on 10-pin header (X5)
  - 1 x UART A with TTL levels shared with SPI signals on 10-pin header (X4)
- Socket for XBee<sup>®</sup> module
- Peripheral application header
  - Including access to 16-bit data/10-bit address bus signals
- Headers with 1:1 copies of the module pins (X1/X2)
- Two user pushbuttons, two user LEDs, one wake-up button
- Eight-position configuration dip switches

- ## ConnectCore 3G 9P 9215 Specifics

- ### Connection to module via U.FL connectors

## ConnectCore 9P 9215 Development Board



# User interface

The ConnectCore 9P 9215 Development Board implements two user buttons and two user LEDs, in addition to those provided on the module.

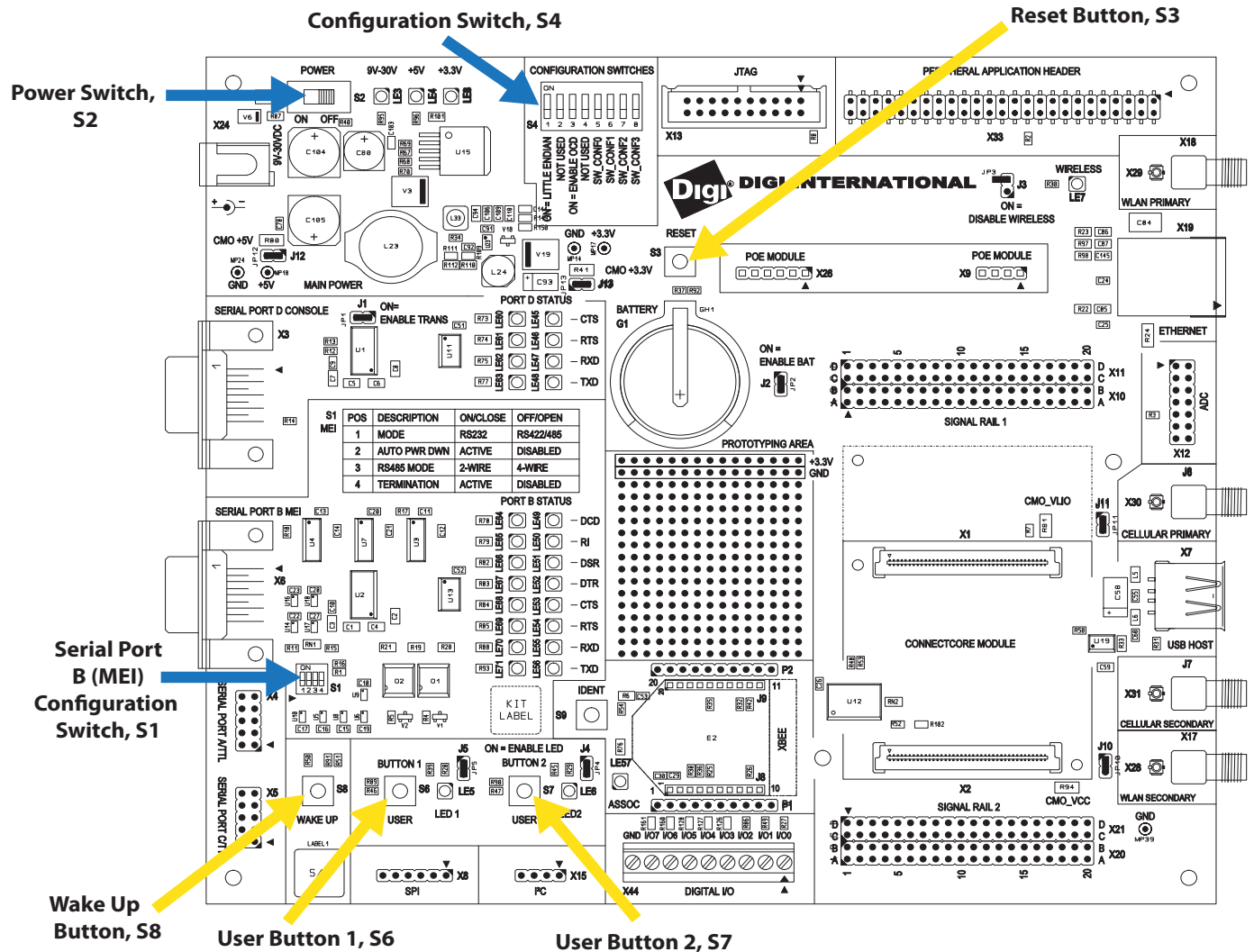
The user LEDs on the Development Board can be enabled or disabled by population option jumper J4 & J5.

The table below shows which NS9215 GPIO is available for implementing the user interface.

| Signal name  | GPIO used | Comments                                            |
|--------------|-----------|-----------------------------------------------------|
| USER_BUTTON1 | GPIO81    | 10k pull-up to +3.3V on the Development Board       |
| USER_LED1#   | GPIO82    | Remove jumper J5 to isolate (and disable) LED (LE5) |
| USER_BUTTON2 | GPIO84    | 10k pull-up to +3.3V on the Development Board       |
| USER_LED2#   | GPIO85    | Remove jumper J4 to isolate (and disable) LED (LE6) |

## Switches and Pushbuttons

### ConnectCore 9P 9215 Development Board



#### Reset control, S3

The reset pushbutton, S3, resets the module. On the module, RSTOUT# and PWRGOOD are produced for peripherals. A pushbutton allows manual reset by connecting RSTIN# to ground.

#### Power switch, S2

The Development Board has an ON/OFF switch, S2. The power switch, S2, can switch both 9V-30V input power supply and 12V coming out of the PoE module. However, if a power plug is connected in the DC power jack, the PoE module is disabled.

### User pushbuttons, S6 and S7

Use the user pushbuttons to interact with the applications running on the ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 modules. Use these module signals to implement the pushbuttons:

| Signal name        | Switch (pushbutton) | GPIO used |
|--------------------|---------------------|-----------|
| USER_PUSH_BUTTON_1 | S6                  | GPIO81    |
| USER_PUSH_BUTTON_2 | S7                  | GPIO84    |

**Note:** User Button 1 has reserved functionality. A quick button press causes a soft reset. Holding the button at power-up for 20 seconds, then releasing, will factory default the module.

### Legend for multi-pin switches

Switches 1 and 4 are multi-pin switches. In the description tables for these switches, the pin is designated as *S[switch number].[pin number]*. For example, pin 1 in switch 4 is specified as S4.1.

### Module configuration switches, S4

Use S4 to configure the module:

| Switch pin  | Function                                     |
|-------------|----------------------------------------------|
| S4.1        | On = Little endian<br>Off = Big endian       |
| S4.2        | Not used                                     |
| S4.3        | On = ARM Debug<br>Off = Boundary Scan        |
| S4.4        | Not used                                     |
| S4.5 – S4.8 | Used for application configuration settings. |

**Note:** When running Linux based applications, always select Little Endian. All other applications must use Big Endian. Failure to do so will prevent your board from running or booting.

### Wake-up button, S8

The wake-up pushbutton, S8, generates an external interrupt to the module's NS9215 processor using the EIRQ2 signal.

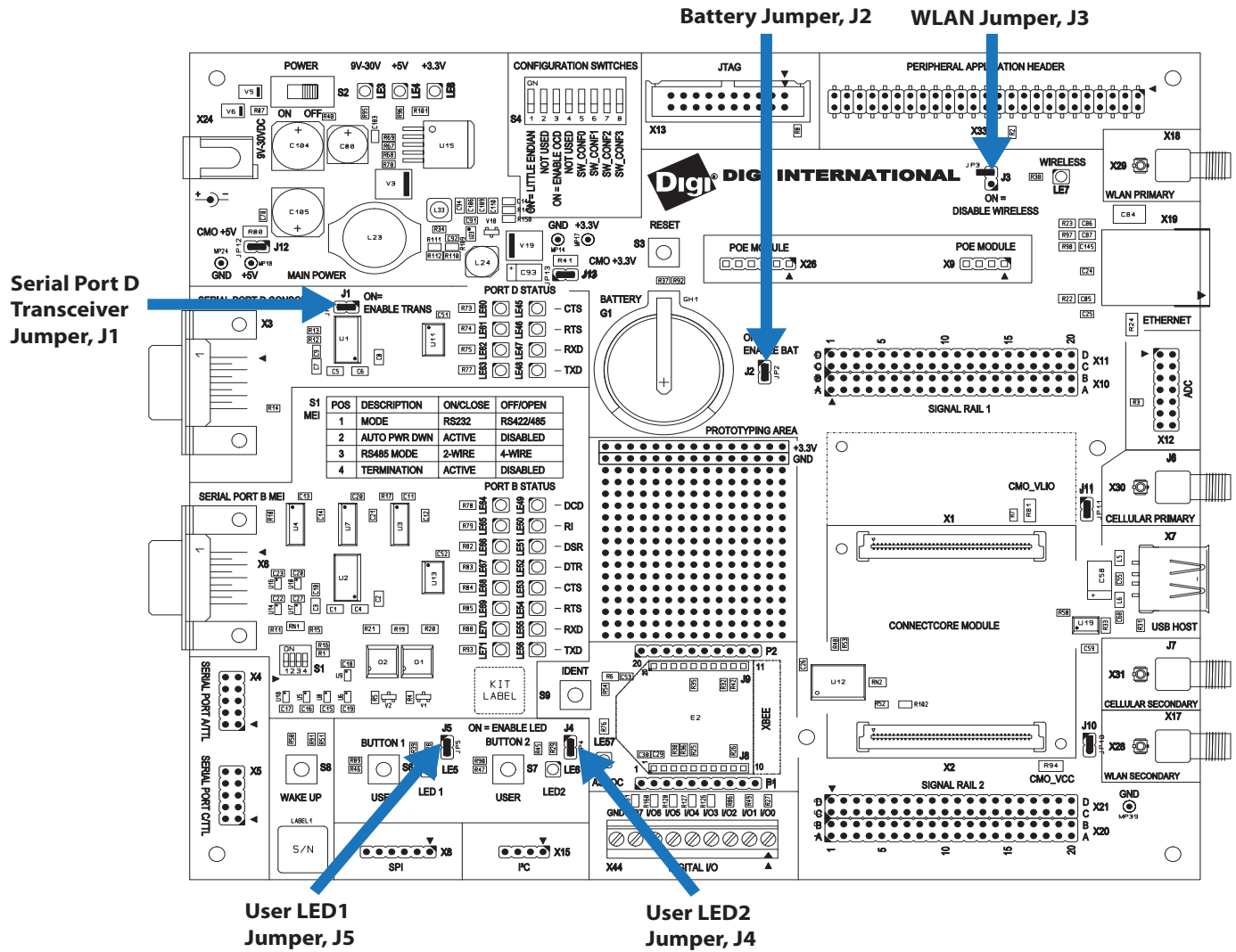
## Serial Port B MEI configuration switches, S1

Use S1 to configure the line interface for serial port B MEI:

| Switch pin | Function                                                                                                                                    | Comments                                                                                                                                                                                                                                                                                                                                                     |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| S1.1       | On = RS232 transceiver enabled<br>RS422/RS485 transceivers disabled<br>Off = RS232 transceiver disabled<br>RS422/RS485 transceivers enabled |                                                                                                                                                                                                                                                                                                                                                              |
| S1.2       | On = Auto Power Down enabled<br>Off = Auto Power Down disabled                                                                              | Auto Power Down is not supported on this board. This signal is only accessible to permit the user to completely disabled the MEI interface for using the signals for other purposes. To disable the MEI interface, go into RS232 mode (S1.1 = ON) and activate the Auto Power Down feature (S1.2 = ON) - be sure that no cable is connected to connector X3. |
| S1.3       | On = 2-wire interface (RS422/RS485)<br>Off = 4-wire interface (RS422)                                                                       |                                                                                                                                                                                                                                                                                                                                                              |
| S1.4       | On = Termination on<br>Off = No termination                                                                                                 |                                                                                                                                                                                                                                                                                                                                                              |

# Jumpers

## ConnectCore 9P 9215 Development Board



## Jumper functions

| Jumper | Name               | If connection made                                                                                                                                            | Default                                       |
|--------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|
| J1     | Enable transceiver | This jumper allows a user to disable the console RS232 transceiver.                                                                                           | Connection made = console active              |
| J2     | Battery enable     | Supplies the real time clock with 3V from the battery (lithium coin cell battery, G1) even if the board is switched off. This is for keeping time in the RTC. | Connection not made = Backup battery disabled |
| J3     | WLAN_DISABLE#      | Disables the WiFi unit on the module.                                                                                                                         | Connection made = WLAN disabled               |
| J4     | USER_LED2#         | Enables User LED2 (LE6) to show the status of this signal (lit if low).                                                                                       | Connection made = User LED2 enabled           |
| J5     | USER_LED1#         | Enables User LED1 (LE5) to show the status of this signal (lit if low).                                                                                       | Connection made = User LED1 enabled           |

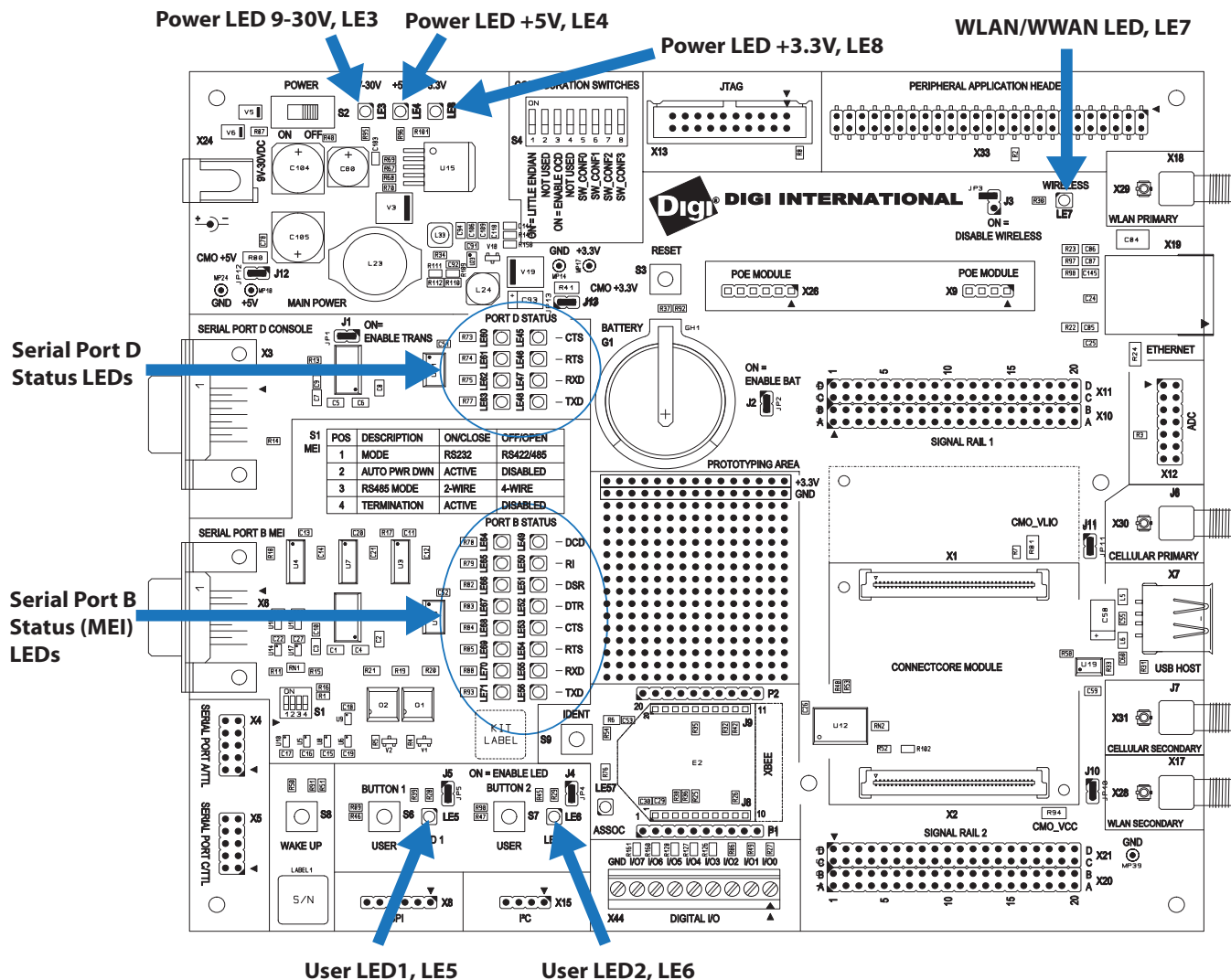
**Note:** The User LEDs are specific to the ConnectCore 3G 9P 9215 module:  
 USER\_LED2 - indicated GPS lock  
 USER\_LED1 - available through the Python GPIO API

## Battery and Battery Holder

| Battery Holder                           | Battery                                 |
|------------------------------------------|-----------------------------------------|
| Coin-Cell Holder for CR2477 Battery, THT | Lithium coin cell, CR2477, 24mm, 950mAh |
| Keystone 1025-7                          | Panasonic CR2477                        |
| Ettinger 15.61.252                       | Renata CR2477N                          |

## LEDs

### ConnectCore 9P 9215 Development Board



## WLAN LED LE7

LED indicating WLAN activity.

ConnectCore 3G 9P 9215 - LED indicating WWAN activity (directly connected to the PCIe connector pin 42).

## Power LEDs, LE3 and LE4

The power LEDs are all red LEDs. These power supplies must be present and cannot be switched:

- LE3 ON indicates the +9VDC / +30VDC power is present.
- LE4 ON indicates the +5VDC power is present.

- LE8 ON indicates the +3.3VDC power is present.

## User LEDs, LE5 and LE6

The user LEDs are controlled through applications running on the ConnectCore 9P 9215 Family of modules, if jumpers J5 and J4 are inserted. Use these module signals to implement the LEDs:

| Signal name | LED | GPIO used |
|-------------|-----|-----------|
| USER_LED1#  | LE5 | GPIO82    |
| USER_LED2#  | LE6 | GPIO85    |

**Note:** On the ConnectCore 3G 9P 9215, USER\_LED2 is reserved for the GPS lock indication.

## Serial status LEDs

The Development Board has two sets of serial port LEDs — four for serial port D and eight for serial port B. The LEDs are connected to the TTL side of the RS232 or RS422/485 transceivers.

- Green means corresponding signal high.
- Red means corresponding signal low.
- The intensity and color of the LED will change when the voltage is switching.

## Status LEDs Serial Port D LEDs

| LED reference |       | Function     |
|---------------|-------|--------------|
| RED           | GREEN |              |
| LE60          | LE45  | CTSD#/GPIO60 |
| LE61          | LE46  | RTSD#/GPIO64 |
| LE62          | LE47  | RXDD/GPIO62  |
| LE63          | LE48  | TXDD/GPIO66  |

## Status LEDs Serial Port B LEDs

| LED reference |       | Function     |
|---------------|-------|--------------|
| RED           | GREEN |              |
| LE64          | LE49  | DCDB#/GPIO51 |
| LE65          | LE50  | RIB#/GPIO55  |
| LE66          | LE51  | DSRB#/GPIO53 |
| LE67          | LE52  | DTRB#/GPIO57 |
| LE68          | LE53  | CTSB#/GPIO52 |

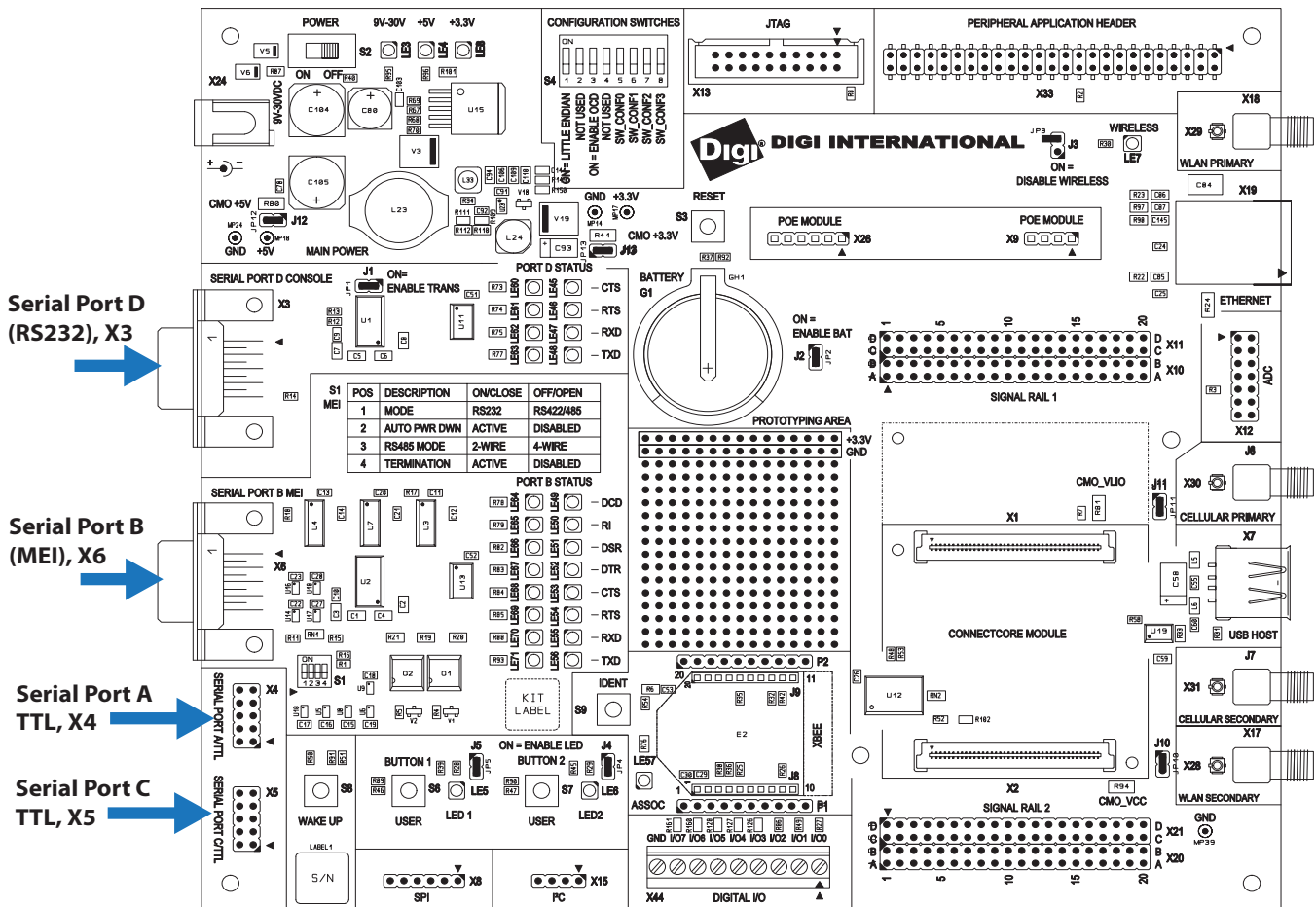
| LED reference |      | Function     |
|---------------|------|--------------|
| LE69          | LE54 | RTSB#/GPIO56 |
| LE70          | LE55 | RXDB/GPIO54  |
| LE71          | LE56 | TXDB/GPIO58  |

**Note:** For more information please see the ConnectCore 9P 9215 schematics document online.

## Serial UART Ports

The Development Board supports the four serial ports available on the ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 modules, including the three serial ports available on the Connect Core 3G 9P 9215. (ConnectCore 9P 9215 Port C is not available on the Connect Core 3G 9P 9215.)

### ConnectCore 9P 9215 Development Board



### Serial port D, RS232

The serial (UART) port D connector, X3, is a DB9 male connector and is also used as the standard console. This asynchronous serial port is DTE and requires a null-modem cable to connect to a computer serial port.

The serial port D interface corresponds to NS9215 UART port D. The line driver is enabled or disabled using jumper J1.

Serial port D pins are allocated as shown:

| Pin | Function | Connector X2 Pin | Defaults to |
|-----|----------|------------------|-------------|
| 1   | DCD#     | X2_27            | GPIO59      |
| 2   | RXD      | X2_30            | GPIO62      |
| 3   | TXD      | X2_34            | GPIO66      |
| 4   | DTR#     | X2_33            | GPIO65      |
| 5   | GND      |                  |             |
| 6   | DSR#     | X2_29            | GPIO61      |
| 7   | RTS#     | X2_32            | GPIO64      |
| 8   | CTS#     | X2_28            | GPIO60      |
| 9   | RIB#     | X2_31            | GPIO63      |

By default, Serial D signals are configured to their respective GPIO signals.

It is the responsibility of the driver to configure them properly.

### Serial port A, TTL interface

The serial (UART) port A interface is a TTL interface connected to a 2x5 pin, 0.1" connector, X4. The connector supports only TTL level.

The serial port A interface corresponds to NS9215 UART port A.

Serial port A pins are allocated as shown:

| Pin | Function      | Connector X2 Pin | Defaults to | Comment                                                                                    |
|-----|---------------|------------------|-------------|--------------------------------------------------------------------------------------------|
| 1   | DCDA#/SPI_EN# | X2_3             | GPIO0       | Can be programmed as SPI enable to X4                                                      |
| 2   | DSRA#         | X2_5             | GPIO2       |                                                                                            |
| 3   | RXDA/SPI_RXD  | X2_6             | GPIO3       | Can be programmed as SPI receive data to X4                                                |
| 4   | RTSA#/SPI_CLK | X2_8             | GPIO5       | Can be programmed as SPI clock to X4                                                       |
| 5   | TXDA/SPI_TXD  | X2_10            | GPIO7       | Can be programmed as SPI transmit data to X4                                               |
| 6   | CTSA#         | X2_4             | GPIO1       |                                                                                            |
| 7   | DTRA#         | X2_9             | GPIO6       |                                                                                            |
| 8   | RIA#/EIRQ2    | X2_7             | GPIO4       | This signal is default configured to support the wake-up button on the Development Board.. |

| Pin | Function | Connector<br>X2 Pin | Defaults<br>to | Comment |
|-----|----------|---------------------|----------------|---------|
| 9   | GND      |                     |                |         |
| 10  | 3.3V     |                     |                |         |

By default, Serial A signals are configured to their respective GPIO signals. It is the responsibility of the driver to configure them properly.

Serial port A must not be connected if SPI, WakeUp, or XBee module functionality is used.

### Serial port A, XBee socket

The XBee socket consists of two separate connectors J8 and J9. The XBee pinning counts counter-clockwise, so pin 1 of J9 is pin 20 of the module. All pins are connected 1:1 to a pin row to enable the usage of unconnected pins.

| Pin | Function                               | Connector<br>X2 Pin | Defaults to | Comments                                      |
|-----|----------------------------------------|---------------------|-------------|-----------------------------------------------|
| 1   | VCC                                    |                     |             | Onboard 3.3V                                  |
| 2   | RXDA/SPI_RXD/GPIO3                     | X2_6                | GPIO3       | Can be programmed as SPI receive data to X4   |
| 3   | TXDA/SPI_TXD/GPIO7                     | X2_10               | GPIO7       | Can be programmed as SPI transmit data to X4  |
| 4   | NC                                     |                     |             |                                               |
| 5   | DSRA#/GPIO2/<br>XBEE_RESET#            | X2_5                | GPIO2       |                                               |
| 6   | NC                                     |                     |             |                                               |
| 7   | NC                                     |                     |             |                                               |
| 8   | NC                                     |                     |             |                                               |
| 9   | DTRA#/GPIO6/SLEEP_RQ                   | X2_9                | GPIO6       |                                               |
| 10  | GND                                    |                     |             |                                               |
| 11  | NC                                     |                     |             |                                               |
| 12  | CTSA#/GPIO01                           | X2_4                | GPIO1       |                                               |
| 13  | DCDA#/SPI_EN#/GPIO0/<br>XBEE_ON_SLEEP# | X2_3                | GPIO0       |                                               |
| 14  | NC                                     |                     |             |                                               |
| 15  | ASSOC                                  |                     | ASSOC       | LED output of XBEE module (LE57 on dev-board) |
| 16  | RTSA#/SPI_CLK/GPIO5                    | X2_8                | GPIO5       | Can be programmed as SPI clock on X4          |

| Pin | Function | Connector X2 Pin | Defaults to | Comments                     |
|-----|----------|------------------|-------------|------------------------------|
| 17  | NC       |                  |             |                              |
| 18  | NC       |                  |             |                              |
| 19  | NC       |                  |             |                              |
| 20  | IDNET    |                  | IDENT       | Connected to S9 on dev-board |

### Serial port C, TTL interface

The serial (UART) port C interface is a TTL interface connected to a 2x5 pin, 0.1" connector, X5. The connector supports only TTL level.

The serial port C interface corresponds to the NS9215 UART port C. The signals are shared with the HDLC interface.

Serial port C pins are allocated as shown:

| Pin | Function            | Connector X2 Pin | Defaults to           | Comments |
|-----|---------------------|------------------|-----------------------|----------|
| 1   | DCDC#/TXCLKC        | X2-11            | GPIO8.                |          |
| 2   | DSRC#               | X2-13            | GPIO10.               |          |
| 3   | RXDC#               | X2-14            | GPIO11                |          |
| 4   | RTSC#/RXCLKC        | X2-16            | GPIO13                |          |
| 5   | TXDC                | X2-18            | GPIO15                |          |
| 6   | CTSC#               | X2-12            | GPIO9                 |          |
| 7   | DTRC#/TXCLKC        | X2-17            | GPIO14                |          |
| 8   | RIC#/RXCLKC/GPIO 12 | X2-15            | RESET_DONE (see note) |          |
| 9   | GND                 |                  |                       |          |
| 10  | 3.3V                |                  |                       |          |

**Note:** If using GPIO12 as RIC#, be sure to populate a series resistor on the Development Board. This is necessary to avoid conflict between the default configuration of the GPIO when booting (RESET\_DONE / output) and the chosen configuration once booted (RIC# / input).

By default, Serial C signals are configured to their respective GPIO signals, except for GPIO12. It is the responsibility of the driver to configure them properly.

## Serial port B, MEI interface

The serial (UART) port B connector, X6, is a DB9 male connector. This asynchronous serial port is DTE and requires a null-modem cable to connect to a computer serial port.

The serial port B MEI (Multiple Electrical Interface) interface corresponds to NS9215 UART port B. The line drivers are configured using switch S1.

Note that all pins on S1 contribute to the line driver settings for this port.

Serial port B pins are allocated as shown:

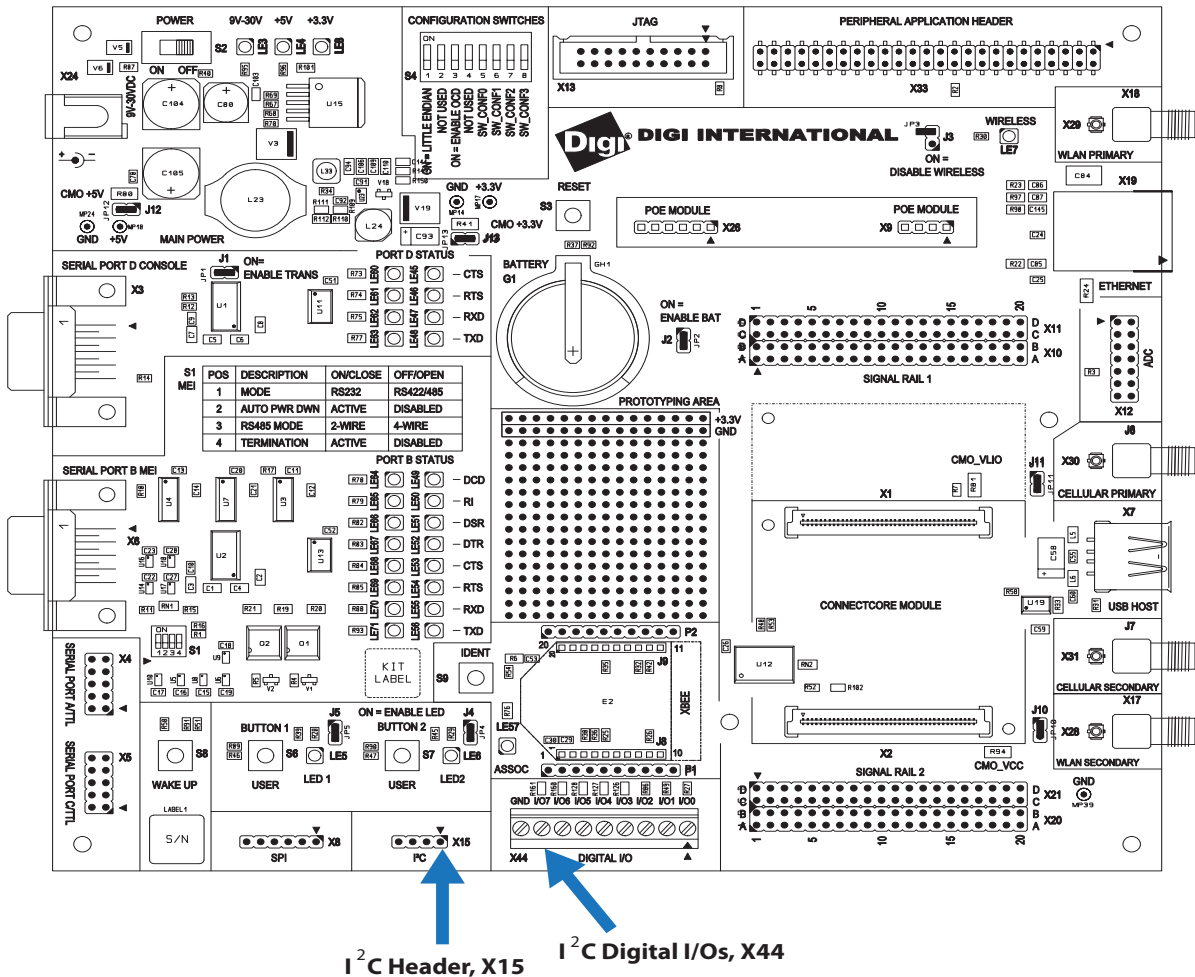
| Pin | RS232<br>function | RS232<br>default | Connector X2<br>Pin | RS485<br>function | RS485<br>default |
|-----|-------------------|------------------|---------------------|-------------------|------------------|
| 1   | DCD#              | GPIO51           | X2-19               | CTS-              | n/a              |
| 2   | RXD               | GPIO54           | X2-22               | RX+               | GPIO54           |
| 3   | TXD               | GPIO58           | X2-26               | TX+               | GPIO58           |
| 4   | DTR#              | GPIO57           | X2-25               | RTS-              | n/a              |
| 5   | GND               |                  |                     | GND               |                  |
| 6   | DSR#              | GPIO53           | X2-21               | RX-               | n/a              |
| 7   | RTS#              | GPIO56           | X2-24               | RTS+              | GPIO56           |
| 8   | CTS#              | GPIO52           | X2-20               | CTS+              | GPIO52           |
| 9   | RI#               | GPIO55           | X2-23               | TX-               | n/a              |

By default, Serial B signals are configured to their respective GPIO signals.

It is the responsibility of the driver to configure them properly.

# I<sup>2</sup>C Interface

## ConnectCore 9P 9215 Development Board



## I<sup>2</sup>C header

The I<sup>2</sup>C interface has only one device connected to the bus on the Development Board - an I/O expander (see next paragraph). Otherwise, additional I<sup>2</sup>C devices (like EEPROMs) can be connected to the module by using I<sup>2</sup>C header X15. The pinning of this header is provided as follows:

| Pin | Signal          |
|-----|-----------------|
| 1   | I2C_SDA/GPIO103 |
| 2   | +3.3V           |
| 3   | I2C_SCL/GPIO102 |
| 4   | GND             |

### I<sup>2</sup>C digital I/O expansion

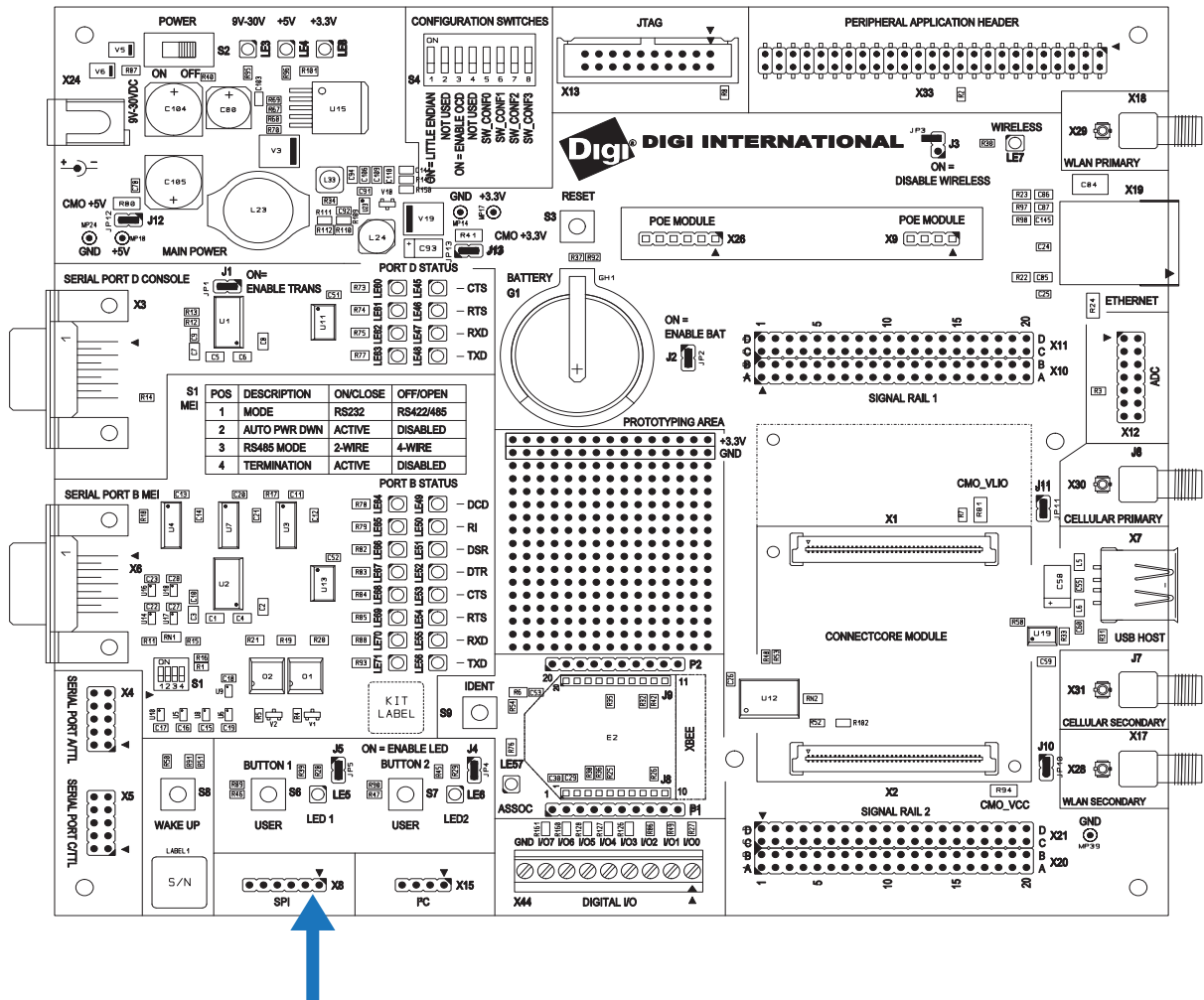
The Development Board provides a 3.81mm (1.50") green terminal block, X44, for additional digital I/Os. The I<sup>2</sup>C I/O port chip is on-chip ESD-protected, and provides an open drain interrupt output.

The I/O expander is a Philips PCA9554D at I<sup>2</sup>C address 0x20 / 0x21. The pins are allocated as shown:

| Pin | Signal |
|-----|--------|
| 1   | IO_0   |
| 2   | IO_1   |
| 3   | IO_2   |
| 4   | IO_3   |
| 5   | IO_4   |
| 6   | IO_5   |
| 7   | IO_6   |
| 8   | IO_7   |
| 9   | GND    |

.....

## ConnectCore 9P 9215 Development Board



## SPI Header, X8

The Development Board provides access to the SPI interface on the module using the SPI connector, X8. The SPI interface on the Development Board is shared with UART\_A (NS9215 port A). Since the module's SPI interface is shared with a UART interface, you cannot use both simultaneously.

**Note:** The default configuration of UART Port A is to support GPIOs. To move from GPIO to UART or SPI, you need to configure the software properly.

## Pin allocation

SPI connector pins are allocated as shown:

| Pin | Signal              |
|-----|---------------------|
| 1   | +3.3V               |
| 2   | TXDA/SPI_TXD/GPIO7  |
| 3   | RXDA/SPI_RXD/GPIO3  |
| 4   | RTSA#/SPI_CLK/GPIO5 |
| 5   | DCDA#/SPI_EN#/GPIO0 |
| 6   | GND                 |

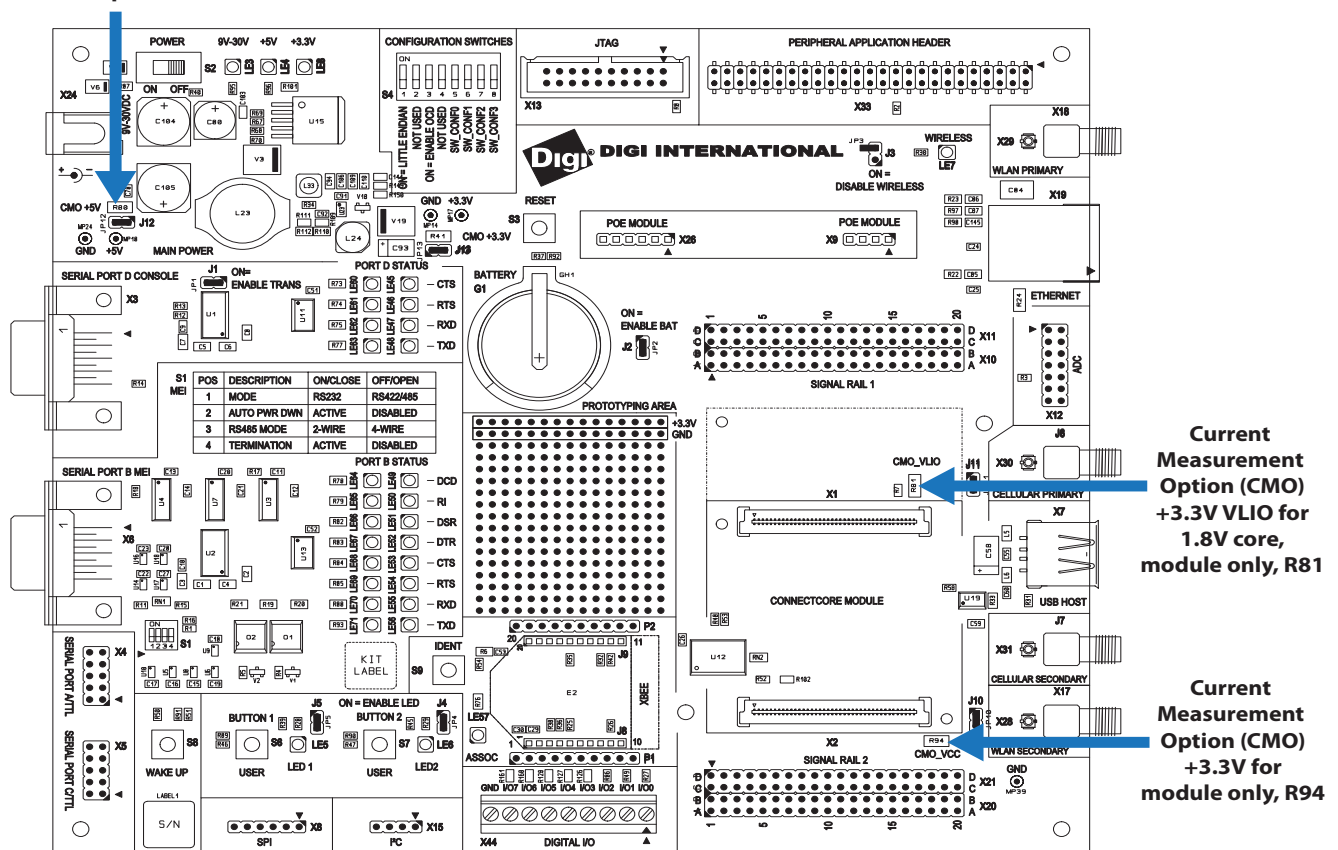
.....

The Current Measurement Option uses 0.025R ohm series resistors to measure the current. The ConnectCore 9P 9215 Development Board allows a user to measure:

- the current used by the Development Board and module (through R80), and
- the current used by the internal NS9215 1.8V core generated from VLIO using a high-efficiency synchronous step-down converter (through R81)

## ConnectCore 9P 9215 Development Board

### Current Measurement Option (CMO) +3.3V development board and module, R80



## How the CMO works

To measure the load current used on different power supplies, measure DC voltage across the sense (CMO) resistor. The value of the resistor is  $0.025R \pm 1\%$ . Calculate the current using this equation:  $I = U/R$

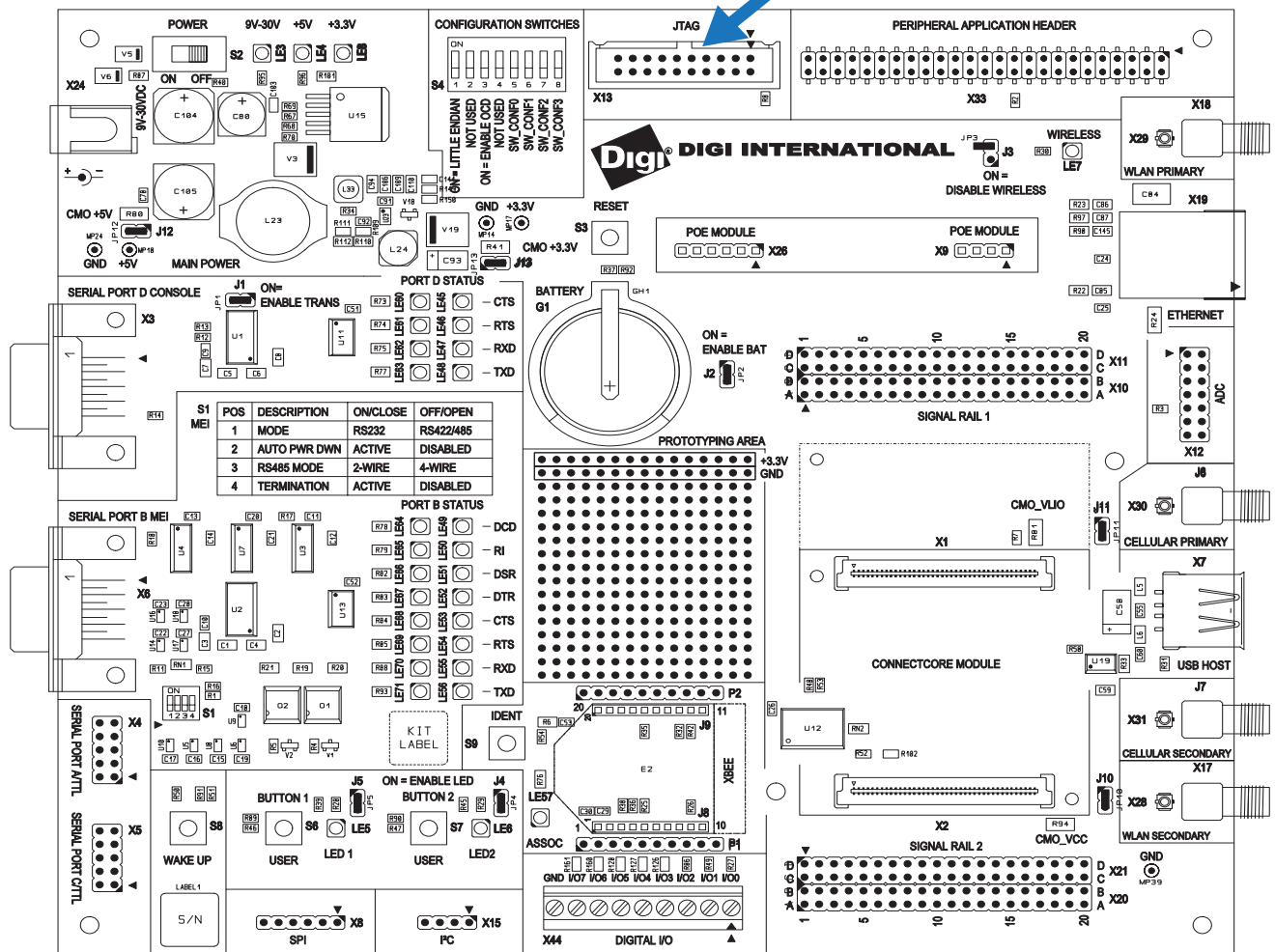
where

- I = current in Amps
- U = measured voltage in Volts
- R = 0.025 Ohms

# JTAG Interface

## ConnectCore 9P 9215 Development Board

JTAG Multi-Ice Connector, X13



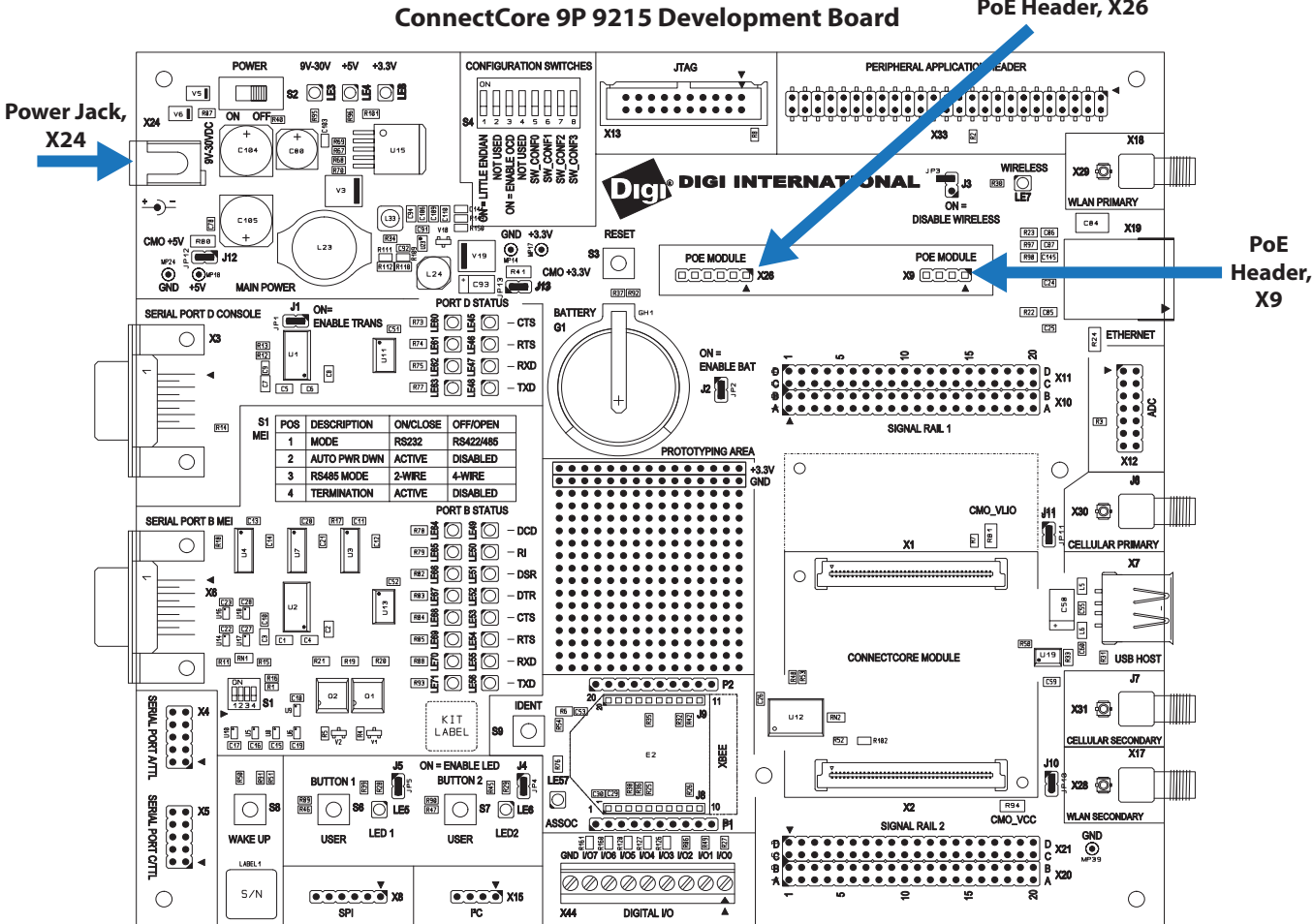
### Standard JTAG ARM connector, X13

The standard JTAG ARM connector is a 20-pin header and can be used to connect development tools such as Digi's JTAG Link, ARM's Multi-ICE, Abatron BDI2000, and others.

| Pin | Signal          | Pin | Signal |
|-----|-----------------|-----|--------|
| 1   | +3.3V           | 2   | +3.3V  |
| 3   | TRST#           | 4   | GND    |
| 5   | TDI             | 6   | GND    |
| 7   | TMS             | 8   | GND    |
| 9   | TCK             | 10  | GND    |
| 11  | RTCK (optional) | 12  | GND    |
| 13  | TDO             | 14  | GND    |
| 15  | SRESET#         | 16  | GND    |
| 17  | No connect      | 18  | GND    |
| 19  | No connect      | 20  | GND    |

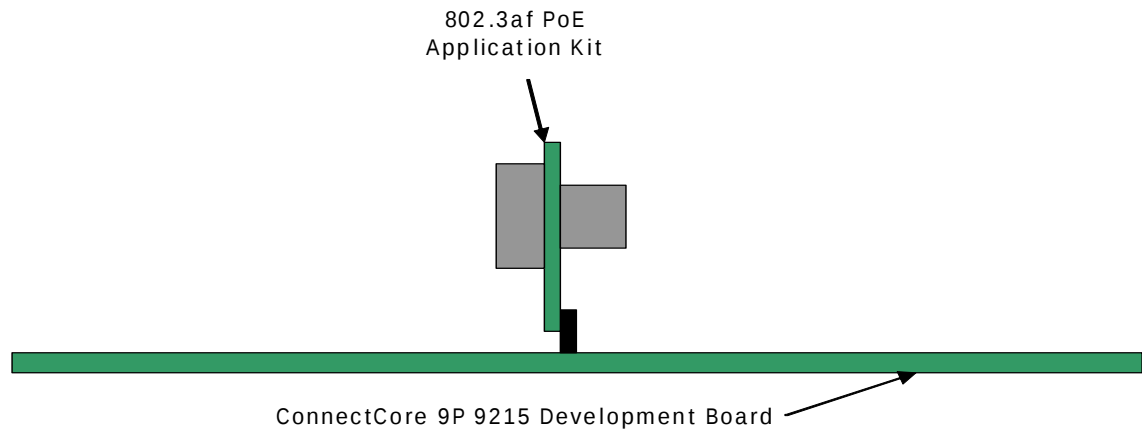
.....

- X9, input connector: Provides access to the PoE signals coming from the Ethernet interface.
- X26, output connector: Provides the output power supply from the PoE module.



## The 802.3af PoE Application Kit

Plug in the 802.3af PoE Application Kit (P/N DG-ACC-POE) at a right angle to the Development Board, as shown in the following drawing:



### X9

PoE input connector pins are allocated as shown:

| Pin | Signal       |
|-----|--------------|
| 1   | POE_TX_CT    |
| 2   | POE_RX_CT    |
| 3   | POE_RJ45_4/5 |
| 4   | POE_RJ45_7/8 |

### X26

PoE output connector pins are allocated as shown:

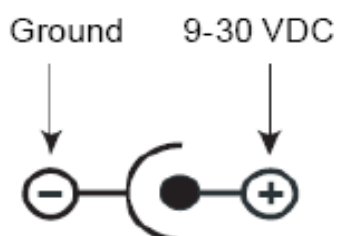
| Pin | Signal   |
|-----|----------|
| 1   | +12V_PoE |
| 2   | +12V_PoE |
| 3   | GND      |
| 4   | GND      |
| 5   | PoE_GND  |
| 6   | PoE_GND  |

## POE\_GND

The Development Board provides access to POE\_GND allowing it to be turned off when power is provided through the power jack, X26.4 and X26.5.

## Power Jack, X24

The power jack is a barrel connector with 9-30VDC operating range. The power jack is labeled X24 on the Development Board. The following figure schematically represents the power jack's polarity.

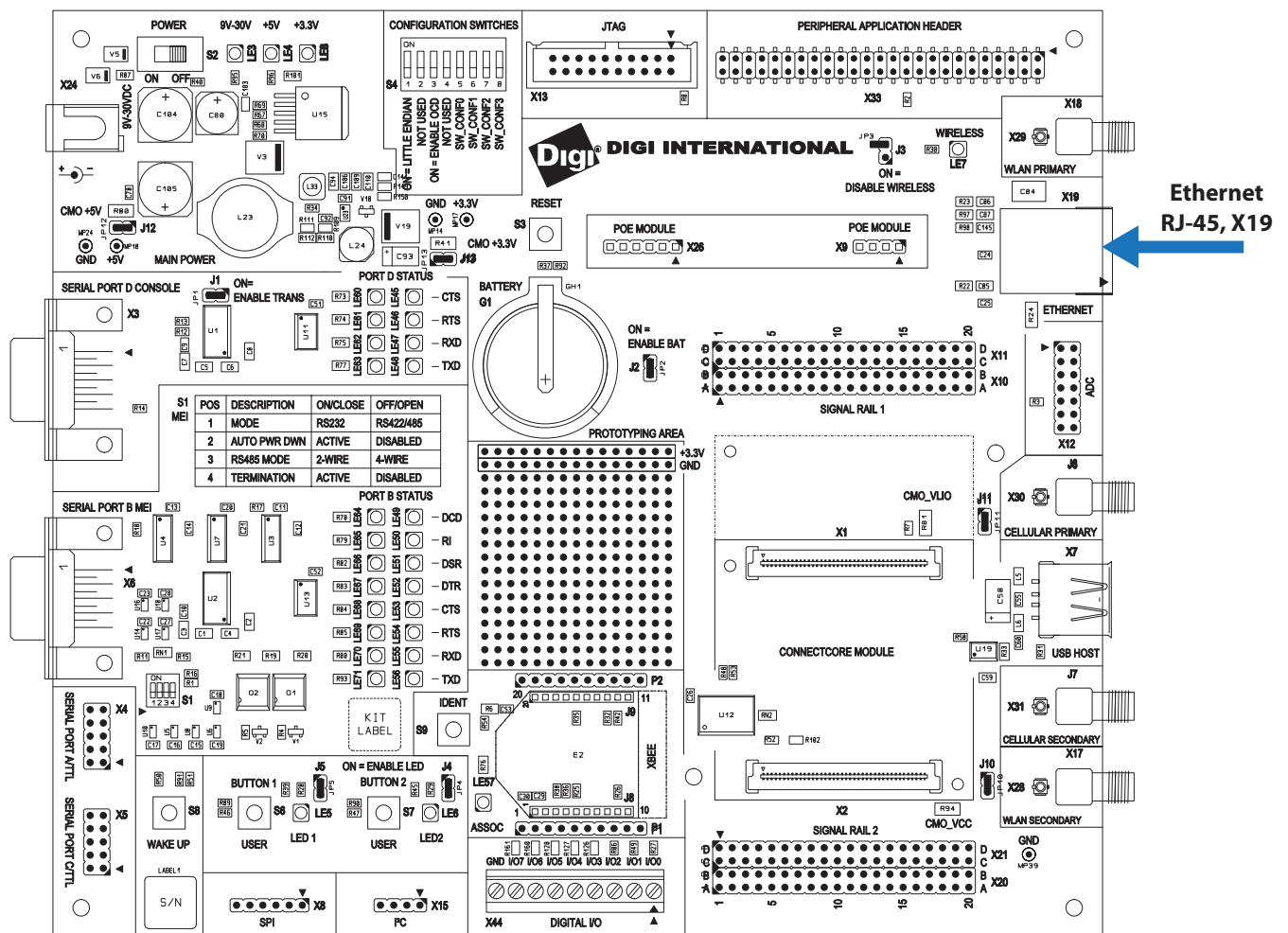


## Ethernet Interface

The module provides the 10/100 Ethernet PHY chip. The Development Board provides the 1:1 transformer and Ethernet connector.

The Ethernet connector is an 8-wire RJ-45 jack, labeled X19 on the Development Board. The connector has eight interface pins, as well as two integrated LEDs that provide link status and network activity information.

### ConnectCore 9P 9215 Development Board



### RJ-45 pin allocation, X19

RJ-45 connector pins are allocated as shown:

| Pin | Signal | 802.3af End-Span (Mode A) | 802.3af Mid-Span (Mode B) | Description         |
|-----|--------|---------------------------|---------------------------|---------------------|
| 1   | TXD+   | Negative $V_{Port}$       |                           | Transmit data +     |
| 2   | TXD-   | Negative $V_{Port}$       |                           | Transmit data -     |
| 3   | RXD+   | Positive $V_{Port}$       |                           | Receive data +      |
| 4   | EPWR+  |                           | Positive $V_{Port}$       | Power from switch + |
| 5   | EPWR+  |                           | Positive $V_{Port}$       | Power from switch + |
| 6   | RXD-   | Positive $V_{Port}$       |                           | Receive data -      |
| 7   | EPWR-  |                           | Negative $V_{Port}$       | Power from switch - |
| 8   | EPWR-  |                           | Negative $V_{Port}$       | Power from switch - |

### LEDs

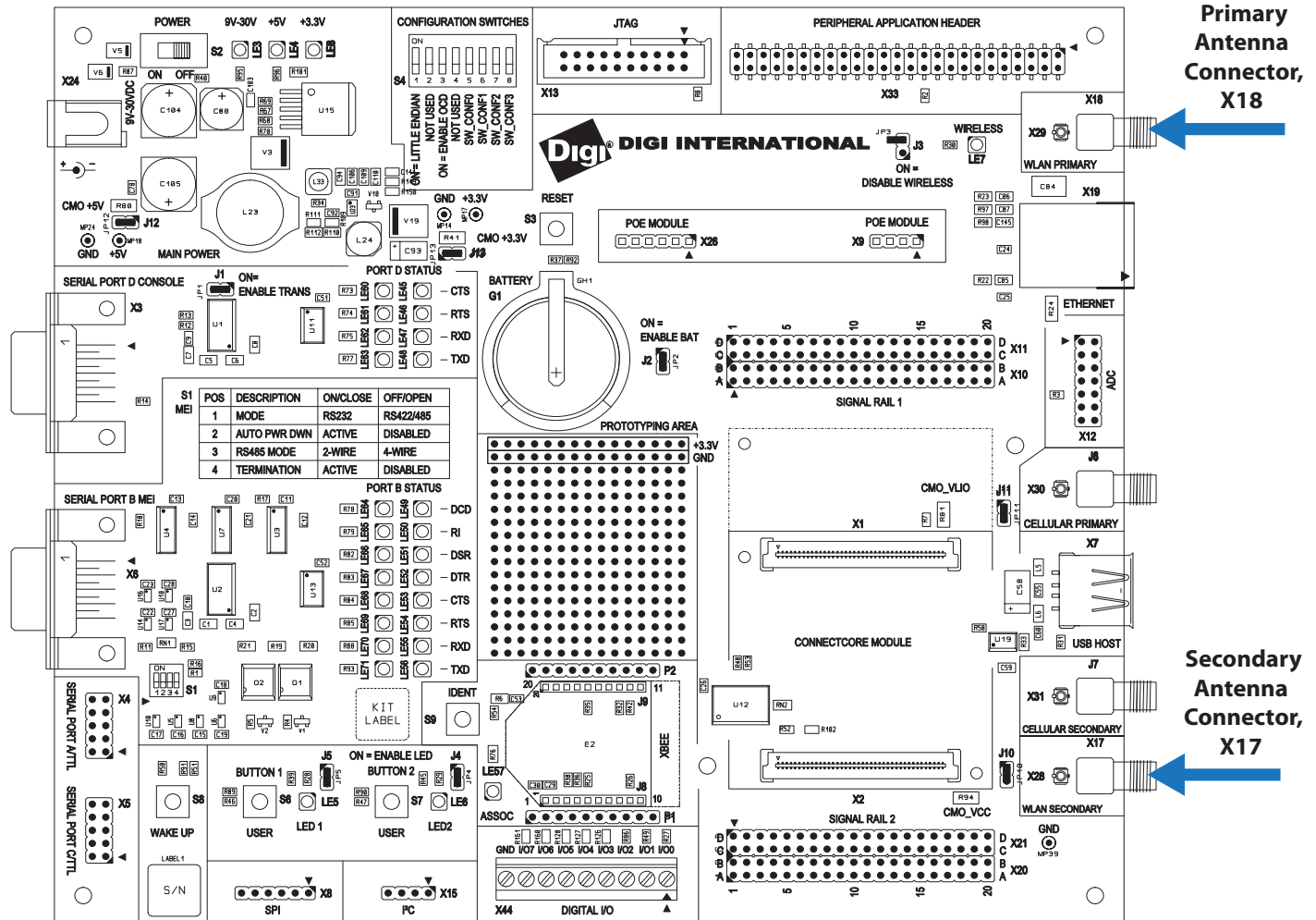
The RJ-45 connector has two LEDs located near the outer lower corners of the connector. These LEDs are not programmable.

| LED    | Description                                                                                             |
|--------|---------------------------------------------------------------------------------------------------------|
| Yellow | Network activity (speed): Flashing when network traffic detected; Off when no network traffic detected. |
| Green  | Network link: On indicates an active network link; Off indicates that no network link is present.       |

## WLAN Interface

For the ConnectCore Wi-9P 9215, attach the antenna to the primary connector [X18] and the secondary connector [X17] on the Development Board (see the figure below for details).

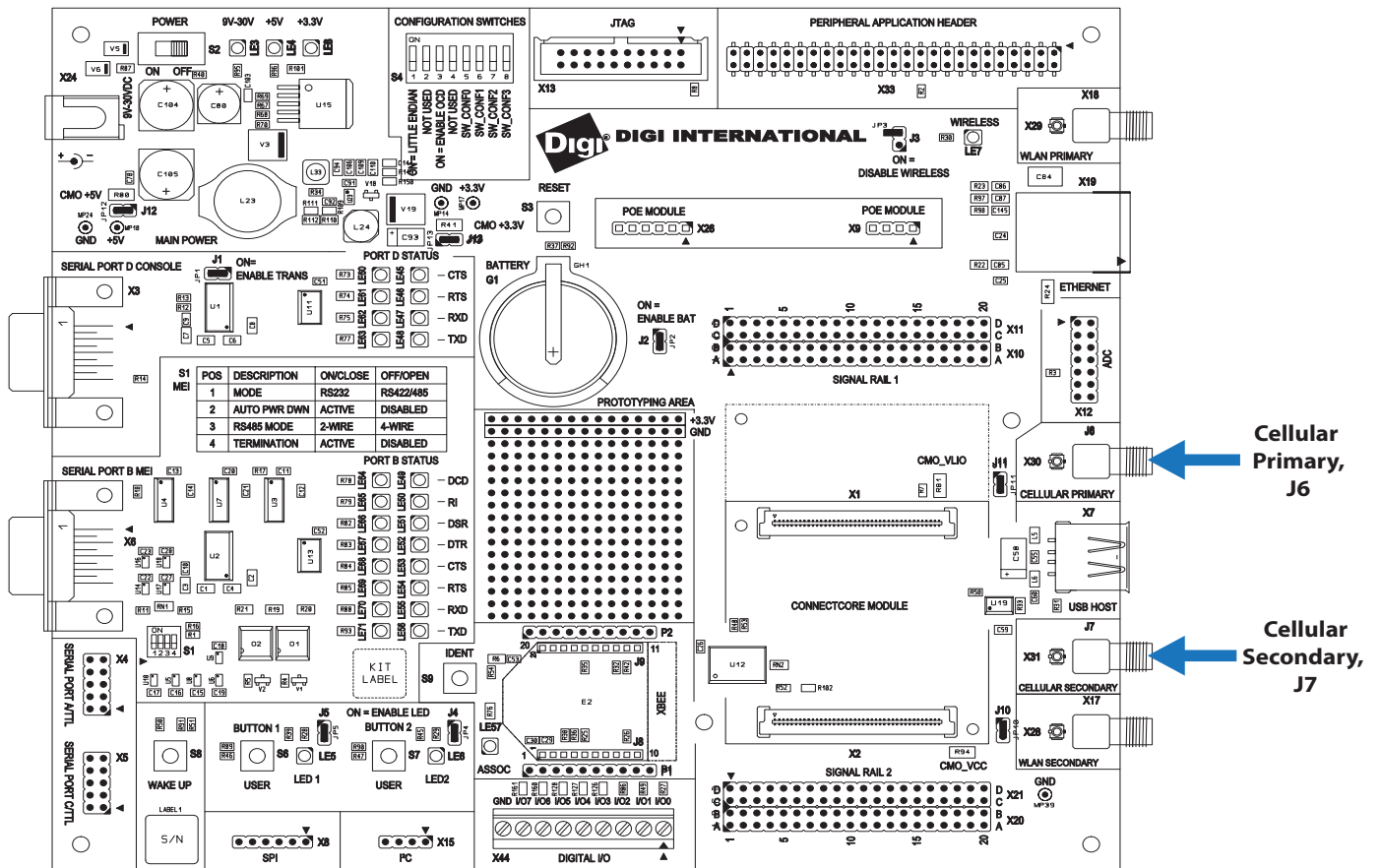
**ConnectCore 9P 9215 Development Board**



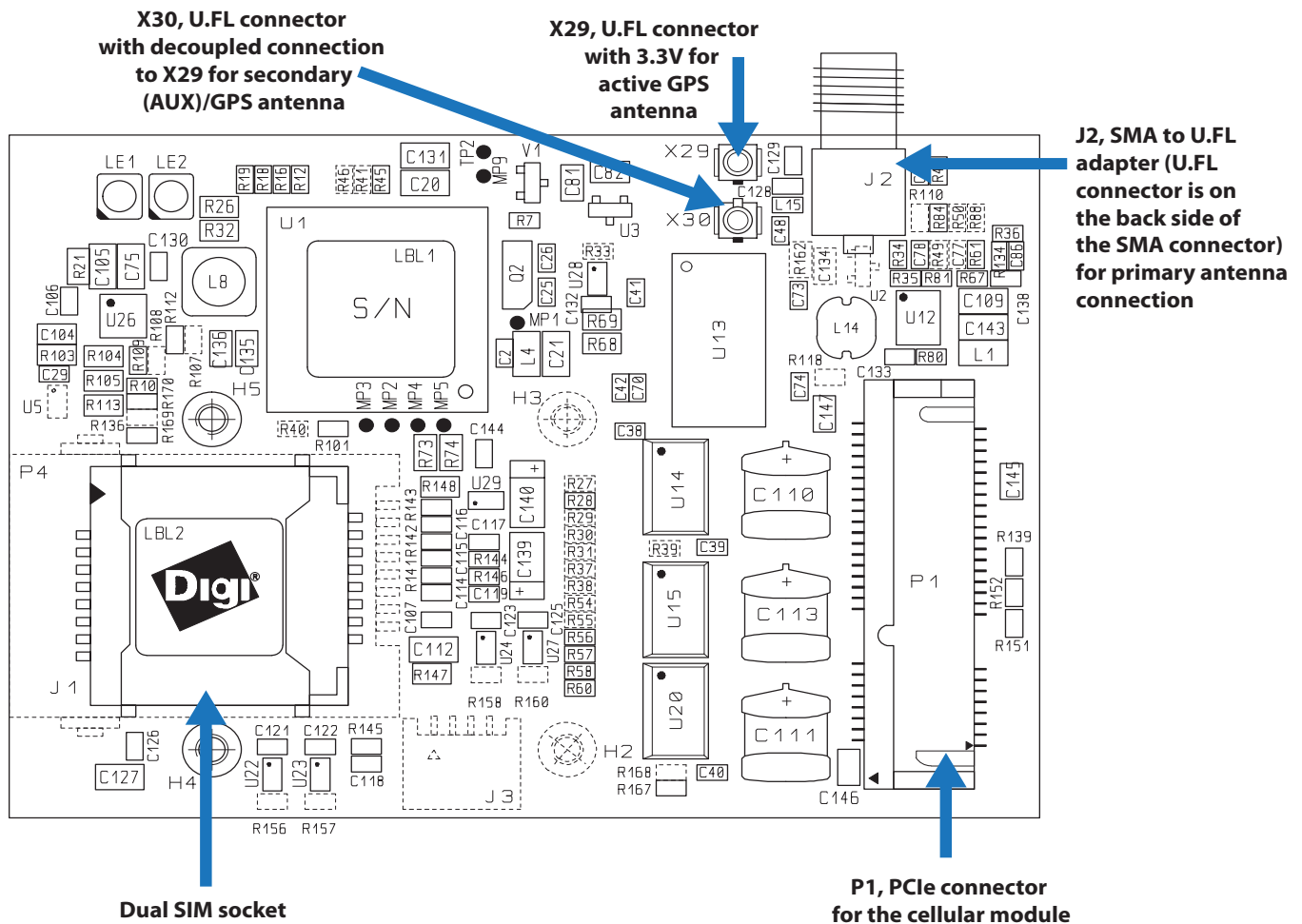
.....

For the ConnectCore 3G 9P 9215, attach the cellular antenna to the primary connector [J6] and the GPS antenna to the secondary connector [J7].

## ConnectCore 9P 9215 Development Board

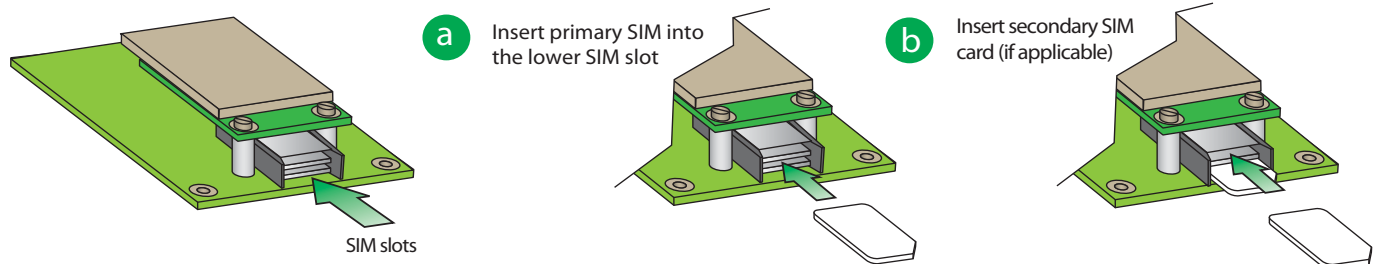


## ConnectCore 3G 9P 9215 Module



### SIM Installation

If you have not done so already, insert your SIM card(s) as shown (GSM/GPRS networks only):

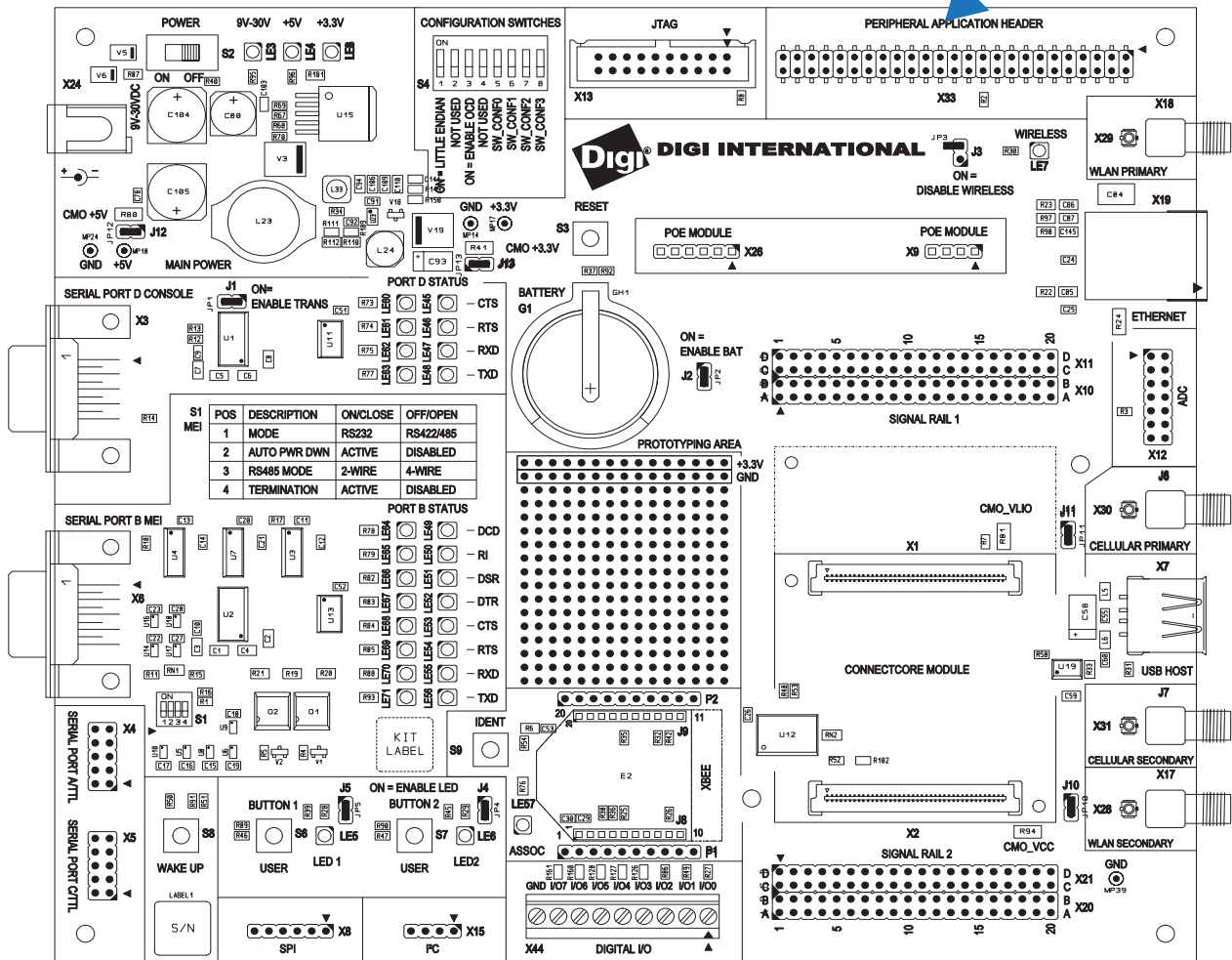


**Note:** The correct orientation for the SIMs is notched-side out, SIM cards are not included in your Digi JumpStart Kit®.

## Peripheral (Expansion) Headers

### ConnectCore 9P 9215 Development Board

Peripheral Application Header, X33



The Development Board provides one, 2x25-pin, 0.10" (2.54mm) pitch header for supporting application-specific daughter cards/expansion boards:

- **X33, Peripheral application header:** Provides access to an 16-bit data bus, 10-bit address bus, and control signals (such as CE#, IRQ#, WE#), as well as I<sup>2</sup>C and power (+3.3V). Using these signals, you can connect Digi-specific extension modules or your own daughter card to the module's address/data bus.

## Peripheral application header, X33

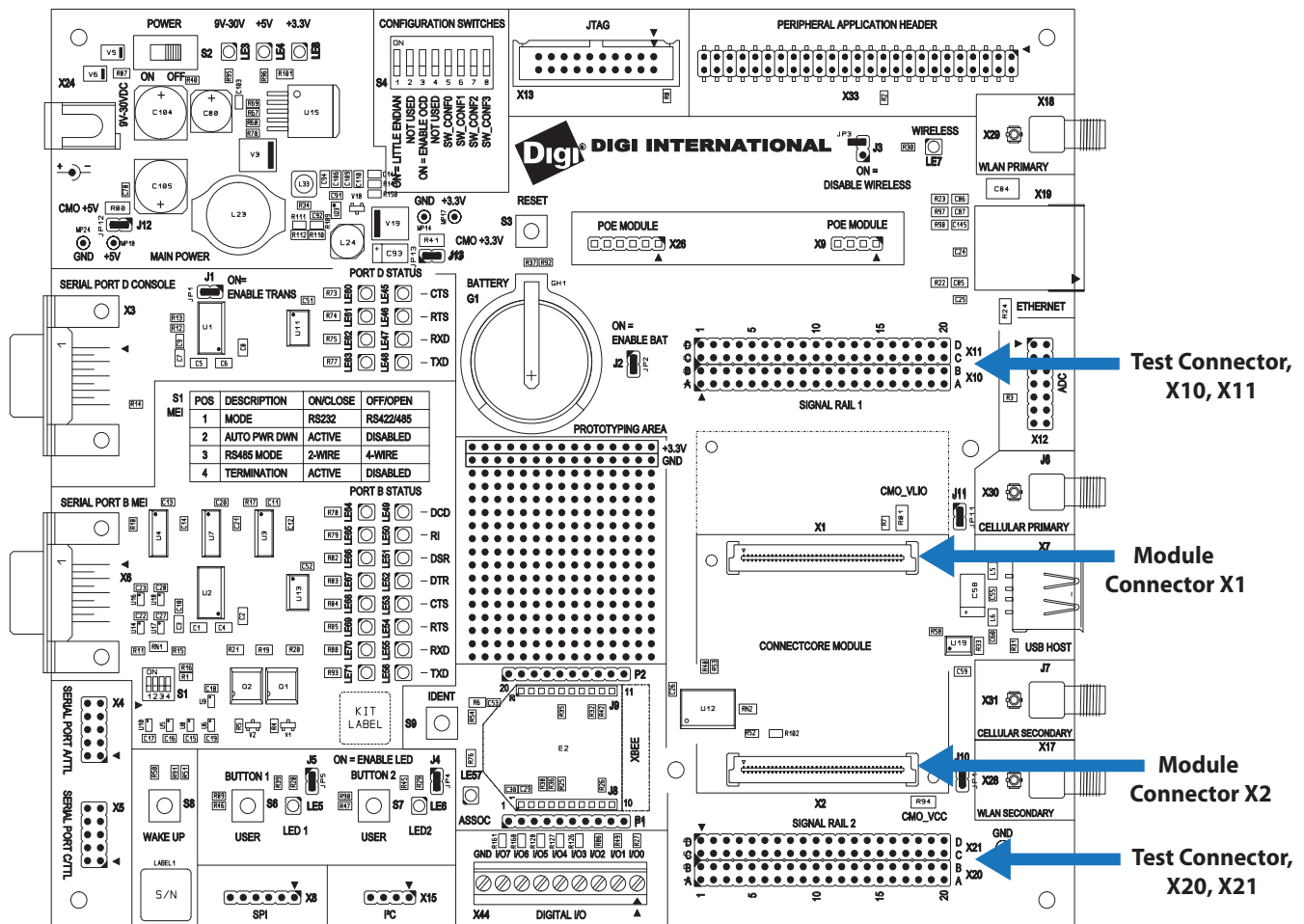
Peripheral application pins are allocated as shown:

| Pin | Signal          | Pin | Signal                                           |
|-----|-----------------|-----|--------------------------------------------------|
| 1   | GND             | 2   | BDO                                              |
| 3   | BD1             | 4   | BD2                                              |
| 5   | BD3             | 6   | GND                                              |
| 7   | BD4             | 8   | BD5                                              |
| 9   | BD6             | 10  | BD7                                              |
| 11  | GND             | 12  | BD8                                              |
| 13  | BD9             | 14  | BD10                                             |
| 15  | BD11            | 16  | GND                                              |
| 17  | BD12            | 18  | BD13                                             |
| 19  | BD14            | 20  | BD15                                             |
| 21  | GND             | 22  | * 8-bit / 16-bit#<br>GND selects 16-bit data bus |
| 23  | GND             | 24  | +3.3V                                            |
| 25  | +3.3V           | 26  | BA0                                              |
| 27  | BA1             | 28  | BA2                                              |
| 29  | BA3             | 30  | GND                                              |
| 31  | BA4             | 32  | BA5                                              |
| 33  | BA6             | 34  | BA7                                              |
| 35  | GND             | 36  | BA8                                              |
| 37  | BA9             | 38  | GND                                              |
| 39  | EXT_CSO#        | 40  | I2C_SDA/GPIO103                                  |
| 41  | EXT_WE#         | 42  | EXT_OE#                                          |
| 43  | I2C_SCL/GPIO102 | 44  | EIRQ3/GPIO101                                    |
| 45  | +3.3V           | 46  | +3.3V                                            |
| 47  | GPIO86          | 48  | GPIO87                                           |
| 49  | EXT_CLK         | 50  | GND                                              |

## Module and Test Connectors

The ConnectCore 9P 9215 Family of modules plug into the module connectors X1 and X2 on the Development Board.

### ConnectCore 9P 9215 Development Board



### Module connectors

See “Module pinout” on page 41 for related information.

### Test connectors

The Development Board provides two 4x20 pin test connectors, labeled X10/X11 and X20/X21. These connectors are 1:1 copies of the module pins and are used for measurement or test purposes.

- X10 and X11 correspond to module connector X1.
- X20 and X21 correspond to module connector X2.

## X10 pinout

| X10 pin | Signal             | X10 pin | Signal        |
|---------|--------------------|---------|---------------|
| A1      | GND                | B1      | GND           |
| A2      | RSTOUT#            | B2      | TCK           |
| A3      | TDO                | B3      | TRST#         |
| A4      | LITTLE#/BIG_ENDIAN | B4      | WLAN_DISABLE# |
| A5      | SW_CONF2           | B5      | SW_CONF3      |
| A6      | BD0                | B6      | BD1           |
| A7      | BD4                | B7      | BD5           |
| A8      | BD8                | B8      | BD9           |
| A9      | BD12               | B9      | BD13          |
| A10     | GND                | B10     | BA0           |
| A11     | BA3                | B11     | BA4           |
| A12     | BA7                | B12     | BA8           |
| A13     | BA11               | B13     | BA12          |
| A14     | BA15               | B14     | BA16          |
| A15     | EXT_WE#            | B15     | EXT_CS0#      |
| A16     | BE3#               | B16     | EXT_WAIT#     |
| A17     | NC                 | B17     | NC            |
| A18     | NC                 | B18     | NC            |
| A19     |                    | B19     |               |
| A20     |                    | B20     | VBAT          |

\*USB and Ethernet signals are not connected to this connector due to signal quality.

## X11 pinout

| X11 pin | Signal                    | X11 pin | Signal   |
|---------|---------------------------|---------|----------|
| C1      | RSTIN#                    | D1      | SRESET#  |
| C2      | TMS                       | D2      | TDI      |
| C3      | RTCK                      | D3      | OCD_EN#  |
| C4      | SW_CONF0                  | D4      | SW_CONF1 |
| C5      | WLAN_LED# (CC Wi-9P 9215) | D5      | GND      |
| C6      | BD2                       | D6      | BD3      |
| C7      | BD6                       | D7      | BD7      |
| C8      | BD10                      | D8      | BD11     |
| C9      | BD14                      | D9      | BD15     |
| C10     | BA1                       | D10     | BA2      |
| C11     | BA5                       | D11     | BA6      |
| C12     | BA9                       | D12     | BA10     |
| C13     | BA13                      | D13     | BA14     |
| C14     | GND                       | D14     | EXT_OE#  |
| C15     | EXT_CS2#                  | D15     | BE2#     |
| C16     | EXT_CLK                   | D16     | GND      |
| C17     | NC                        | D17     | NC       |
| C18     | GND                       | D18     |          |
| C19     |                           | D19     |          |
| C20     | 3.3V                      | D20     | GND      |

\*USB and Ethernet signals are not connected to this connector due to signal quality.

## X20 pinout

| X20 pin | Signal               | X20 pin | Signal             |
|---------|----------------------|---------|--------------------|
| A1      | GND                  | B1      | GND                |
| A2      | DSRA#/GPIO2          | B2      | RXDA/SPI_RXD/GPIO3 |
| A3      | DTRA#/GPIO6          | B3      | TXDA/SPI_TXD/GPIO7 |
| A4      | DSRC#/GPIO10         | B4      | RXDC/GPIO11        |
| A5      | DTRC#/TXCLKC/GPIO14  | B5      | TXDC/GPIO15        |
| A6      | DSRB#/GPIO53         | B6      | RXDB/GPIO54        |
| A7      | DTRB#/GPIO57         | B7      | TXDB/GPIO58        |
| A8      | DSRD#/GPIO61         | B8      | RXDD/GPIO62        |
| A9      | DTRD#/GPIO65         | B9      | TXDD/GPIO66        |
| A10     | GPIO69               | B10     | GPIO70             |
| A11     | GPIO73               | B11     | GPIO74             |
| A12     | GPIO77               | B12     | GPIO78             |
| A13     | USER_BUTTON1#/GPIO81 | B13     | USER_LED1#/GPIO82  |
| A14     | USER_LED2#/GPIO85    | B14     | GPIO86             |
| A15     | GPIO94               | B15     | GPIO95             |
| A16     | CAN1_RXD/GPIO98      | B16     | CAN1_TXD/GPIO99    |
| A17     | I2C_SCL/GPIO102      | B17     | I2C_SDA/GPIO103    |
| A18     | ADC_IN2              | B18     | ADC_IN3            |
| A19     | ADC_IN6              | B19     | ADC_IN7            |
| A20     | +3.3V                | B20     | +3.3V              |

## X21 pinout

| X21 pin | Signal             | X21 pin | Signal               |
|---------|--------------------|---------|----------------------|
| C1      | DCDA#/SPI_EN/GPIO0 | D1      | CTSA#/GPIO1          |
| C2      | RIA#/EIRO2/GPIO4   | D2      | RTSA#/SPI_CLK/GPIO5  |
| C3      | DCDC#/TXCLKC/GPIO8 | D3      | CTSC#/GPIO9          |
| C4      | RIC#/RXCLKC/GPIO12 | D4      | RTSC#/RCLKC/GPIO13   |
| C5      | DCDB#/GPIO51       | D5      | CTSB#/GPIO52         |
| C6      | RIB#/GPIO55        | D6      | RTSB#/GPIO56         |
| C7      | DCDD#/GPIO59       | D7      | CTSD#/GPIO60         |
| C8      | RID#/GPIO63        | D8      | RTSD#/GPIO64         |
| C9      | GPIO67             | D9      | GPIO68               |
| C10     | GPIO71             | D10     | GPIO72               |
| C11     | GPIO75             | D11     | GPIO76               |
| C12     | GPIO79             | D12     | GPIO80               |
| C13     | GPIO83             | D13     | USER_BUTTON2#/GPIO84 |
| C14     | GPIO87             | D14     | GPIO93               |
| C15     | CAN0_RXD/GPIO96    | D15     | CAN0_TXD/GPIO97      |
| C16     | GPIO100            | D16     | EIR03#/GPIO101       |
| C17     | ADC_IN0            | D17     | ADC_IN1              |
| C18     | ADC_IN4            | D18     | ADC_IN5              |
| C19     | AGND_ADC           | D19     | VREF_ADC             |
| C20     | GND                | D20     | GND                  |



# Appendix A: Specifications

This appendix provides environmental, mechanical, safety and power information for the ConnectCore 9P 9215 Family of modules.

## Mechanical Information

### ConnectCore 9P 9215

The module size is 50 x 50mm.

Two board-to-board connectors are used on the module. The distance between the module and the Development Board depends on the counterpart on the Development Board; the minimum distance is 5mm.

The height of the parts mounted on the bottom side of the module does not exceed 2.5mm. The height of the parts mounted on the top side of the module does not exceed 2.5mm if X3 is not populated, or 14 mm if X3 is populated.

### ConnectCore Wi-9P 9215

The module size is 50 x 70mm.

Two board-to-board connectors are used on the module. The distance between the module and the Development Board depends on the counterpart on the Development Board; the minimum distance is 5mm.

The height of the parts mounted on the bottom side of the module does not exceed 2.5mm. The height of the parts mounted on the top side of the modules does not exceed 5mm if X3 is not populated, or 14 mm if X3 is populated.

## ConnectCore 3G 9P 9215

The module size is 50 x 70mm.

Two board-to-board connectors are used on the module. The distance between the module and the Development Board depends on the counterpart on the Development Board; the minimum distance is 5mm.

The height of the parts mounted on the bottom side of the module does not exceed 2.5mm. The height of the parts mounted on the top side of the modules does not exceed 10mm including the cellular module.

## Network Interface

### Ethernet

- Standard: IEEE 802.3
- Physical layer: 10/100Base-T
- Data rate: 10/100 Mbps
- Mode: Full or half duplex

### WLAN Interface

**Note:** This WLAN Interface information applies to the ConnectCore Wi-9P 9215 module only.

- Standard: IEEE802.11a/b/g
- Frequency: 2.412GHz - 5.875GHz
- Data Rates Supported
  - 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, 54 Mbps
- Media Access Protocol
  - Carrier-Sense Multiple Access with Collision Avoidance (CSMA/CA)
- Wireless Medium
  - 802.11b/g: Direct Sequence-Spread Spectrum (DSSS) and Orthogonal Frequency Divisional Multiplexing (OFDM)
  - 802.11a: OFDM
- DFS Client
  - This module supports the DFS Client only between the 5.25 and 5.35GHz bands. It does not support being a DFS Master, nor can it be connected to an ad hoc network in these bands.
- Modulation DSSS
  - Differential Binary Phase Shift Keying (DBPSK) @ 1 Mbps
  - Differential Quadrature Phase Shift Keying (DQPSK) @ 2 Mbps

- Complementary Code Keying (CCK) @ 5.5 and 11 Mbps OFDM
- BPSK @ 6 and 9 Mbps
- QPSK @ 12 and 18 Mbps
- 16-Quadrature Amplitude Modulation (QAM) @ 24 and 36 Mbps
- 64-QAM @ 48 and 54 Mbps
- Frequency Bands
  - 2.412 to 2.472 GHz (ETSI)
  - 2.412 to 2.462 GHz (FCC)
  - 5.150 to 5.250 GHz (ETSI)
  - 5.250 to 5.350 GHz (ETSI) excluding TPC and DFS Client
  - 5.470 to 5.725 GHz (ETSI) excluding TPC and DFS Client
  - 5.725 to 5.875 GHz (ETSI) excluding TPC and DFS Client
  - 5.15 to 5.350 GHz (FCC UNII1 and UNII2)
  - 5.470 to 5.725 GHz
  - 5.725 to 5.850 GHz (FCC)
- Receive Sensitivity 802.11a (typical @ 25°C)

| CH      | 5200 | 5500 | 5785 |
|---------|------|------|------|
| 6 Mbps  | -85  | -85  | -85  |
| 54 Mbps | -65  | -65  | -65  |

- Receive Sensitivity 802.11g (typical 25°C)
  - -84 dBm @ 6 Mbps
  - -81 dBm @ 9 Mbps
  - -80 dBm @ 12 Mbps
  - -80 dBm @ 18 Mbps
  - -78 dBm @ 24 Mbps
  - -76 dBm @ 36 Mbps
  - -70 dBm @ 48 Mbps
  - -68 dBm @ 54 Mbps
- Receive Sensitivity 802.11b (typical 25°C)
  - -86 dBm @ 1 Mbps
  - -86 dBm @ 2 Mbps
  - -84 dBm @ 5.5 Mbps
  - -80 dBm @ 11 Mbps

- Available Transmit Power Settings  
(Maximum power setting will vary according to individual country regulations).  
Typical (  $\pm 2$  dBm) 25°C

802.11b/g:

- 14 dBm (~25 mW) @ 1, 2, 5.5, and 11 Mbps
- 12 dBm (~16 mW) @ 6, 12, 18, 24, 36, 48, and 54 Mbps
- 6 dBm (~4 mW) @ 6, 12, 18, 24, 36, 48, and 54 Mbps

802.11a:

- 6 dBm for all channels

**Note:** During manufacturing, EVM values are verified up to -23 dBm rms for band A.

- Available Transmit Power Settings (Typical (  $\pm 2$  dBm) @ 25°C)

**Note:** Maximum power setting will vary according to individual country regulations.

- Connector: 2 x U.FL

**Note:** Please use the HIROSE U.FL-LP-N-2 extraction tool for removing a U.FL cable from the ConnectCore Wi-9P 9215 or ConnectCore 3G 9P 9215 modules.

## WWAN Interface

**Note:** This WWAN Interface information applies to the ConnectCore 3G 9P 9215 module only.

2G/3G cellular connectivity based on Qualcomm Gobi 3000:

| Technology                   | Bands                          |
|------------------------------|--------------------------------|
| 1xEV-DO Rev A<br>1xRTT Rev 0 | BC0 - 800 MHz - US cell        |
|                              | BC1 - 1900MHz - US PCS         |
|                              | BC4 - 1800 MHz - KPCS          |
|                              | BC6 - 2100 MHz - IMT           |
| UMTS/HSDPA/HSUPA             | B9 - 1700 MHz - Japan 1700 MHz |
|                              | B8 - 900 MHz                   |
|                              | B6 - 900 MHz - Japan 800 MHz   |
|                              | B4 - 1700/2100 - AWS           |
|                              | B5 - 850 MHz - US Cell         |
|                              | B3 - 1800 MHz - KPCS           |
|                              | B2 - 1900 MHz - US PCS         |

| Technology       | Bands    |
|------------------|----------|
| GSM/GPRS/EDGE    | 850 MHz  |
|                  | 900 MHz  |
|                  | 1800 MHz |
|                  | 1900 MHz |
| Simultaneous GPS |          |

**Note:** D = Rx diversity supported  
X = band class supported without Rx diversity  
blank = band class not supported

Supported Data Rates:

| Gobi Operating Mode | Peak FL Data Rate | Peak RL Data Rate |
|---------------------|-------------------|-------------------|
| CDMA 1xRTT          | 153 kbps          | 153 kbps          |
| CDMA 1xEV-DO        | 3.1 Mbps          | 1.8 Mbps          |
| WCDMA               | 384 kbps          | 384 kbps          |
| HSDPA/HSUPA         | 7.2 Mbps          | 2.0 Mbps          |
| GSM                 | 14.1 kbps         | 14.1 kbps         |
| GPRS                | 115 kbps          | 115 kbps          |
| EDGE                | 384 kbps          | 384 kbps          |

## Environmental Information

.....

The module board assemblies meet all functional requirements when operating in the environments provided below.

**Note:** Please refer to the thermal specifications in this manual for additional information about operating temperature conditions

### **ConnectCore 9P 9215**

- Operating temperature: -40°C to +85°C max
- Storage temperature: -40°C to +125°C
- Relative humidity: 5% to 95%, non-condensing
- Altitude: 0 to 12,000 feet

### **ConnectCore Wi-9P 9215 & ConnectCore 3G 9P 9215**

- Operating temperature: -40°C to +85°C max
- Storage temperature: -40°C to +125°C
- Relative humidity: 5% to 95%, non-condensing
- Altitude: 0 to 12,000 feet
- Qualcomm Gobi3000 operating temperature: -30°C to +70°C
- Qualcomm Gobi3000 storage temperature: -55°C to +100°C
- Qualcomm Gobi3000 relative humidity: 10% to 90%, non-condensing

## Thermal Specifications

The table below shows the specific standard operating temperature ranges for the entire ConnectCore 9P 9215 Family of embedded core modules.

| Standard Operating Temperature Ranges |                                                                               |
|---------------------------------------|-------------------------------------------------------------------------------|
| Product                               | Operating Temperature Range                                                   |
| ConnectCore 9P 9215                   | -40 to +85°C                                                                  |
| ConnectCore Wi-9P 9215                | -40 to +65°C @ 100% Duty Cycle (WLAN)<br>-40 to +85°C @ 33% Duty Cycle (WLAN) |
| ConnectCore 3G 9P 9215                | -30 to +70°C                                                                  |

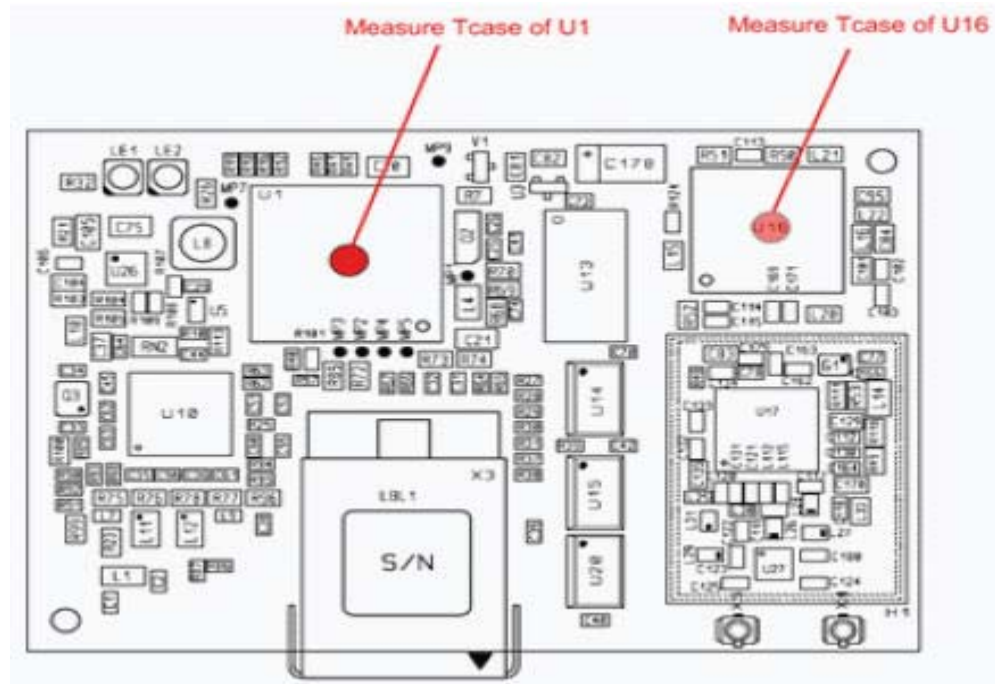
The lower standard operating temperature range is specified without restrictions, except condensation must not occur.

The upper operating temperature limit depends on the host PCB layout and surrounding environmental conditions. To simplify the customer's design process, a maximum component case temperature has been specified.

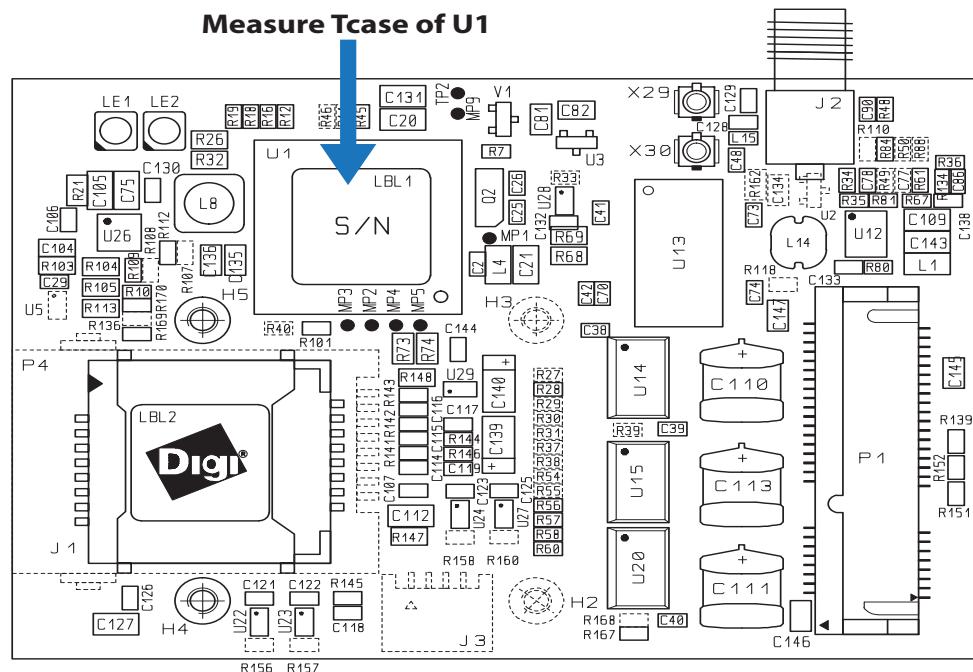
| Maximum Component Case Temperature |           |                          |
|------------------------------------|-----------|--------------------------|
| Product                            | Component | Maximum Case Temperature |
| ConnectCore 9P 9215                | U1        | 120°C                    |
| ConnectCore Wi-9P 9215             | U16       | 95°C                     |
| ConnectCore 3G 9P 9215             | U1        | 120°C                    |

The maximum component case temperature must remain below the maximum, measured at the locations shown in the figure below.

## ConnectCore Wi-9P 9215 Module



## ConnectCore 3G 9P 9215 Module



When attaching thermocouples, please abide by the following guidelines:

- Carefully remove any labels or other foreign material from the component.
- Ensure an adhesive with high thermal conductivity is used. Use as little adhesive as possible.
- Make sure the thermocouple is touching the case of the component and not "floating" in the adhesive.
- The use of precision, fine-wire K-type thermocouples is strongly recommended
  - Omega Engineering P/N 5TC-TT-K-36-72, or similar

### Additional design suggestions

The following list provides additional design guidance with respect to thermal management in applications with operating temperatures at the high end or beyond the specified standard ambient temperature range.

- Providing air movement will improve heat dissipation.
- The host PCB plays a large part in dissipating the heat generated by the module. A large copper plane located will improve the heat dissipation capabilities of the PCB.
- If the design allows, added buried PCB planes will also improve heat dissipation. The copper planes create a larger surface to spread the heat into the surrounding environment.

## Safety Statements

---

### **To avoid contact with electrical current:**

- Never install electrical wiring during an electrical storm.
- Use a screwdriver and other tools with insulated handles.
- Wear safety glasses or goggles.
- Installation of inside wiring may bring you close to electrical wire, conduit, terminals, and other electrical facilities. Extreme caution must be used to avoid electrical shock from such facilities. Avoid contact with all such facilities.
- Protectors and grounding wire placed by the service provider must not be connected to, removed, or modified by the customer.
- Do not touch or move the antenna(s) while the unit is transmitting or receiving.
- Do not hold any component containing a radio such that the antenna is very close to or touching any exposed parts of the body, especially the face or eyes, while transmitting.
- Do not operate a portable transmitter near unshielded blasting caps or in an explosive environment unless it is a type especially qualified for such use.
- Any external communications wiring you may install needs to be constructed to all relevant electrical codes. In the United States, this is the National Electrical Code Article 800. Contact a licensed electrician for details.

## Power Requirements

### ConnectCore 9P 9215

| Parameter                                        | Limits                    |                  |          |
|--------------------------------------------------|---------------------------|------------------|----------|
| Input voltage (Vcc)                              | 3.3V±10% (3.00V to 3.60V) |                  |          |
| Input current                                    | 660mA max                 |                  |          |
| Input low voltage                                | 0.0V                      | <V <sub>IL</sub> | <0.3*Vcc |
| Input high voltage                               | 0.7*Vcc                   | <V <sub>IH</sub> | <Vcc     |
| Output low voltage<br>(@I <sub>OL</sub> =100uA)  | 0.0V                      | <V <sub>OL</sub> | <0.2V    |
| Output high voltage<br>(@I <sub>OH</sub> =100uA) | Vcc-0.2V                  | <V <sub>OH</sub> | <Vcc     |

### ConnectCore Wi-9P 9215

| Parameter           | Limits                    |                  |          |
|---------------------|---------------------------|------------------|----------|
| Input voltage (Vcc) | 3.3V±10% (3.00V to 3.60V) |                  |          |
| Input current       | 1A max                    |                  |          |
| Input low voltage   | 0.0V                      | <V <sub>IL</sub> | <0.3*Vcc |
| Input high voltage  | 0.7*Vcc                   | <V <sub>IH</sub> | <Vcc     |
| Output low voltage  | 0.0V                      | <V <sub>OL</sub> | <0.4V    |
| Output high voltage | Vcc-0.4V                  | <V <sub>OH</sub> | <Vcc     |

### ConnectCore 3G 9P 9215

| Parameter           | Limits                    |                  |          |
|---------------------|---------------------------|------------------|----------|
| Input voltage (Vcc) | 3.3V±10% (3.00V to 3.60V) |                  |          |
| Input current       | 1.9A max                  |                  |          |
| Input low voltage   | 0.0V                      | <V <sub>IL</sub> | <0.3*Vcc |
| Input high voltage  | 0.7*Vcc                   | <V <sub>IH</sub> | <Vcc     |
| Output low voltage  | 0.0V                      | <V <sub>OL</sub> | <0.4V    |
| Output high voltage | Vcc-0.4V                  | <V <sub>OH</sub> | <Vcc     |

## IEEE802.11 a/b/g WLAN

The ConnectCore Wi-9P 9215 provides access to an IEEE802.11a/b/g WLAN interface. The whole circuitry is located on the module. The user can track WLAN activity through the WLAN-LED# signal. The user can also disable the RF power amplifier by activating the WLAN-DISABLE# signal.

Two U.FL connectors are available for dual-diversity.

The WLAN baseband controller can be reset through GPIO92. When this signal is low, the baseband controller is in reset mode. When high, the controller is active.

The interrupt signal connected to the baseband controller is GPIO\_AO.

## WWAN Activity

The ConnectCore3G 9P 9215 provides access to a PCIe 3G module. The entire 3G circuitry is located on the module. The user can track WWAN activity through the LED\_WWAN# signal. The user can also disable the 3G module by activating the CELL\_DISABLE\_N signal.

Not including the Gobi modem there are three U.FL connectors for a WWAN antenna and a GPS antenna available on the ConnectCore 3G 9P 9215 module. Including the Gobi modem there are five U.FL connectors available.

## ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 Typical Power Save Current/Power Measurements

The following information illustrates typical power consumption for the ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 modules. These measurements were made using the NET+OS napsave sample application in function `applicationStart( )`, with the module's Ethernet connected to a 100Mb network. For the ConnectCore Wi-9P 9215 module, WiFi is enabled and associated.

### ConnectCore 9P 9215

|                                      | Module and Dev Board <sup>1</sup> | Module only <sup>2</sup> |
|--------------------------------------|-----------------------------------|--------------------------|
| Normal operational mode <sup>3</sup> | 1.63W (496mA)                     | 1.45W (443mA)            |
| Sleep mode <sup>4</sup>              | .346W (105mA)                     | .151W (46mA)             |

### ConnectCore Wi-9P 9215

|                                      | Module and Dev Board <sup>1</sup> | Module only <sup>2</sup> |
|--------------------------------------|-----------------------------------|--------------------------|
| Normal operational mode <sup>3</sup> | 2.69W (816mA)                     | 2.36W (716mA)            |
| Sleep mode <sup>4</sup>              | 0.73W (220mA)                     | 0.46W (138mA)            |

<sup>1</sup> This measurement was taken from the R80 current sense resistor (0.025 ohm) on the JumpStart Kit Development Board.

<sup>2</sup> This measurement represents only the current of the VLIO and +3.3V inputs to the module, measured from the two current sense resistors R81 and R94 (0.025 ohm) located on the JumpStart Kit Development Board.

<sup>3</sup> This is the default power consumption mode when entering application `Start()`, as measured with the napsave sample application. The value of the NS9215 Clock Configuration register (A090017C) is 02012015 hexadecimal. (Note 02012015 enables USART B, UART D, the Ethernet MAC, the I/O Hub, and Memory Clock 0).

<sup>4</sup> This measurement was produced by selecting the “Deep Sleep/Wakeup with an External IRQ” menu option in the napsave sample application.

## ConnectCore 3G 9P 9215 Typical Power Save Current /Power Measurements

The following information illustrates typical power consumption for the ConnectCore 3G 9P 9215 module. These measurements were made using a Python application, which made a call into `digipowercontrol.system_power_set(0)`, which placed the module into a deep sleep mode.

### ConnectCore 3G 9P 9215

|                                      | Module and Dev Board <sup>1</sup> | Module only <sup>2</sup> |
|--------------------------------------|-----------------------------------|--------------------------|
| Normal operational mode <sup>4</sup> | 2.60W (800mA)                     | 2.30W (708mA)            |
| Sleep mode <sup>3, 4</sup>           | 0.61W (184mA)                     | 0.463W (140mA)           |

<sup>1</sup> This measurement was taken from the R80 current sense resistor (0.025 ohm) on the JumpStart Kit Development Board.

<sup>2</sup> This measurement represents only the current of the VLIO and +3.3V inputs to the module, measured from the two current sense resistors R81 and R94 (0.025 ohm) located on the JumpStart Kit Development Board.

<sup>3</sup> This measurement was made using the Python `digipowercontrol.system_power_set(0)` API, which places the module into a deep sleep mode.

<sup>4</sup> These measurements were made with an ethernet cable plugged in and no external USB devices connected.

## Typical Module Current/Power Measurements

The following information illustrates typical power consumption using various NS9215 power management mechanisms. These measurements were taken with all NS9215 I/O clocks disabled except UART B, UART D, Ethernet MAC, I/O Hub, and the Memory Clock; the Ethernet connected to a 100Mb network and the WLAN interface associated with an access point, using a standard module plugged into a JumpStart Kit Development Board, with nominal voltage applied.

### ConnectCore 9P 9215

|                                        | VLIO <sup>1</sup>    | +3.3V <sup>1</sup>   | Total Power |
|----------------------------------------|----------------------|----------------------|-------------|
| With FIMs (DRPIC) enabled <sup>4</sup> | 1.27W (384mA @ 3.3V) | .561W (170mA @ 3.3V) | 1.83W       |
| Full clock scaling mode <sup>4</sup>   | .904W (274mA @ 3.3V) | .561W (170mA @ 3.3V) | 1.47W       |

### ConnectCore Wi-9P 9215

|                                         | VLIO <sup>1</sup>    | +3.3V <sup>1</sup>   | Total Power |
|-----------------------------------------|----------------------|----------------------|-------------|
| With all clocks enabled <sup>2, 4</sup> | 1.43W (432mA @ 3.3V) | 1.17W (354mA @ 3.3V) | 2.6W        |
| Default configuration <sup>3, 4</sup>   | 1.13W (343mA @ 3.3V) | 1.17W (354mA @ 3.3V) | 2.30W       |

<sup>1</sup> VLIO is supplying the core voltage regulator. This typical measurement was made with VLIO and +3.3V set to 3.3V. VLIO can vary between 2.5V to 5.0V. +3.3V can vary between 3.1V to 3.6V.

<sup>2</sup> This is power consumption with all clocks on, NS9215 Clock Configuration register (A090017C) set to 02013BFF hexadecimal.

<sup>3</sup> This is the default power consumption. Note the default value of the NS9215 Clock Configuration register (A090017C) is 02012015 hexadecimal.

<sup>4</sup> FIM is the Flexible Interface Module. DRPIC is a high performance 8-bit RISC Microcontroller.

## Layout Recommendation

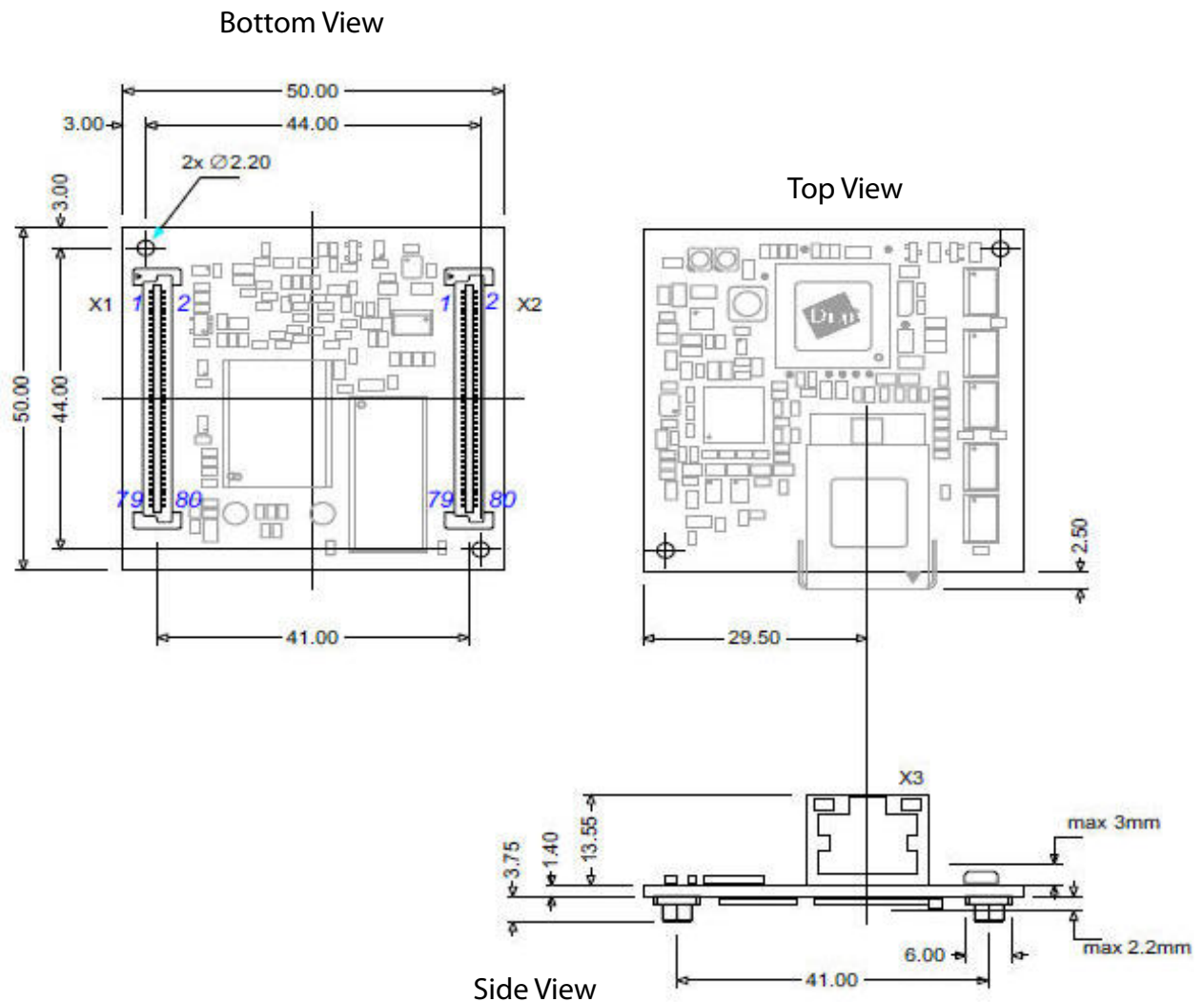
Below are the mechanical dimensions of the ConnectCore 9P 9215 Family of modules.

The layout of the JumpStart board is consistent with the recommendations from Berg/FCI for the mating connector (Berg/FCI 61083-084409LF). There is a 41mm separation between the two module connectors. Drawing number 61083 on the FCI web page: [www.fciconnect.com](http://www.fciconnect.com) shows the manufacturer recommended layout.

**Note:** Measurements are in millimeters.

### ConnectCore 9P 9215

#### Top, bottom and side views



- 
- 
- 
- 
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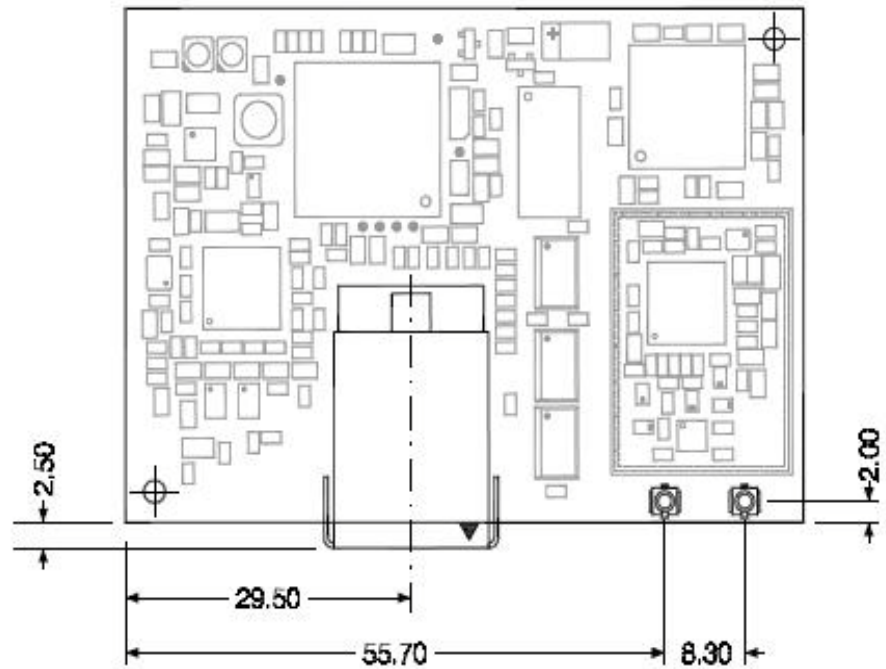


| Device                                                                             | Berg/FCI connector |
|------------------------------------------------------------------------------------|--------------------|
| ConnectCore 9P 9215 module                                                         | 61082-081409LF     |
| ConnectCore 9P 9215 JumpStart board<br>(mating connector on the Development Board) | 61083-084409LF     |

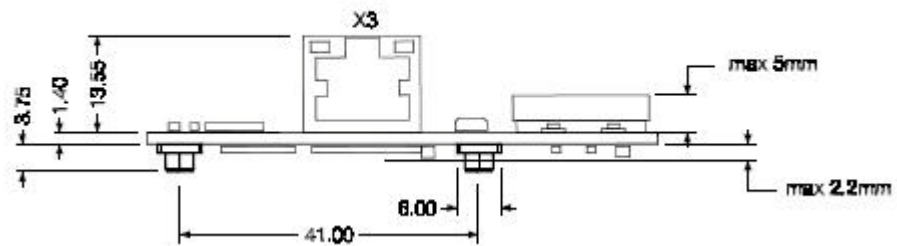
| Device                                                                                                 | Berg/FCI connector |
|--------------------------------------------------------------------------------------------------------|--------------------|
| ConnectCore 9P 9215 - Wi-9P 9215 module                                                                | 61082-081409LF     |
| ConnectCore Wi-9P 9215 JumpStart board<br>(mating ConnectCore 9P 9215 - Wi-9P 9215<br>JumpStart board) | 61083-084409LF     |

**ConnectCore Wi-9P 9215**

Below are the mechanical dimensions of the ConnectCore Wi-9P 9215 module.

**Top view**

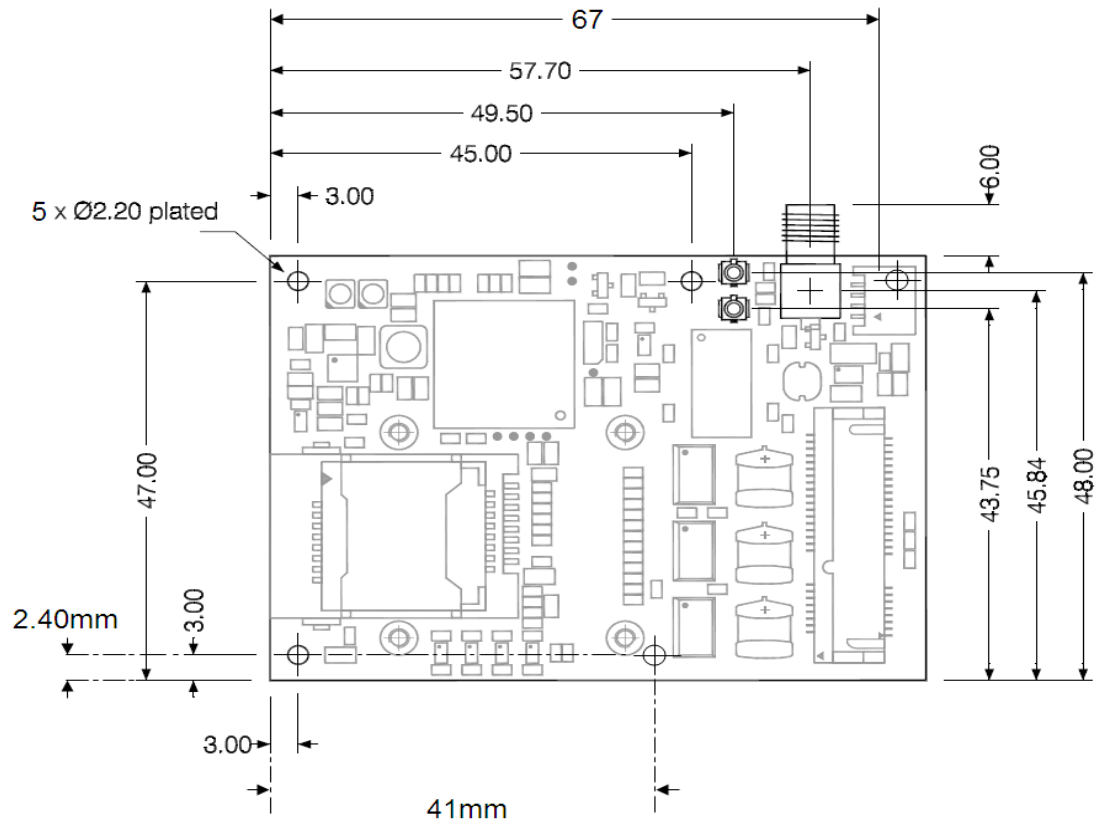
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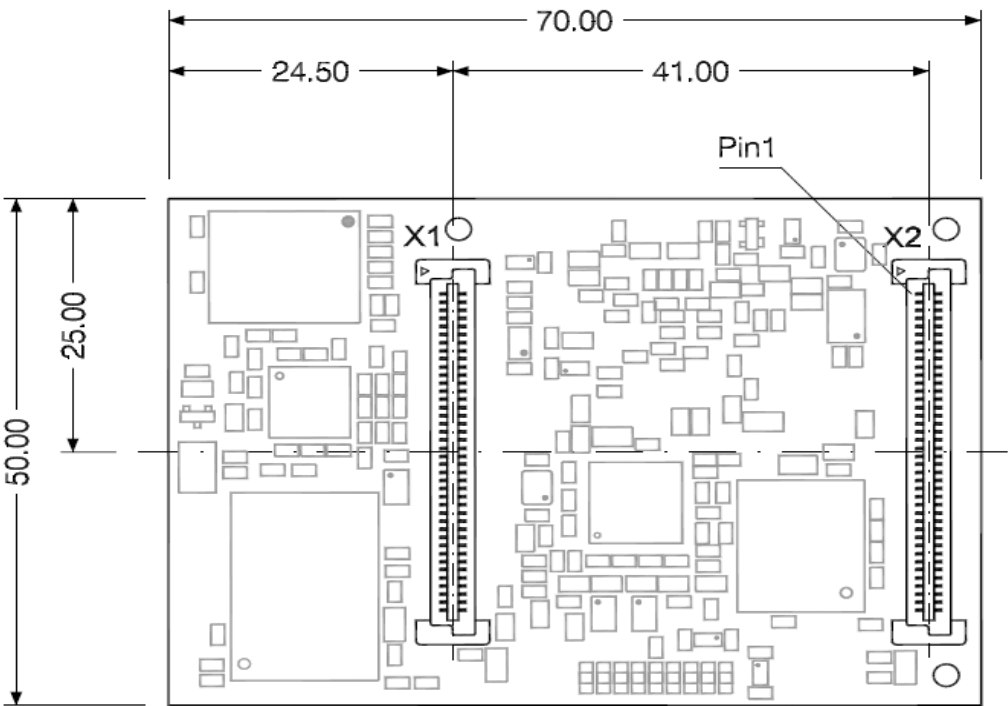
## ConnectCore 3G 9P 9215

Below are the mechanical dimensions of the ConnectCore 3G 9P 9215 module.

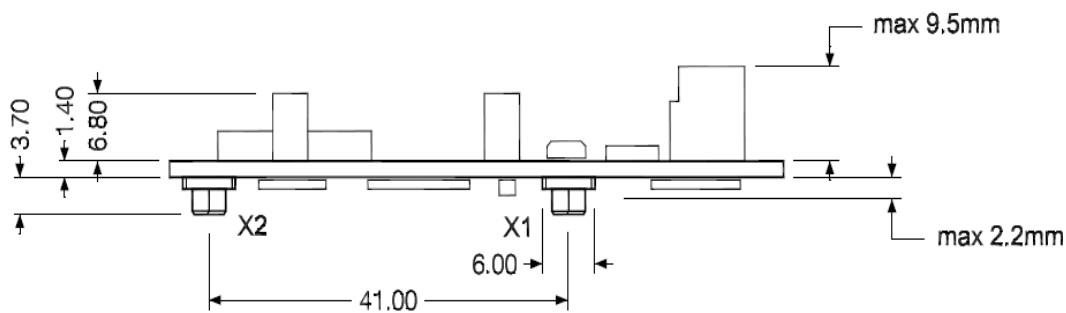
### Topview



### Bottom view



### Side view

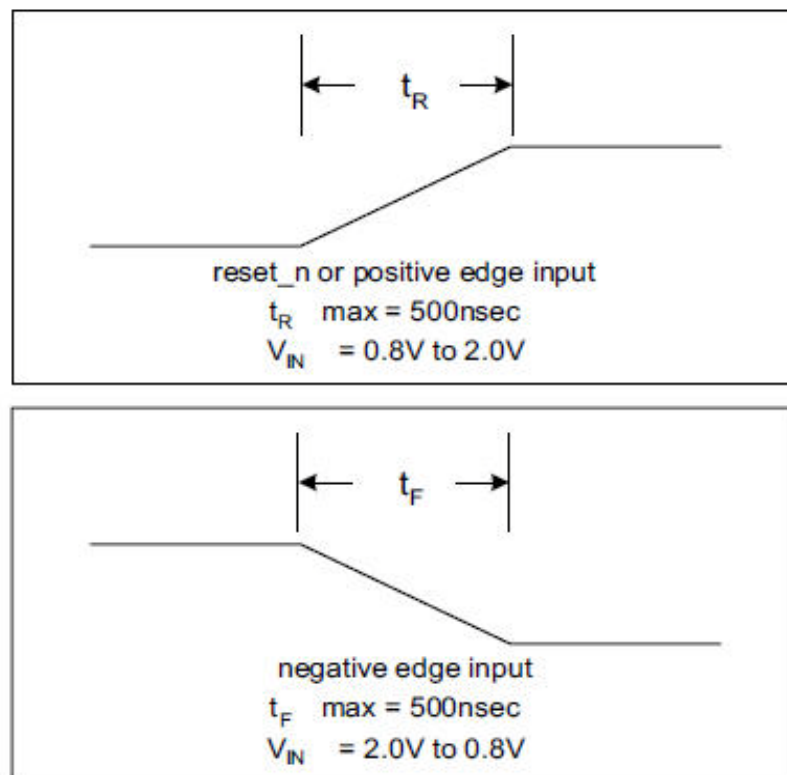


| Device                                                                                                   | Berg/FCI connector |
|----------------------------------------------------------------------------------------------------------|--------------------|
| ConnectCore 3G 9P 9215                                                                                   | 61082-081409LF     |
| ConnectCore 3G 9P 9215 Development Board<br>(mating ConnectCore 9P 9215 - Wi-9P 9215<br>JumpStart board) | 61083-084409LF     |

## Reset and Edge Sensitive Input Timing Requirements

The ConnectCore 9P 9215 Family of modules' critical timing requirement is the rise and fall time of the input. If the rise time is too slow for the reset input, the hardware strapping options may be registered incorrectly. If the rise time of a positive-edge-triggered external interrupt is too slow, then an interrupt may be detected on both the rising and falling edge of the input signal.

A maximum rise and fall time must be met to ensure that reset and edge sensitive inputs are handled correctly. With Digi processors, the maximum is 500 nanoseconds as shown:

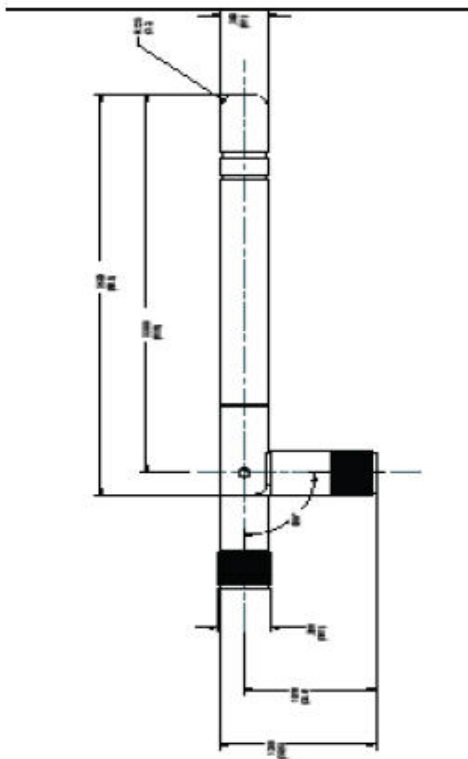


On the ConnectCore 9P 9215 Development Board there was a measurement of 220ns rise time and 10ns fall time.

.....

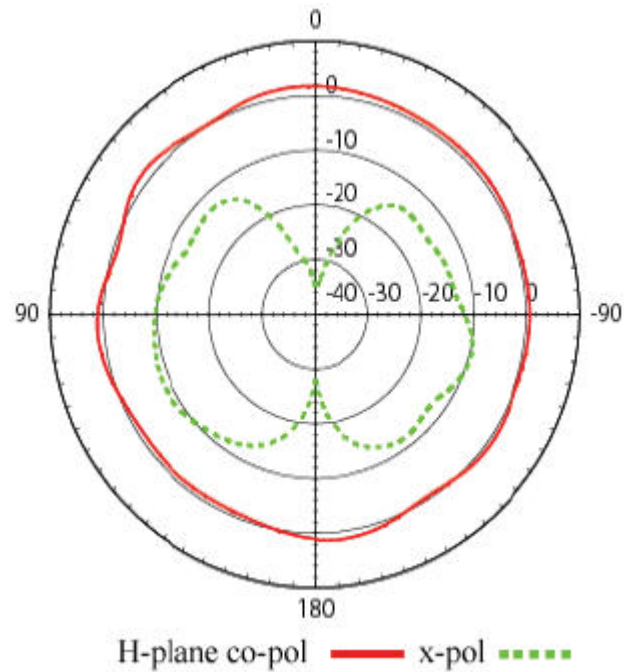
| Attribute          | Property           |
|--------------------|--------------------|
| Frequency          | 2.4~2.5 GHz        |
| Power output       | 2W                 |
| DB gain            | 2 dBi              |
| VSWR               | < or = 2.0         |
| Dimension          | 108.5 mm x 10.0 mm |
| Weight             | 10.5g              |
| Temperature rating | -40°~+80° C        |
| Part number        | DG-ANT-20DP-BG     |

**Note:** Dimensions are provided for reference purposes only. The actual antenna may vary.



### Antenna strength (radiation pattern) diagram

This diagram below shows the strength of the signal received by the whip antenna on both a horizontal and vertical plane. The diagram shows the magnetic field when the antenna is in a vertical position. The red solid line represents the horizontal plane and the green dotted line represents the vertical plane. You can see in the illustration that at 90 degrees, the signal strength is 0 (as expected).



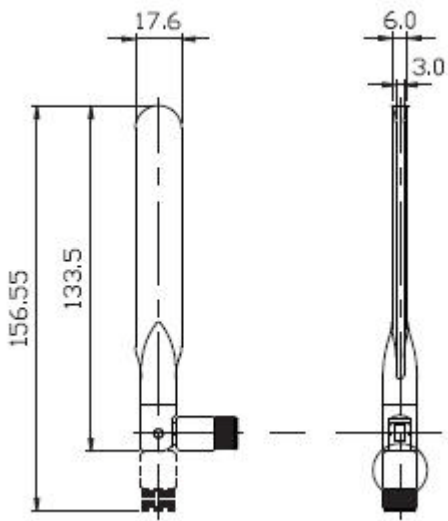
# ConnectCore Wi-9P 9215 Antenna Specifications: 5.5 dBi Dipoles

## Attributes

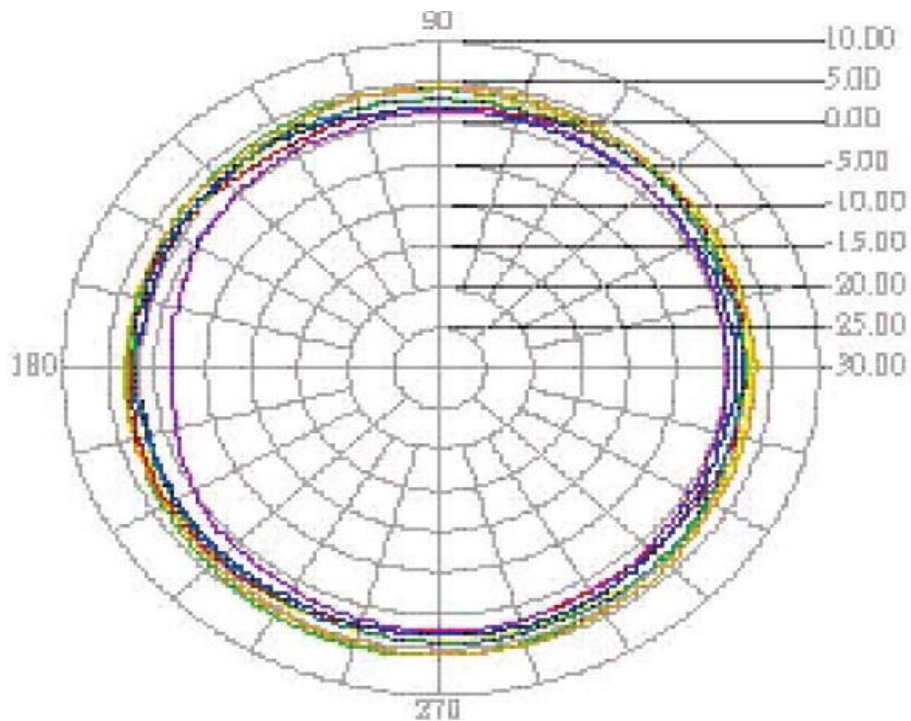
| Attributes            | Band 1                                          | Band 2                          |
|-----------------------|-------------------------------------------------|---------------------------------|
| Frequency             | 2.4~2.5 GHz                                     | 5.15~5.35 GHz<br>5.725~5.85 GHz |
| VSWR                  | 2.0 max                                         |                                 |
| Return loss           | -10 dB max                                      |                                 |
| DB gain               | 5 dBi (Typ)                                     |                                 |
| Polarization          | Linear                                          |                                 |
| Power output          | 1W                                              |                                 |
| Dimension             | See measurements in the drawing after the table |                                 |
| Operating temperature | -20°~+65°C                                      |                                 |
| Storage temperature   | -20°~+65°C                                      |                                 |
| Part number           | DG-ANT-50DP-AG                                  |                                 |

## Dimensions

**Note:** Dimensions are provided for reference purposes only. The actual antenna may vary.

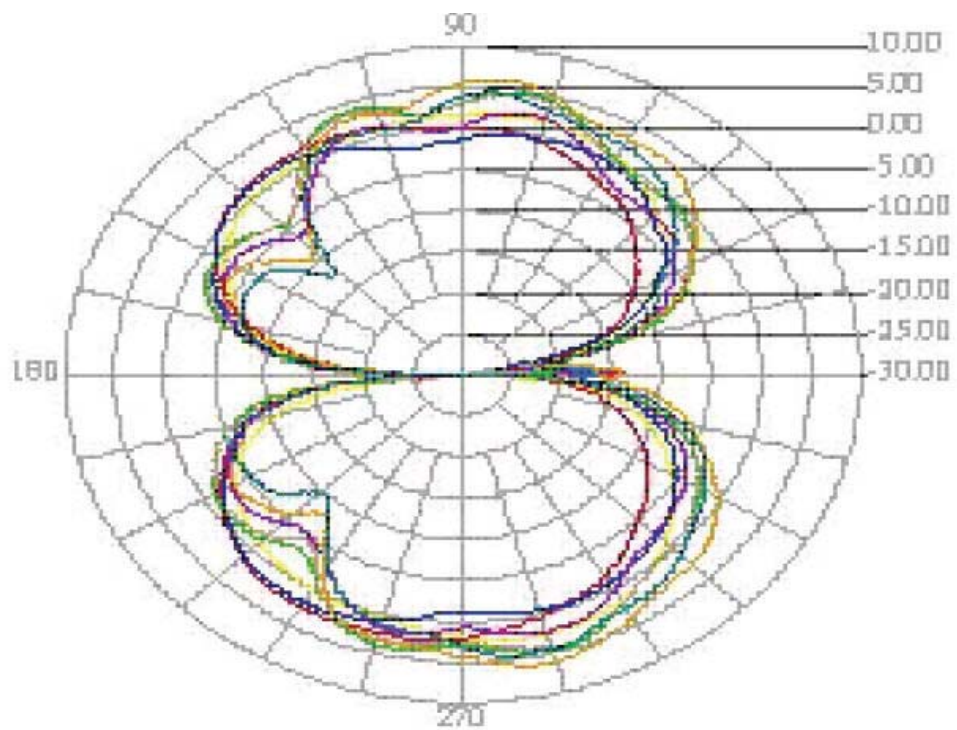


**Radiation  
pattern: H-  
Plane (2.0 and  
5.0 GHz)**



| Color       | Freq (MHz) | Peak (dBi) | Angle (o) | Avg (dBi) |
|-------------|------------|------------|-----------|-----------|
| Yellow      | 2400.0     | 3.39       | 257.68    | 2.98      |
| Red         | 2450.00    | 3.17       | 214.74    | 2.37      |
| Blue        | 2500.00    | 2.79       | 288.0     | 1.96      |
| Purple      | 5150.00    | 2.25       | 280.42    | 0.82      |
| Green       | 5200.00    | 5.23       | 252.63    | 2.71      |
| Light brown | 5250.00    | 4.51       | 272.84    | 3.16      |
| Orange      | 5750.00    | 5.03       | 267.79    | 3.88      |
| Aqua        | 5850.00    | 3.83       | 276.63    | 2.74      |

**Radiation  
pattern: E-  
plane (2.0 and  
5.0 GHz)**



| Color       | Freq (MHz) | Peak (dBi) | Angle (o) | Avg (dBi) |
|-------------|------------|------------|-----------|-----------|
| Yellow      | 2400.0     | 2.60       | 283.22    | -1.10     |
| Red         | 2450.00    | 2.57       | 240.42    | -1.36     |
| Blue        | 2500.00    | 1.92       | 237.27    | -1.78     |
| Purple      | 5150.00    | 2.37       | 78.67     | -1.91     |
| Green       | 5200.00    | 4.80       | 79.30     | 0.32      |
| Light brown | 5250.00    | 4.49       | 79.93     | -0.01     |
| Orange      | 5750.00    | 6.34       | 283.85    | 1.08      |
| Aqua        | 5850.00    | 4.67       | 283.22    | -0.46     |

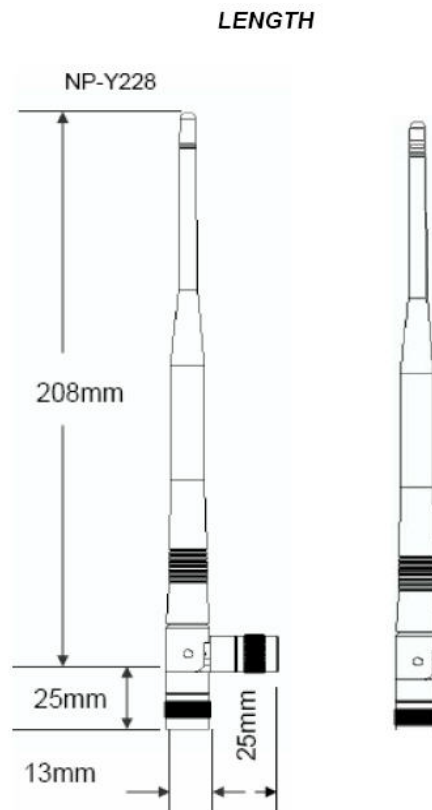
## ConnectCore 3G 9P 9215 Cellular Antenna

### Attributes

| Attributes            | Band 1                                               | Band 2      |
|-----------------------|------------------------------------------------------|-------------|
| Frequency             | 824 - 896                                            | 1710 - 1990 |
| VSWR                  | $\leq 2.0 :1$                                        |             |
| dBi gain              | 2                                                    | 3           |
| Polarization          | Vertical                                             |             |
| Impedance             | 50 Ohm                                               |             |
| Power Output          | See measurements in the drawing following this table |             |
| Operating Temperature | -30° C to +70° C                                     |             |
| Storage Temperature   | -40° C to +85° C                                     |             |
| Part number           | <b>DC-ANT-DBDP3</b>                                  |             |

### Dimensions

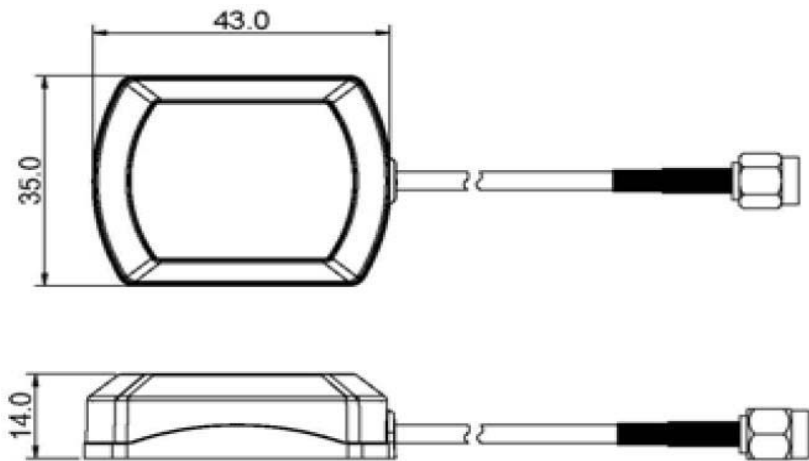
**Note:** Dimensions are provided for reference purposes only. The actual antenna may vary.



# ConnectCore 3G 9P 9215 GPS Antenna .....

## Attributes

| Parameter             | Specification                                        |
|-----------------------|------------------------------------------------------|
| Frequency             | 1575 ± 3 MHz                                         |
| VSWR                  | max. 2                                               |
| Bandwidth             | min 10 MHz                                           |
| Impedance             | 50 Ohm                                               |
| Peak Gain             | 4 dBic min. (on 7cm x 7cm ground plane)              |
| Gain Coverage         | ≥ -4dBic at -90° ≤ $\theta$ ≤ -90° (over 75% volume) |
| Power Handling        | 1 watt                                               |
| Polarization          | RHCP                                                 |
| Amplifier Gain        | typ. 27 dB (without cable)                           |
| Noise Figure          | typ. 1.5 dB                                          |
| Output VSWR           | max 2.0                                              |
| Filtering             | -35 dB (± 100 MHz)                                   |
| DC Voltage            | 2.7 to 6.0 VDC                                       |
| DC Current            | typ 8.5 mA, ± 4.5 mA                                 |
| Operating Temperature | -40° C to +85° C                                     |
| Storage Temperature   | -40° C to +85° C                                     |
| Vibration             | Sine, Sweep, 1G (0-P), 10-150?Hz each axis           |
| Humidity              | 95% ~100% RH                                         |
| Part Number           | 76000842                                             |





# Appendix B: Certifications

The ConnectCore 9P 9215 Family of modules comply with the standards cited in this section.

## FCC Part 15 Class B

### Radio Frequency Interface (RFI) (FCC 15.105)

The ConnectCore 9P 9215, ConnectCore Wi-9P 9215, and ConnectCore 3G 9P 9215 modules have been tested and found to comply with the limits for Class B digital devices pursuant to Part 15 Subpart B, of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential environment. This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try and correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

## Labeling Requirements (FCC 15.19)

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

If the FCC ID is not visible when installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module FCC ID. This exterior label can use wording such as the following: "Contains Transmitter Module FCC ID: MCQ-50M1589/ IC: 1846A-50M1589".

## RF Exposure

RF exposure considerations require that a 20 cm separation distance between users and the installed antenna location shall be maintained at all times when the module is energized. OEM installers must consider suitable module and antenna installation locations in order to assure this 20 cm separation, and end users must be also be advised of the requirement.

## Modifications (FCC 15.21)

Changes or modifications to this equipment not expressly approved by Digi may void the user's authority to operate this equipment.

## Industry Canada

This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class B prescrites dans le Règlement sur le brouillage radioélectrique édicté par le ministère des Communications du Canada.

The maximum antenna gain permitted in the bands 5250-5350 MHz and 5470-5725 MHz to comply with the e.i.r.p. limit is, according to RSS-210 section A9.2(2):

- 250mW conducted power
- 1.0W max EIRP

This limit is met with the highest gain antenna listed, World Products Inc WPANTE3.

The maximum antenna gain permitted in the band 5725-5825 MHz to comply with the e.i.r.p. limit specified for non point-to-point operation is, according to RSS-210 section A9.2(3):

- 1W conducted power.
- 4.0W max EIRP.

This limit is met with the highest gain antenna listed, World Products Inc WPANTE3.

OEM installers and users are cautioned to take note that high-power radars are allocated as primary users (meaning they have priority) of the bands 5250-5350 MHz and 5650-5850 MHz and these radars could cause interference and/or damage to devices operating in these frequency bands.

## Indoor/Outdoor

When the ConnectCore Wi-9P 9215 module is installed in devices that can be used outdoors, the channels in the band 5150-5250 MHz must be disabled to comply with US and Canadian regulatory requirements. The OEM users are encouraged to inform end users of this restriction as well.

## Declaration of Conformity

(In accordance with FCC Dockets 96-208 and 95-19)

|                                    |                                                 |
|------------------------------------|-------------------------------------------------|
| <b>Manufacturer's Name:</b>        | Digi International                              |
| <b>Corporate Headquarters:</b>     | 11001 Bren Road East<br>Minnetonka MN 55343     |
| <b>Manufacturing Headquarters:</b> | 10000 West 76th Street<br>Eden Prairie MN 55344 |

Digi International declares that the product:

|                       |                     |
|-----------------------|---------------------|
| <b>Product Name</b>   | ConnectCore 9P 9215 |
| <b>Model Numbers:</b> | FS-3029<br>FS-3038  |

and the product:

|                       |                         |
|-----------------------|-------------------------|
| <b>Product Name</b>   | ConnectCore Wi- 9P 9215 |
| <b>Model Numbers:</b> | FS-3044                 |

to which this declaration relates, meet the requirements specified by the Federal Communications Commission as detailed in the following specifications:

- Part 15, Subpart B, for Class B equipment
- FCC Docket 96-208 as it applies to Class B personal
- Personal computers and peripherals

The products listed above have been tested at an External Test Laboratory certified per FCC rules and have been found to meet the FCC, Part 15, Class B, Emission Limits. Documentation is on file and available from the Digi International Homologation Department.

**ConnectCore 3G 9P 9215:****Qualcomm  
Gobi 3000  
Module  
Certifications**

- TIA/EIA IS-98E (CDMA2000)
- TIA/EIA IS-866 (1xEV-DO)
- TS 25.101 (UMTS)
- TS 45.005 (GSM)
- CTIA/GCF/PTCRB
- FCC
  - 47 CFR Part 1, RF radiation exposure limits
  - 47 CFR Part 2, equipment authorization
  - 47 CFR Part 15, unintentional radiators
  - 47 CFR Part 22, cellular
  - 47 CFR Part 24, PCS
- CE
  - EMC protection requirements
    - EN 301 489-1, common technical requirements
    - EN 301 489-7, GSM and DCS
    - EN 301 489-24, WCDMA 2100
    - EN 301 489-25, CDMA2000
  - Effective use of spectrum to avoid unwanted interference requirements
    - EN 301 908-1, general requirements
    - EN 301 908-2, WCDMA 2100
    - EN 301 908-4, CDMA2000
    - EN 301 511 GSM900/1800
    - EN 301 607-1 GSM900/1800
- UICC: TS 51.101 & IEC-6801-3
  - Compliance dependent on platform characteristics
- USB 2.0 High Speed
  - Compliance dependent on platform characteristics
- Safety: EN 50360/61 full carrier certification
- Microsoft WHQL certification
- ROHS compliance

# International EMC Standards

The ConnectCore 9P 9215, ConnectCore Wi-9P 9215, and ConnectCore 3G 9P 9215 modules meet the following standards:

| Standards | ConnectCore 9P 9215                               |
|-----------|---------------------------------------------------|
| Emissions | FCC Part 15 Subpart B<br>ICES-003                 |
| Immunity  | EN 55022<br>EN 55024                              |
| Safety    | UL 60950-1<br>CSA C22.2, No. 60950-1<br>EN60950-1 |



# Appendix C: Change Log

The following changes were made to this document in revisions listed below.

## Revision B

- 1 Deleted the following non-applicable text: “Onboard flash: The module has 8Mx16 NOR by 2Mx16 NOR flash onboard. Greater sizes can optionally be populated, if available. “
- 2 Replaced “Current measurements with FIM (DRPIC) enabled” and “Current measurements with FIM (DRPIC) disabled” with “Typical module current / power measurements” and “Typical power save module / JumpStart board current / power consumption measurements.”

## Revision C

- 1 On page 9 updated Digi information.
- 2 On page 43 within Serial Port B MEI configuration switches table, deleted no applicable reference to RS422/RS485 regarding S1.1.
- 3 On page 48 corrected Serial UART ports figure callout arrows.
- 4 On page 60 regarding POWE\_GND, corrected from X24 to X26.4 and X26.5.
- 5 On page 72 corrected figure of module top.

## Revision D

- 1 Made additions necessary to accomodate additional device, CCWi-9P 9215.

## Revision E

- 1 Made corrections to current draw information.

## Revision F

- 1 Minor data corrections were made and Canadian certifications information was expanded.

## Revision G

- 1 On page 92, corrected FCC ID number.

## Revision H

- 1 On page 87, corrected the 5.5 dBi Dipoles antenna's part number within the attributes table.

## Revision I

- 1 Removed "5V tolerant" from the I<sup>2</sup>C digital I/O expansion section.

## Revision J

- 1 Revised the WLAN Interface section of Appendix A.

## Revision K

- 1 Added ConnectCore 3G 9P 9215 information to the manual.

## Revision L

- 1 Revised the Strapping Options table in Appendix C.

- 2 Revised the Configuration Pins section text of Chapter 1.
- 3 Revised the User Interface section of Chapter 2.
- 4 Added text describing the WWAN Interface section of Chapter 2.
- 5 Renamed the Typical Power Save Current /Power Measurements section ConnectCore 9P 9215 and ConnectCore Wi-9P 9215 Typical Power Save Current / Power Measurements in Appendix A. Also, added the ConnectCore 3G 9P 9215 Typical Power Save Current/ Power Measurements section to Appendix A.
- 6 Revised the Typical Module Current/ Power Measurements section of Appendix A.

## Revision M

- 1 Revised bullet 17 of the Features and Functionality section of Chapter 1.

## Revision N

- 1 Added information for Digi Plug-and-Play software users to Chapter 1.
- 2 Added ConnectCore 3G 9P 9215 GPS antenna information to Appendix A.
- 3 Added 802.11a available transmit power settings to Appendix A.

## Revision P

**Note:** Revision O is not used.

- 1 Revised the “Module Functionality” and “I/O Multiplexing” descriptions for pins 1, 2, 45, 76, 77, 78, 79, and 80 in the X2 Pinout table of Chapter 1.

## Revision R

**Note:** Revision Q is not used.

- 1 Added a comment to all tables of Chapter 1 containing EIRQ0 regarding this item’s availability.



