CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX970
IF/RF Quadrature Demodulator

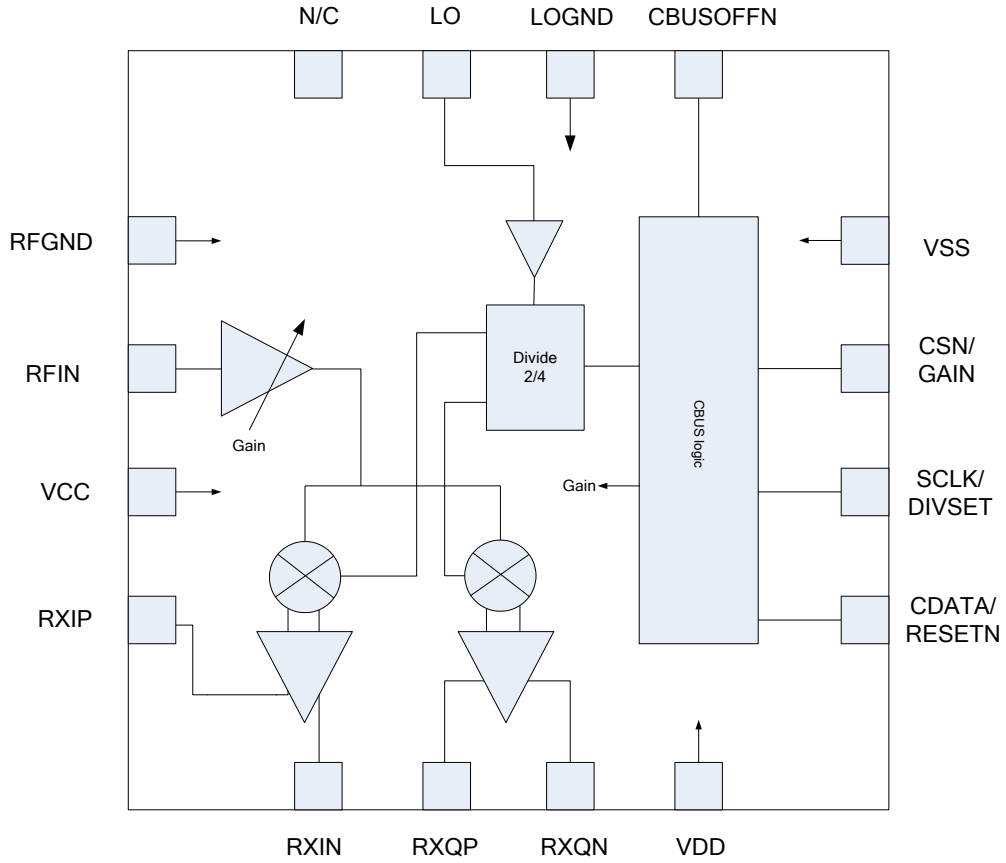
D/970/10 April 2022 Provisional Issue

Features

- 20 – 300 MHz IF/RF Demodulator
- 10MHz I/Q Bandwidth
- Serial Bus or Direct Control Operation
- Variable Gain and DC Offset Adjustments
- Low Power 3.0V – 3.6V Operation
- Small 16-lead VQFN Package

Applications

- Wireless Data Terminals
- HF/VHF and UHF Mobile Radio
- Avionics Radio Systems



1 Brief Description

The CMX970 is a low power IF or RF quadrature demodulator featuring a wide operating frequency range and low power consumption. Suitable for architectures with IF or RF frequencies up to 300MHz the device may be used in low IF systems or those converting down to baseband. Control of the CMX970 may be either by serial bus or by direct control (with reduced functionality). The small, RF-optimised VQFN package and minimal external components make the device ideal for space-constrained applications.

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CONTENTS

Section Page

1 Brief Description 1

2 Block Diagram 4

3 Pin and Signal List 5
3.1 Main Functions 5
3.2 Direct Control Functions 5

4 External Components 6
4.1 Power Supply Decoupling 6
4.2 Quadrature Demodulator 7
4.3 Local Oscillator (LO) Input 7

5 General Description 8
5.1 Programmable Data Interface 8
5.2 Quadrature Demodulator 8
5.2.1 I/Q Amplitude and Phase Correction 9
5.2.2 DC Offset Correction 11
5.3 Local Oscillator (LO) 11

6 C-BUS Interface and Register Description 12
6.1 General Reset Command 13
6.1.1 General Reset Command C-BUS address $1A 13
6.2 General Control Register 13
6.2.1 General Control Register: C-BUS address $1B 13
6.3 Control Register 14
6.3.1 Control Register: C-BUS address $1C 14
6.4 Mode Register 15
6.4.1 Mode Register: C-BUS address $1D 15
6.5 Offset Register 16
6.5.1 Offset Register: C-BUS address $1F 16
6.6 Intermod Control Register 17
6.6.1 Intermod Control Register: C-BUS address $2F 17

7 Direct Control Option 18

8 Application Notes 20
8.1 IF/RF Input Matching 20
8.2 Receiver Intermodulation and Output Drive Capability 21
8.3 Receiver Variation with Temperature 22
8.4 Effect of Gain Control on Receiver Performance 23
8.5 Measurement of CMX970 Demodulator Intermodulation Performance 25
8.6 Operation with large input signals 26

9 Performance Specification 27
9.1 Electrical Performance 27
9.1.1 Absolute Maximum Ratings 27
9.1.2 Operating Limits 27
9.1.3 Operating Characteristics 28
9.2 Packaging 32

Section Page
Table 1 Main Pin Functions 5
Table 2 Direct Control Pin Functions 5
Table 3 Power Supply Component Values 6
Table 4 Quadrature Demodulator Input Components 7
Table 5 Typical Phase Balance in Divide by 2 Mode 9
Table 6 FREQ bit Settings in the Mode Register 9
Table 7 Effect of FREQ bits ($1D, b3-b0) on I/Q Phase Balance at 250MHz 10
Table 8 Effect of FREQ bits ($1D, b3-b0) on I/Q Phase Balance at 300MHz with Temperature 10
Table 9 DC Offset Correction Adjustments 11
Table 10 Direct Control Pin Functions 18
Table 11 Quadrature Demodulator Input Impedance and Parallel Equivalent Circuit 20
Table 12 Typical Noise Figure and Gain of IF Amp, VGA and I/Q Mixer 21
Table 13 Typical Third Order Intercept Performance of Receiver at 45MHz (straight-in case) 21

Section Page
Figure 1 Block Diagram 4
Figure 2 Power Supply Connections and Decoupling 6
Figure 3 RF Input Matching Circuit 7
Figure 4 LO Input Configuration 7
Figure 5 Demodulator Gain Control 8
Figure 6 Frequency Response, showing effect of COR bit ($1C, b6) and FREQ bits($1D, b3-b0) 10
Figure 7 Simplified Schematic of DC Offset Correction 11
Figure 8 C-BUS Transactions 13
Figure 9 Quadrature Demodulator Input Impedance (10MHz to 300MHz) 20
Figure 10 Demodulator Gain Variation With Temperature 22
Figure 11 Variation in Gain with Temperature (COR = '0' $1D = 0x00) 22
Figure 12 Variation in CMX970 Demodulator Noise Figure with VGA/VGB Control 23
Figure 13 Variation in Input Third Order Intercept Point with VGA/VGB Control 24
Figure 14 Variations in Signal and IMD Product Levels 25
Figure 15 Output Signal Level Variations with Large Input Signals 26
Figure 16 C-BUS Timing 31
Figure 17 Q7 Mechanical Outline: *Order as part no.* CMX970*Q7* 32

History

Version	Changes	Date
10	• Section 8.6: updated input 1dB compression point • Section 8.6: new Figure 15 Gain v Input level at IF of 45MHz	26/04/22
8 / 9	N/A	-
7	• Correction to LO frequency range and i/p impedance	17/2/15
6	• Gain compression information added (section 8.6); related clarifications.	16/11/12
5	• Rx operation to 300MHz	18/6/12
4	• Additional information on FREQ bit settings, section 5.2.1 • Updated parametric information, after further characterisation	17/5/12
3	• Update to front page, Mode register and package drawing	14/3/12
2	• Corrections to Direct Mode description	27/2/12
1	• First Issue	15/2/12

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2 Block Diagram

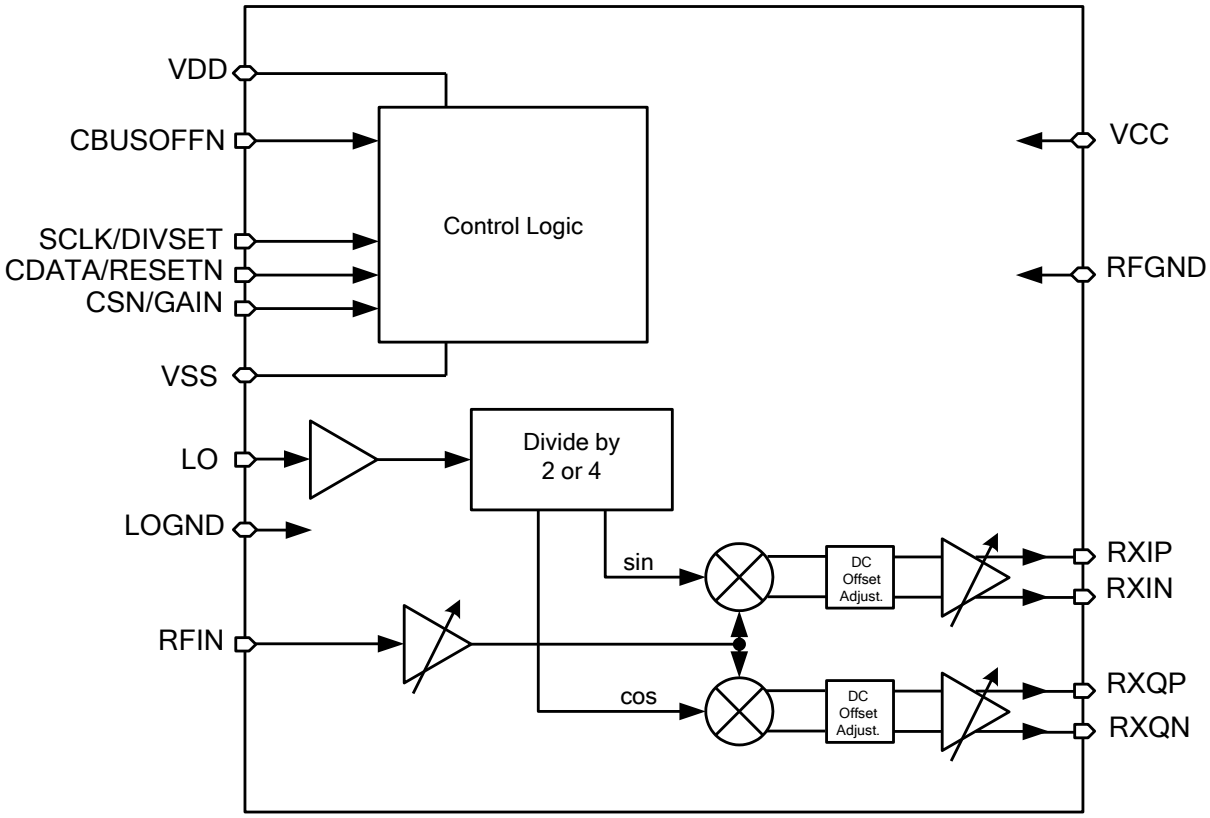


Figure 1 Block Diagram

3 Pin and Signal List

3.1 Main Functions

Pin	Name	Type	Signal Description
1	RFGND	PWR	Analogue and RF ground
2	RFIN	IP	IF or RF input signal
3	VCC	PWR	Analogue and RF supply
4	RXIP	OP	Analogue output for baseband receive I signal (positive)
5	RXIN	OP	Analogue output for baseband receive I signal (negative)
6	RXQP	OP	Analogue output for baseband receive Q signal (positive)
7	RXQN	OP	Analogue output for baseband receive Q signal (negative)
8	VDD	PWR	C-BUS and digital supply
9	CDATA / RESETN*	IP	C-BUS data-in
10	SCLK / DIVSET*	IP	C-BUS clock input
11	CSN / GAIN*	IP	C-BUS chip select
12	VSS	PWR	C-BUS and digital ground
13	CBUSOFFN	IP	Disable pin for C-BUS operation. If held low, direct control pin functions are selected as described in Table 2 and it enables demodulator sections (equivalent to General Control register b1 and b4 = '1', see section 6.2.1). Internal ≈1MΩ pullup resistor.
14	LOGND	PWR	LO buffer ground
15	LO	IP	Analogue input for local oscillator signal
16	–	NC	No connection. Do not connect to this pin
~	EXPOSED METAL PAD	PWR	Substrate. Connect to Analogue and RF ground
* Direct control functions for these pins selected if CBUSOFFN pin = '0', see Table 2			

Table 1 Main Pin Functions

Notes: IP = Input
OP = Output
PWR = Power Connection
NC = No connection – should NOT be connected to any signal

3.2 Direct Control Functions

When C-BUS is disabled (CBUSOFFN pin is low), pins 9, 10 and 11 have the following functions (Table 2). Every time the CBUSOFFN pin is held low the registers of the device are placed in the RESET state (section 6.1.1), except ENBIAS and RXEN (see section 6.2.1) which are active. The functions listed in Table 2 are then controlled by the appropriate pins.

Pin	Function
9	**RESETN** - when low puts the device into low power mode. No internal pullup resistor.
10	**DIVSET** - if low sets mixer input to local oscillator divide by two, if high sets mixer input to local oscillator divide by four (equivalent to the inverse of bit 7 of General Control register, section 6.2.1 and section 7.)
11	**GAIN** – if low sets VGA and VGB overall gain to -18dB, if high sets VGA and VGB gain to maximum (0dB)

Note: local oscillator divide by two and local oscillator divide by four will hereafter be referred to as LO/2 and LO/4 respectively.

Table 2 Direct Control Pin Functions

4 External Components

4.1 Power Supply Decoupling

The CMX970 has separate supply pins for the RF/analogue and digital circuitry; a 3.3V nominal supply is recommended for all circuits. It is recommended that the digital supply be decoupled from the RF and analogue supply; an example of such decoupling is shown in Figure 2.

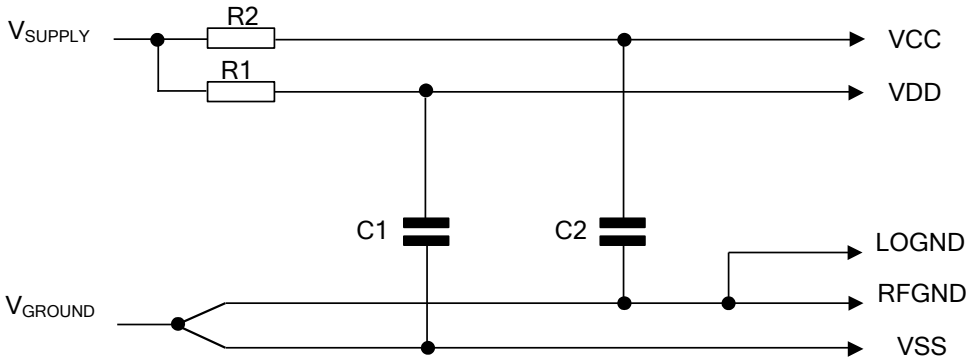


Figure 2 Power Supply Connections and Decoupling

C1	10nF	R1	10Ω
C2	10nF	R2	3.3Ω

Resistors ±1%, capacitors ±20%

Table 3 Power Supply Component Values

Note:

It is expected that low-frequency interference on the 3.3V supply will be removed by active regulation. A large capacitor is an alternative but may require more board space and so may not be preferred. The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well. This may be achieved cost effectively using the resistor as shown. The use of resistors results in small dc voltage drops. Choosing resistor values approximately inversely proportional to the dc current requirements of each supply pin ensures the dc voltage drop on each supply is reasonably matched. In any case, the dc voltage change that results is well within the design tolerance of the device. If higher impedance resistors are used then greater care will be needed to ensure that the supply voltages are maintained within tolerance, including when parts of the device are enabled or disabled.

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4.2 Quadrature Demodulator

The input impedance of the demodulator section is shown in section 8.1. The input can be driven from a 50 Ohm source or can be matched to 50 Ohms. A typical 50 Ohm matching circuit is shown in Figure 3 for operation at 45MHz.

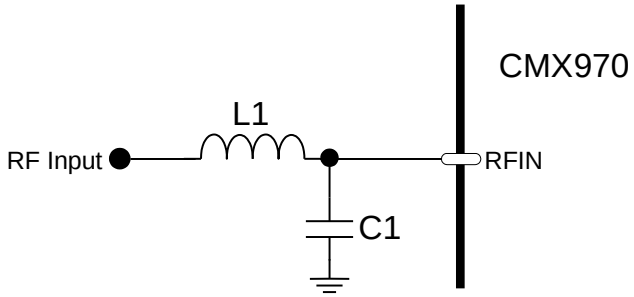


Figure 3 RF Input Matching Circuit

L1	910nH
C1	10pF

Table 4 Quadrature Demodulator Input Components

4.3 Local Oscillator (LO) Input

The CMX970 has a single-ended LO input. Users should be aware that the presence of high levels of harmonics in the signal applied to the LO input might degrade quadrature accuracy.

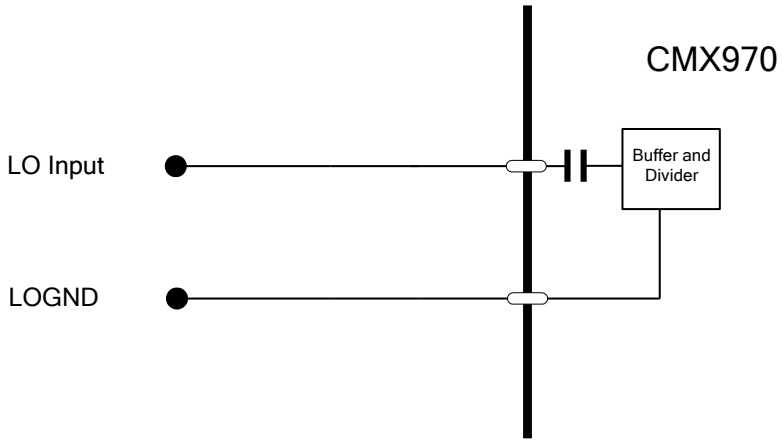


Figure 4 LO Input Configuration

A separate ground pin (LOGND) is used for the LO buffer to allow routing of the ground feed to the device such that any coupling, via the ground plane, between the LO signal and the RF signal can be minimised. In most cases it will be sufficient to just connect this to the RFGND ground plane, although it may be advantageous to supply LOGND from the ground supply for the LO generator or to star-connect the LO generator ground and the LOGND at a single point on the ground plane.

5 General Description

The CMX970 device is an RF integrated circuit providing a quadrature demodulator. A detailed block diagram for the IC is shown in Figure 1. The device can support a wide range of modulation formats. The following sections describe its functionality.

5.1 Programmable Data Interface

The CMX970 may be controlled via its C-BUS serial interface (see section 6). Alternatively, the device can be used under direct control, with reduced programmability. This can be advantageous in systems without a host controller (see section 7).

5.2 Quadrature Demodulator

The quadrature demodulator is designed for IF/RF operation and has very low power consumption. Input frequencies in the range 20MHz to 300MHz are allowed. The demodulator system has two gain-controlled stages, one before and one after the I/Q down-converters, as shown in Figure 5. The two gain control elements can be independently controlled (see section 6.3.1). This flexible architecture allows the users to optimise characteristics depending on their system requirements. Minimum noise figure can be maintained by decreasing gain in VGA with VGB at maximum gain. Intermodulation performance can be optimised by decreasing gain in VGA or VGB. A lower gain in VGA will tend to reduce dc offsets in the output I/Q signal. For further information on the effects of controlling VGA and VGB, see section 8.4.

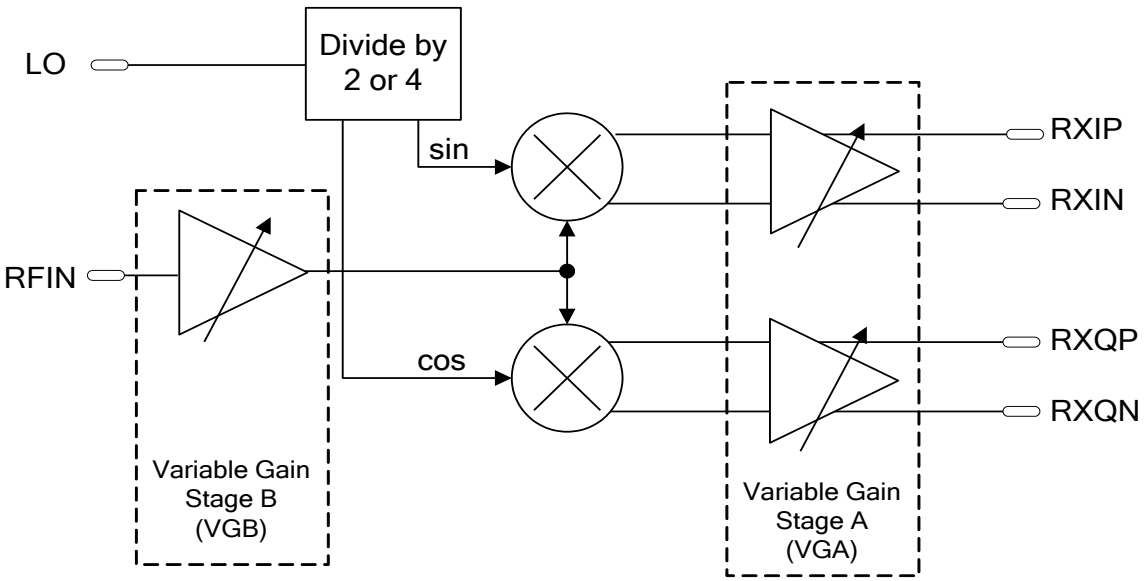


Figure 5 Demodulator Gain Control

The output of the I/Q demodulator is provided as a differential signal (pins RXIP, RXIN, RXQP, RXQN). The bandwidth of the I/Q signals depends on the OUTDRV bit (b7 in the Control register $1C, see section 6.3.1). The CMX970 provides for an optimisation of receiver intermodulation using the “IMD” bits in the Intermod Control register ($2F), further details can be found in section 6.6.

5.2.1 I/Q Amplitude and Phase Correction

The local oscillator path includes a correction circuit for the quadrature demodulator which may be enabled or disabled using the COR bit (b6 in the Control register $1C), see section 6.3.1. When enabled, this will improve the I/Q balance of the demodulator particularly when using the Local Oscillator in divide by two mode; enabling this correction circuit will give a small increase in current consumption of ≈0.5mA. The improvement is most noticeable with higher frequency signals, e.g. circa 200 - 300MHz; at ≈45MHz the improvement is negligible.

	250MHz		45MHz	
Condition	**RXIP / RXQP**	**RXIN / RXQN**	**RXIP / RXQP**	**RXIN / RXQN**
$1C, b6 = '0'	92.0°	92.0°	90.1°	90.2°
$1C, b6 = '1'	89.8°	89.8°	89.9°	89.9°

Table 5 Typical Phase Balance in Divide by 2 Mode

At 250MHz I/Q amplitude balance is typically 0.12dB with COR = '0' and 0.04dB with COR = '1'. Enabling the correction circuit also reduces the I/Q path gain, particularly at higher frequencies. This can be compensated by setting the FREQ bits (b3-0 in the Mode register $1D) to '1111', instead of the default value of '0000'. I/Q path gain is restored at the expense of a slight degradation in I/Q phase balance of ≈0.5°. For many applications, the '1111' setting will be adequate.

At all frequencies, phase correction accuracy is improved by using a lower setting of the FREQ bits (b3-0 in the Mode register $1D). However, care should be taken to avoid significant gain degradation, which occurs if a setting near '0000' is chosen for a high frequency. Table 6 is a guide for the appropriate setting of the FREQ bits, so as to obtain the best phase balance (typically better than 0.06°) with only a small gain reduction (typically less than 0.6dB). Where frequency ranges overlap, either setting of the FREQ bits can be used.

Bit b3	b2	b1	b0	Frequency
0	1	0	0	20MHz to 40MHz
1	0	0	0	40MHz to 80MHz
1	1	0	0	80MHz to 200MHz
1	1	0	1	200MHz to 240MHz
1	1	1	0	240MHz to 300MHz

Table 6 FREQ bit Settings in the Mode Register

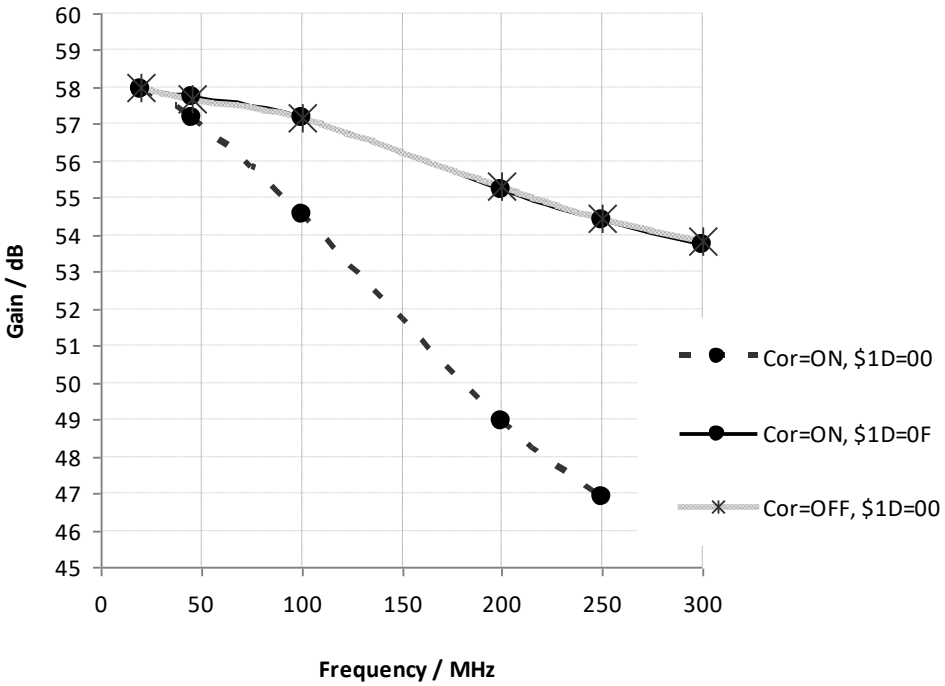


Figure 6 Frequency Response, showing effect of COR bit ($1C, b6) and FREQ bits($1D, b3-b0)

Condition	Typical I/Q Phase Balance
COR = '0' $1D = 0x00	87.95°
COR = '1' $1D = 0x00	90.06°
COR = '1' $1D = 0x0F	90.49°

Table 7 Effect of FREQ bits ($1D, b3-b0) on I/Q Phase Balance at 250MHz

Condition	Typical I/Q Phase Balance
COR = '0' $1D = 0x00, +20°C	87.3°
COR = '1' $1D = 0x0F, -20°C	90.6°
COR = '1' $1D = 0x0F, +20°C	90.6°
COR = '1' $1D = 0x0F, +55°C	90.5°

Table 8 Effect of FREQ bits ($1D, b3-b0) on I/Q Phase Balance at 300MHz with Temperature

5.2.2 DC Offset Correction

Digitally controlled dc offset correction is provided which is capable of reducing the offset to 60mV or less for errors of up to +/-420mV. This represents a reduction in dynamic range of about 0.3dB for a typical ADC input signal range (2Vp-p) and is therefore negligible. The required correction must be measured externally as such measurements are application specific. The correction is applied close to the start of the I/Q baseband chain and therefore maximises dynamic range in the analogue sections.

The correction is applied in a differential manner so positive and negative corrections are possible, see Figure 7. This allows the dc to be corrected to the nominal dc bias level. The voltage sources are scaled in a binary fashion so multiple sources can be added to provide the desired correction. The same arrangement applies independently on both I and Q channels.

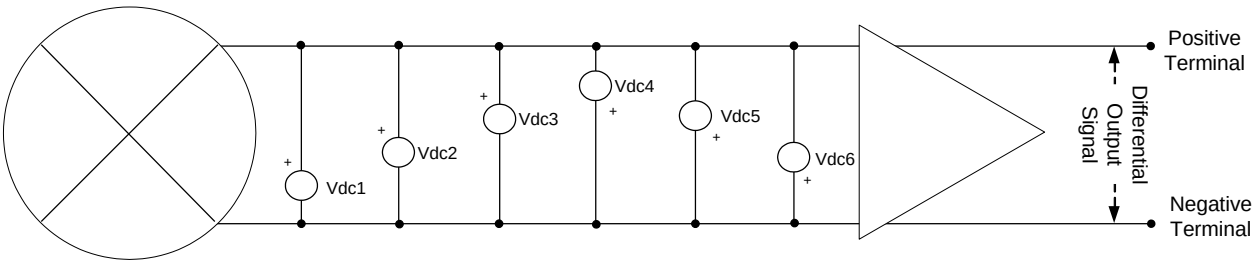


Figure 7 Simplified Schematic of DC Offset Correction

Source	Voltage Correction at Output for Maximum Gain in Baseband Amplifiers	Correction Polarity
Vdc1	60mV	Positive terminal increase, Negative terminal decreases
Vdc2	120mV	Positive terminal increase, Negative terminal decreases
Vdc3	180mV	Positive terminal increase, Negative terminal decreases
Vdc4	60mV	Negative terminal increase, Positive terminal decreases
Vdc5	120mV	Negative terminal increase, Positive terminal decreases
Vdc6	180mV	Negative terminal increase, Positive terminal decreases

Table 9 DC Offset Correction Adjustments

5.3 Local Oscillator (LO)

The LO pin is a single-ended input for the demodulator local oscillator signal. Internal ac coupling is provided so an external dc blocking capacitor is not required, see Figure 4. Note that the LO should be at two or four times the desired RFIN input frequency.

6 C-BUS Interface and Register Description

The C-BUS serial interface supports the transfer of control and status information between the CMX970's internal registers and an external host. Each C-BUS transaction consists of the host sending a single Register Address byte, which may then be followed by zero or one data byte that is written into the corresponding CMX970 register, as illustrated in Figure 8.

Data sent from the host on the Command Data (CDATA) line is clocked into the CMX970 on the rising edge of the Serial Clock (SCLK) input. The C-BUS interface is compatible with common µC/DSP serial interfaces and may also be easily implemented with general purpose I/O pins controlled by a simple software routine. Section 9.1.3.4 gives the detailed C-BUS timing requirements.

Whether a C-BUS register is of read or write type is fixed for a given C-BUS register address, thus it is not possible to read from and write to the same C-BUS register address.

In order to provide ease of addressing when using this device with other CML RF devices the C-BUS addresses below are arranged so as not to overlap those used on the existing CML RF Devices. Thus, a common chip select (CSN) signal can be used, as well as common CDATA, RDATA and SCLK signals. Also note that the General Reset ($1A) command on the CMX970 differs from other CML devices (such as CMX991 / CMX992 / CMX993 / CMX998), which use $01 or $10 for this function.

The CMX970 uses only write-type registers.

The C-BUS functions can be disabled in the CMX970 by using the CBUSOFFN pin, see section 3 for details. The CBUSOFFN pin should be tied high to enable C-BUS operation.

The following C-BUS register addresses are used:

General Reset register (Address only, no data)	Address $1A
General Control register, 8-bit write only.	Address $1B
Control register, 8-bit write only.	Address $1C
Mode register, 8-bit write only.	Address $1D
Offset Correction register, 8-bit write only	Address $1F

Notes:

- All registers will retain data if the VDD pin is held high, even if all other power supply pins are disconnected.
- If clock and data lines are shared with other devices, the VDD pin must be maintained in its normal operating range otherwise ESD protection diodes may cause a problem with loading signals connected to SCLK and CDATA pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the device may be powered down without causing this problem.

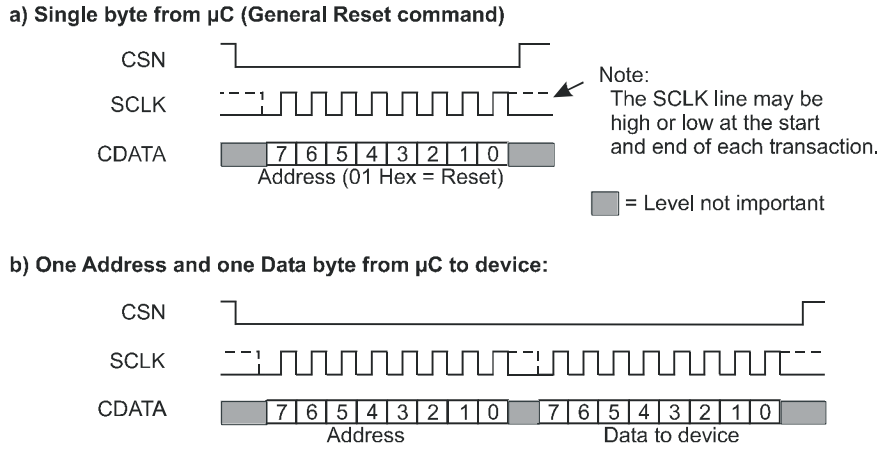


Figure 8 C-BUS Transactions

6.1 General Reset Command

6.1.1 General Reset Command C-BUS address $1A (no data)

This command resets the device and clears all bits of all registers. The General Reset command places the device into powersave mode.

Whenever power is applied to the VDD pin, a built-in power-on-reset circuit ensures that the device powers up into the same state as follows a General Reset command. If the C-BUS is disabled, the RESETN pin on the device will also place the device into the same state whilst the pin is held low.

6.2 General Control Register

8-bit write-only

6.2.1 General Control Register: C-BUS address $1B

This register controls general features such as powersave.

All bits of this register are cleared to '0' during a General Reset command.

Note:
b1 (RXEN) and b4 (ENBIAS) are high if pin CBUSOFFN is low.

Bit:	7	6	5	4	3	2	1	0
	RXDIV	0	0	ENBIAS	0	0	RXEN	0

General Control Register b7, b4 and b1

Writing b7 = '1' the LO is divided by 2; writing b7 = '0' the LO is divided by 4.
Writing b4 = '1' Enables internal bias current supplies.
Writing b1 = '1' Enables the quadrature demodulator.

All other bits are reserved and must be set to '0' for correct operation.

6.3 Control Register

6.3.1 Control Register: C-BUS address $1C

8-bit write-only

This register controls operational modes such as gain setting.

All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	OUTDRV	COR	0	VGB2	VGB1	VGB0	VGA1	VGA0

Control Register b7

Writing b7 = '1' the output drive capability of the demodulator I/Q output is increased, this mode allows the CMX970 to support wider bandwidth modulation and/or drive lower impedance loads; b7 = '0' is the default condition with best power efficiency.

Control Register b6

Writing b6 = '1' enables the correction circuit in the quadrature demodulator. This will improve the I/Q phase balance of the demodulator, particularly in Local Oscillator divide by two mode; enabling this circuit increases the current consumption slightly. For further information see section 5.2.1.

With b6 = '0' this phase correction circuit is disabled for optimum current consumption.

Control Register b5

Reserved, must be set to '0' for correct operation.

Control Register b4 – b2

Variable Gain (VGB) control; these bits control the gain of the IF/RF amplifier, reducing the gain from the maximum in 6dB steps.

Bit	b4	b3	b2	
	1	1	1	Reserved, do not use
	1	1	0	Reserved, do not use
	1	0	1	VG = -30dB
	1	0	0	VG = -24dB
	0	1	1	VG = -18dB
	0	1	0	VG = -12dB
	0	0	1	VG = -6dB
	0	0	0	VG = 0dB (maximum gain)

Control Register b1 – b0

Variable Gain (VGA) control; these bits control the gain of the post-I/Q mixer baseband amplifiers, reducing the gain from the maximum in 6dB steps.

Bit	b1	b0	
	1	1	VG = -18dB
	1	0	VG = -12dB
	0	1	VG = -6dB
	0	0	VG = 0dB (maximum gain)

6.4 Mode Register

6.4.1 Mode Register: C-BUS address $1D
8-bit write-only

This register controls the operational mode of the receiver.

All bits of this register are cleared to ‘0’ by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	M1	M0	0	0	FREQ3	FREQ2	FREQ1	FREQ0

Mode Register b7 – b6

Bit	b7	b6	
	0	0	I and Q channels enabled
	0	1	Only I channel enabled
	1	0	Only Q channel enabled
	1	1	Reserved. do not use

Mode Register b5 - b4

Reserved, must be set to ‘0’ for correct operation.

Mode Register b3 – b0

These bits optimise the operation of the receiver quadrature demodulator mixers by adjusting the LO signal. The bits adjust LO amplitude, which has an impact on mixer gain, but the adjustment also has an effect on quadrature accuracy. See also section 5.2.1. Note that if Control register ($1C) b6 is set to 0, so that phase correction is not being employed, these bits have no effect.

‘0000’ represents the optimum value for phase accuracy.

6.5 Offset Register

6.5.1 Offset Register: C-BUS address $1F

8-bit write-only

All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	QDC3	QDC2	QDC1	QDC0	IDC3	IDC2	IDC1	IDC0

Offset Register b7 – b0

I/Q dc offset correction, see section 5.2.2 for further details.

Bit	b3 b7	b2 b6	b1 b5	b0 b4	I Channel Q Channel
	1	1	1	1	-420mV
	1	1	1	0	-360mV
	1	1	0	1	-300mV
	1	1	0	0	-240mV
	1	0	1	1	-180mV
	1	0	1	0	-120mV
	1	0	0	1	-60mV
	1	0	0	0	No correction
	0	1	1	1	+420mV
	0	1	1	0	+360mV
	0	1	0	1	+300mV
	0	1	0	0	+240mV
	0	0	1	1	+180mV
	0	0	1	0	+120mV
	0	0	0	1	+60mV
	0	0	0	0	No correction

6.6 Intermod Control Register

6.6.1 Intermod Control Register: C-BUS address $2F
8-bit write-only

This register optimises the receiver intermodulation performance. All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	IMD5	IMD4	IMD3	IMD2	IMD1	IMD0	0	0

Intermod Control Register b7 – b2

These bits allow the user to adjust the intermodulation performance of the Rx I/Q mixers. The default value is '0' for all the bits. Improved intermodulation can be achieved with a particular value in these bits. The recommended value for optimum performance is '111111'. This value does not vary between devices or with frequency.

Intermod Control Register b1 – b0

Reserved, must be set to '0' for correct operation.

7 Direct Control Option

As an alternative to the C-BUS method of controlling the device, the CMX970 has the option of using a direct method to control some of the device settings. This is particularly useful in systems that do not require a microcontroller. The settings are limited to being able to reset the device, set the LO divider to LO/2 or LO/4 and set the VGA and VGB gain to maximum (0dB) or to -18dB, equivalent to setting the Control register $1C (b7 – b0) to '01001001' (see section 6.3.1). The I/Q demodulator correction circuit,dc offset correction and intermodulation control are disabled.

The Direct Control Option is selected by holding the CBUSOFFN pin low. This changes the function of the C-BUS pins (CDATA, SCLK and CSN) to those defined in Table 2 (these are RESETN, DIVSET and GAIN respectively), reproduced below as Table 10. Other register settings adopt the values shown in this section.

The device behaviour with CBUSOFFN = 0 is as follows:

RESETN, if asserted by taking the pin low, behaves like a C-BUS General Reset in that all registers will go to an all zero state and the device will go into a low power mode.

When RESETN is deasserted the device comes out of low power mode and enters its active state. In the active state the RESETN, DIVSET and GAIN pins have the following functionality.

Function	Pin at V_{DD}	Pin at V_{SS}
RESETN	Active mode	Low power mode, device reset
DIVSET	Divide by 4	Divide by 2
GAIN	Maximum gain	VGA gain –6 dB VGB gain –12 dB

Table 10 Direct Control Pin Functions

The C-BUS registers will be automatically configured as follows:

General Control Register: C-BUS address $1B

b7	b6	b5	b4	b3	b2	b1	b0
RXDIV			ENBIAS			RXEN	
See below	0	0	1	0	0	1	0

If DIVSET is low, b7 = 1 and the LO is divided by 2
If DIVSET is high, b7 = 0 and the LO is divided by 4

Control Register: C-BUS address $1C

b7	b6	b5	b4	b3	b2	b1	b0
OUTDRV	COR		VGB2	VGB1	VGB0	VGA1	VGA0
0	0	0	See below				

If GAIN is high then b4, b3, b2, b1, b0 = 0 so that the VGA and VGB gain is set to maximum (0dB)
If GAIN is low then b4, b3, b2, b1, b0 = 0, 1, 0, 0, 1 so that the overall VGA and VGB gain is set to -18 dB

Mode Register: C-BUS address $1D

b7	b6	b5	b4	b3	b2	b1	b0
M1	M0			FREQ3	FREQ2	FREQ1	FREQ0
0	0	0	0	1	1	1	1

Offset Register: C-BUS address $1F

b7	b6	b5	b4	b3	b2	b1	b0
QDC3	QDC2	QDC1	QDC0	IDC3	IDC2	IDC1	IDC0
0	0	0	0	0	0	0	0

Intermod Control Register: C-BUS address $2F

b7	b6	b5	b4	b3	b2	b1	b0
IMD5	IMD4	IMD3	IMD2	IMD1	IMD0	0	0
0	0	0	0	0	0	0	0

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8 Application Notes

8.1 IF/RF Input Matching

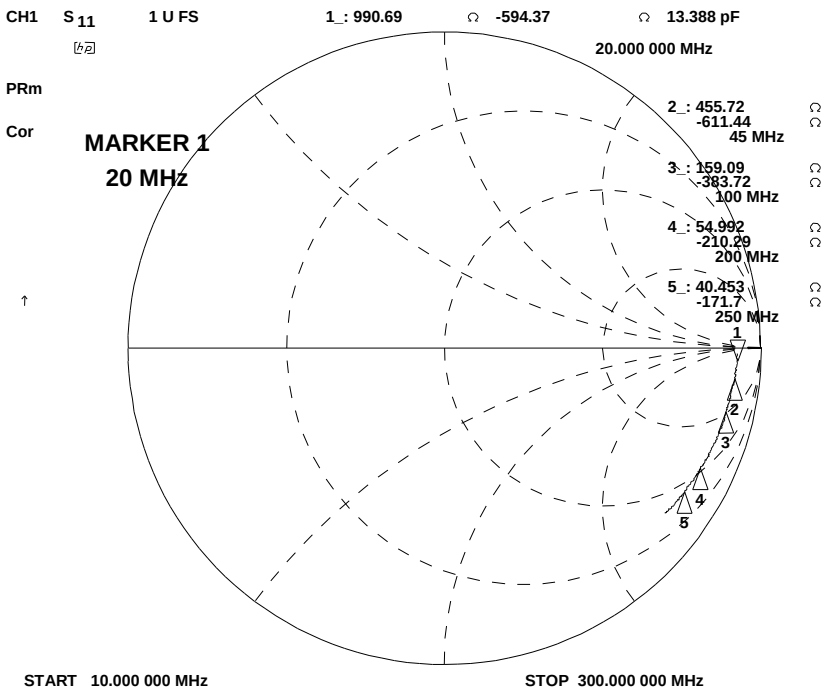


Figure 9 Quadrature Demodulator Input Impedance (10MHz to 300MHz)

Frequency (MHz)	Typical Impedance (Ω-/+jΩ)	Parallel Equivalent Circuit (R//pF)
20	991 - j594	1.35kR // 3.5pF
45	456 - j611	1.28kR // 3.7pF
100	159 - j384	1.08kR // 3.5pF
200	55 - j210	860.5R // 3.5pF
250	41 - j172	768.4R // 3.5pF

Table 11 Quadrature Demodulator Input Impedance and Parallel Equivalent Circuit

The typical input impedance of the RFIN port is shown in Figure 9 and Table 11. The configuration of this RF/IF input has a significant effect on the measured performance. This is demonstrated in Table 12, where the receiver is measured with a 50 Ohm source and three different input conditions. A matched network (as shown in section 4.2) provides the best noise figure and maximum gain, however intermodulation will be degraded in this condition due to the larger signal levels indicated by the extra gain. The 'straight in' condition means that the 50 Ohm signal source was connected directly at RFIN.

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Input Condition	Noise Figure / dB	Gain / dB
50R shunt resistor	16.3	50.5
matched network	7.8	64.0
straight in	10	56.0

Table 12 Typical Noise Figure and Gain of IF Amp, VGA and I/Q Mixer

The gain in the 'straight in' case is based on direct conversion of the signal generator power to a voltage and calculating the gain based on the output voltage. The output signal is the differential signal at RXIN / RXIP (or RXQN / RXQP) so if the voltage is measured at a single pin the signal level must be doubled to get the appropriate differential signal level. Also it should be noted that making a simple conversion of the power in the 'straight in' case is erroneous as the voltage calculated will be a potential difference. As the circuit is un-matched, an e.m.f. would be more appropriate (i.e. twice the potential difference value).

8.2 Receiver Intermodulation and Output Drive Capability

The intermodulation performance of the receiver path may be optimised by use of the output drive bit (Control register $1C b7, see section 6.3.1).Performance can be further optimised by setting the IMD bits in the Intermod Control register (register $2F b2 to b7) to '111111' = 63 decimal.

IMD bits setting (register $2F b2 to b7) decimal value	$1C, b7='0' 50kHz & 100 kHz tones	$1C, b7='1' 50kHz & 100kHz tones	$1C, b7='0' 500kHz & 1MHz tones	$1C, b7='1' 500kHz & 1MHz tones
0	-23 dBm	-12 dBm	-24 dBm	-12 dBm
63	-19 dBm	-11 dBm	-24 dBm	-11 dBm

Table 13 Typical Third Order Intercept Performance of Receiver at 45MHz (straight-in case)

8.3 Receiver Variation with Temperature

The quadrature demodulator exhibits excellent stability with temperature; typical variation of the receive-path gain is shown in Figure 10. The I/Q gain/phase balance, dc level and attenuator steps also show only small variations with temperature.

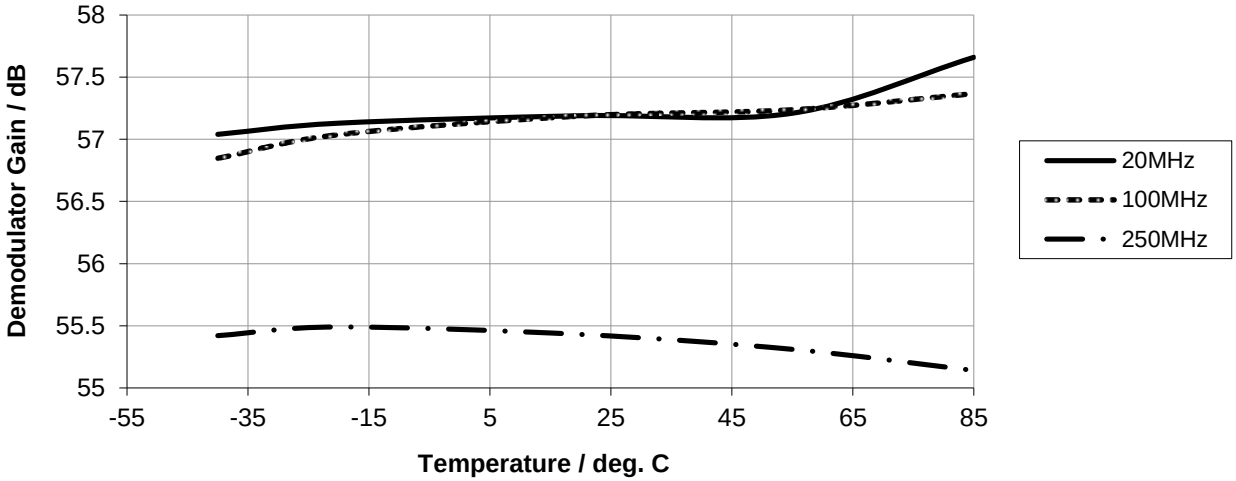


Figure 10 Demodulator Gain Variation With Temperature

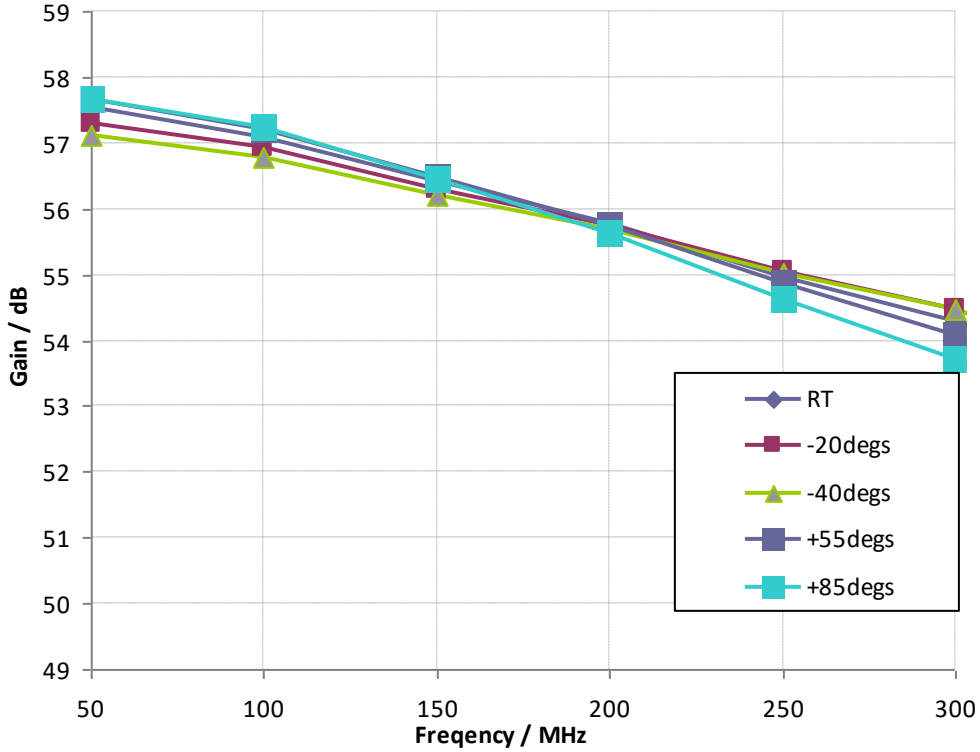


Figure 11 Variation in Gain with Temperature (COR = '0' $1D = 0x00)

8.4 Effect of Gain Control on Receiver Performance

The CMX970 has two independent gain control elements: VGA is the gain control applied in the I/Q sections and VGB is the gain control in the RF/IF sections; further details can be found in section 5.2. The gain can be controlled in 6dB steps via the Control register (see section 6.3.1).

The control of gain using VGA and VGB has an impact on the performance of the CMX970 demodulator. The variation in noise figure (NF) is straight forward, with the IF gain control (VGB) having a direct impact on NF but, due to the gain before the I/Q section, VGA has little impact on NF (see Figure 12). The variation of intermodulation (IMD) is more complex, as shown in Figure 13, where performance is characterised by 'Input Third Order Intercept Point' (IIP3). At maximum gain IIP3 is at a minimum and, as would be expected, the IIP3 increases as the IF gain is reduced (VGB). The improvement reaches a plateau beyond the -18dB gain setting as the input stages limit performance at this level. Reduction in gain with VGA (I/Q gain control) also has a positive effect on IIP3. This is perhaps less intuitive but indicates that the intermodulation performance of the CMX970 demodulator chain is dominated by the output stages rather than IF or mixer stages. Thus –6dB or even –12dB VGA gain control settings can be used to achieve improved IMD performance for negligible change in noise figure (Figure 12), as long as the reduction in gain can be tolerated.

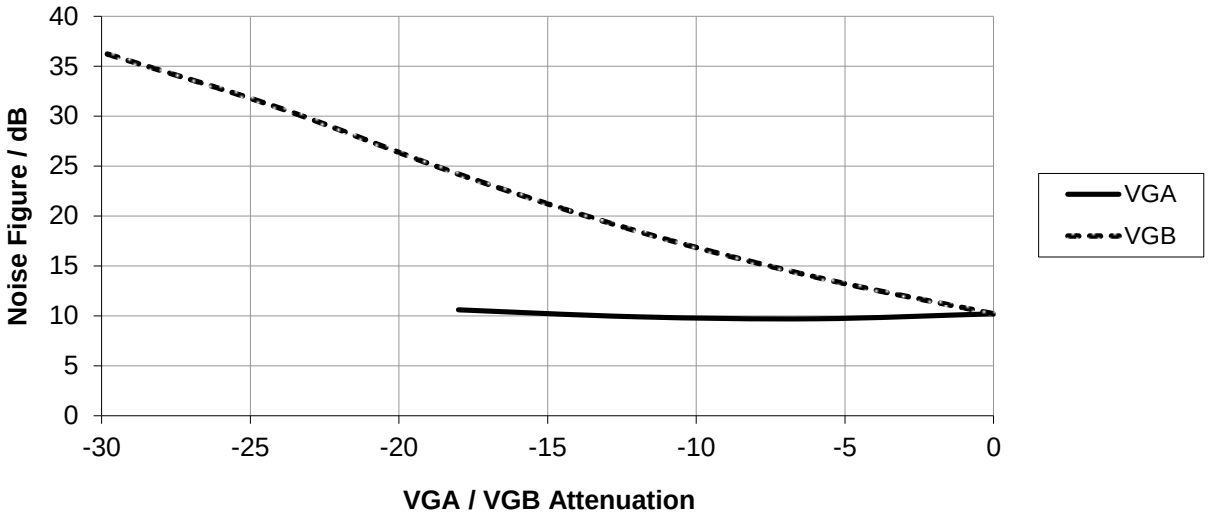


Figure 12 Variation in CMX970 Demodulator Noise Figure with VGA/VGB Control

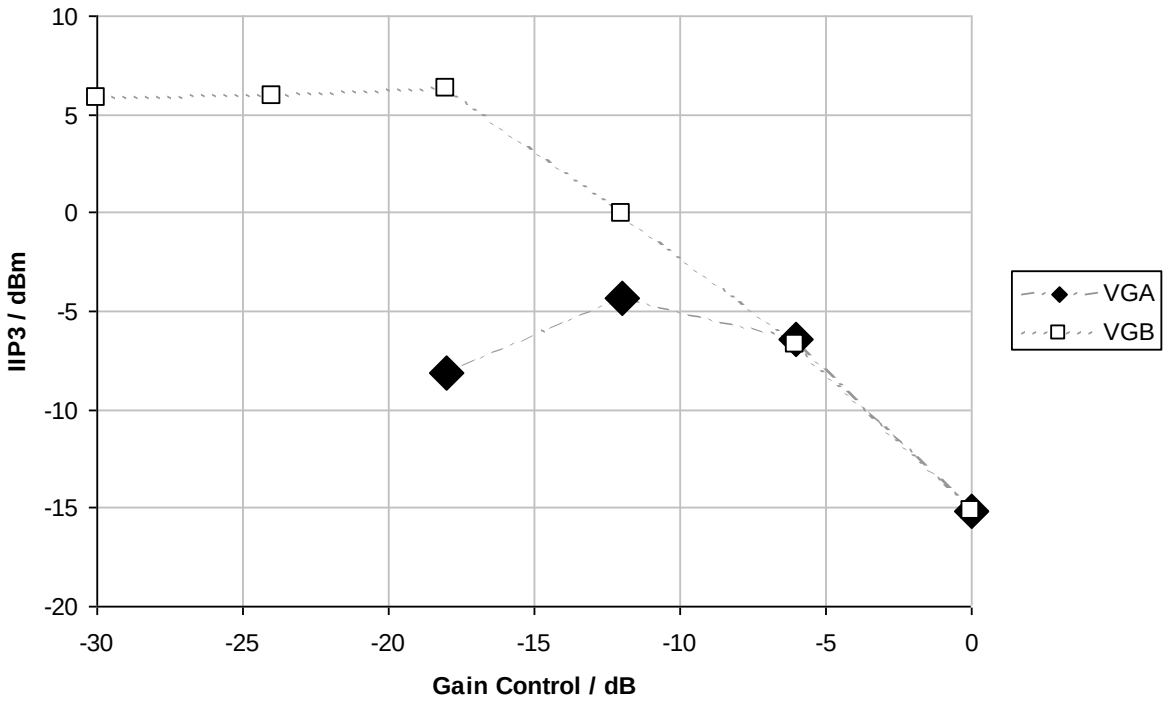


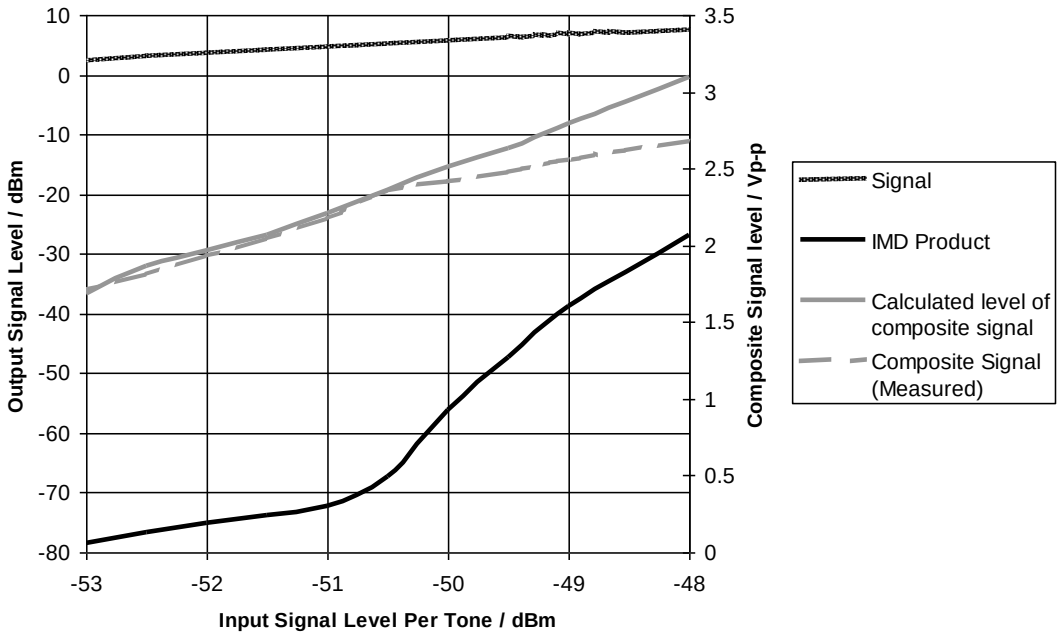
Figure 13 Variation in Input Third Order Intercept Point with VGA/VGB Control

8.5 Measurement of CMX970 Demodulator Intermodulation Performance

The measurement of the intermodulation (IMD) performance of the CMX970 demodulator requires great care because generally the IMD products are at a very low level. As a result it is important to ensure products being measured are generated by the CMX970, not the measurement instrument or the test system.

It is also important to ensure that measurements are taken before the onset of clipping in the I/Q output stages - the effect is shown in Figure 14. Considering the graph, at signal levels below –51dBm per tone (two tone signal, tones of equal amplitude) the measured IMD product rises at the classical rate of 2dB for every 1dB increase in tone level. For input levels above –51dBm the rate of increase rises dramatically due to the onset of clipping. The effect can be seen in the plots of the composite signal: the calculated line is based on a calculation of the peak-to-peak swing of the output I/Q voltage from measured tone level at the output of the CMX970, however the actual output level is also plotted and the two lines deviate at the on-set of clipping.

It will be apparent that any calculation of IMD parameters, e.g. input third order intercept point, from measurements taken after the onset of clipping will give erroneous results if trying to characterise receiver operation at normal signal levels.



(Note: the two curves ‘Signal’ and ‘IMD Product’ are levels in dBm so should be referenced to the left hand Y-axis; the other curves are output voltages and use the right hand Y-axis.)

Figure 14 Variations in Signal and IMD Product Levels

Typical IMD measurements for the CMX970 demodulator usually involve IMD products at least 75dB below the wanted signal.

The input level where compression commences will vary somewhat from device to device, the value of -44.5dBm[1] (Figure 14) is typical, but should only be used as an initial guide.

[1] Note: -50.5 dBm per tone = -44.5 dBm PEP,

8.6 Operation with large input signals

The input 1dB gain compression point of the CMX970 will vary depending on the settings of the VGA and VGB gain stages. Typical results with a 45 MHz signal, 50 ohm source, 'straight in' are as follows:

VGA = 0dB, VGB = 0dB	Input 1dB compression point = -42dBm
VGA = -18dB, VGB = 0dB	Input 1dB compression point = -25dBm
VGA = -18dB, VGB = -12dB	Input 1dB compression point = -12dBm
VGA = -18dB, VGB = -24dB	Input 1dB compression point = -8dBm

The above results are with the OUTDRV bit set to '1' and the IMD5-IMD0 bits in register $2F='000000'. For optimum intermodulation performance the IMDn bits should be set to '111111' which has the effect of reducing the gain by about 1dB thus improving the input compression point by 1dB.

Typical performance at maximum and minimum gain settings, plus some interim attenuator settings, is shown in Figure 15, measured at 45MHz, setting as above. The output is measured by buffering the differential I/Q output signals (voltage), converting to single-ended and then measuring as power based on 50 Ohms.

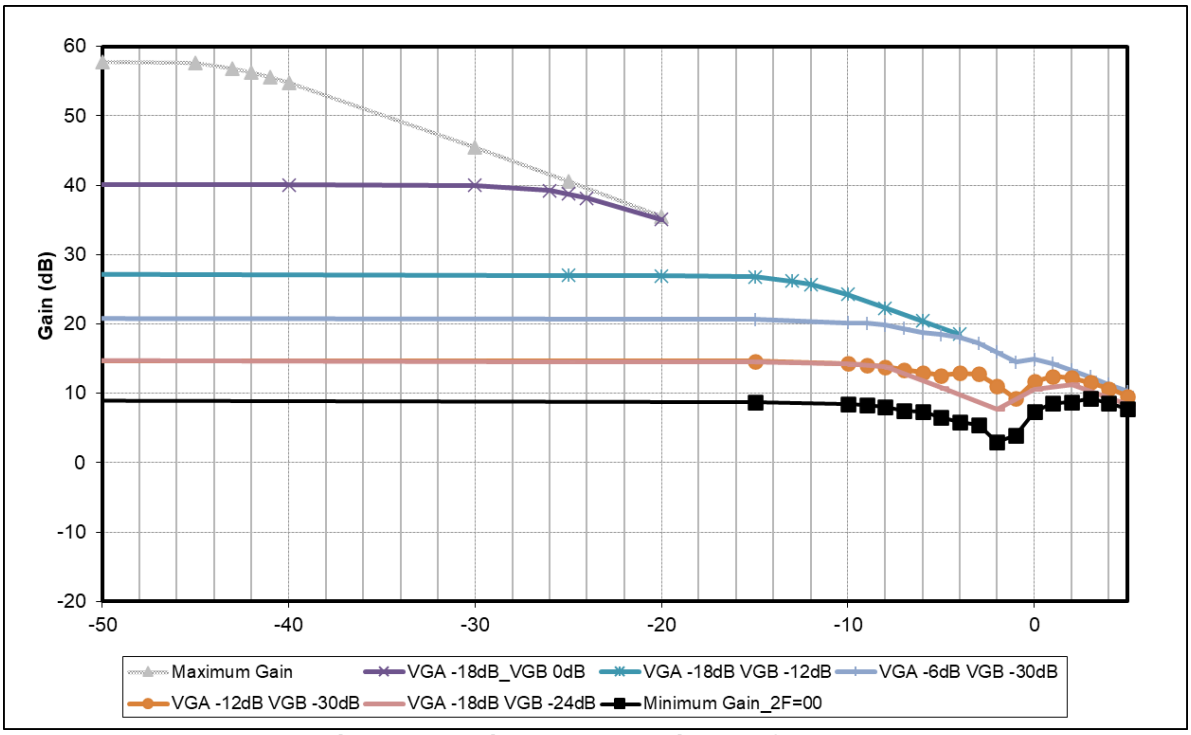


Figure 15 Gain v Input Level at IF of 45MHz

9 Performance Specification

9.1 Electrical Performance

For a definition of voltage and reference signals see Section 3.

9.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS}), (V_{CC} - V_{RFGND}) or (V_{CC} – V_{LOGND})	-0.3	+4.0	V
Voltage on any pin to V_{RFGND}, V_{SS} or V_{LOGND}	-0.3	V_{DD} + 0.3	V
Voltage between V_{SS}, V_{RFGND} and V_{LOGND}	-50	+50	mV
Current into or out of VSS, RFGND, LOGND, VCC or VDD pins	-75	+75	mA
Current into or out of any other pin	-30	+30	mA

Q7 Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	2060	mW
... Derating (see Note below)	–	20.6	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Note: Junction-to-ambient thermal resistance is dependent on board layout and mounting arrangements. The derating factor stated will be better than this with good connection between the device and a ground plane or heat sink.

9.1.2 Operating Limits

	Notes	Min.	Max.	Units
Digital Supply (V_{DD} – V_{SS})		3.0	3.6	V
Analogue Supply (V_{CC} – V_{RFGND})		3.0	3.6	V
Operating Temperature (see Note above)		-40	+85	°C

9.1.3 Operating Characteristics

9.1.3.1 DC Parameters

For the following conditions unless otherwise specified:
V_{DD} = V_{CC} = 3.3V; V_{SS} = V_{RFGND} = V_{LOGND} = 0V. LO Level = -10dBm and T_{AMB} = +25ºC.

DC Parameters	Notes	Min.	Typ.	Max.	Units
Total Current Consumption	1				
Powersave mode	2	–	7	70	µA
Bias only		–	1.7	2.0	mA
Operating	4	–	15	20	mA
Logic '1' Input Level		70%	–	–	V_{DD}
Logic '0' Input Level		–	–	30%	V_{DD}
Logic Input Leakage Current (Vin = 0 to V_{DD})		-1.0	–	+1.0	µA
Output Logic ‘1’ Level (I_{OH} = 0.6 mA)		80%	–	–	V_{DD}
Output Logic ‘0’ Level (I_{OL} = -1.0 mA)		–	–	+0.4	V
Power-up Time					
Voltage Reference	3	–	–	0.5	ms
All blocks except Voltage Reference	3	–	–	10	µs

Notes:

1. Total current, V_{DD} and V_{CC}.
2. Powersave mode includes the case after general reset with all analogue and digital supplies applied and also the case with V_{DD} applied but with all analogue supplies disconnected (i.e. in this latter scenario power from V_{DD} will not exceed the specified value, whatever the state of the registers). At T_{AMB} = 25ºC, not including any current drawn from device pins by external circuitry.
3. Time from the rising edge of the last serial clock input following CSN being asserted for a write to the appropriate control register.
4. Rx and Bias sections active, RXDIV = 0, OUTDRV = 0, COR = 0.

9.1.3.2 AC Parameters

For the following conditions unless otherwise specified:
V_{DD} = V_{CC} = 3.3V; V_{SS} = V_{RFGND} = V_{LOGND} = 0V. LO Level = -10dBm and T_{AMB}= +25ºC.

AC Parameters	Notes	Min.	Typ.	Max.	Units
Local Oscillator Input					
Frequency Range	10	40	–	1000	MHz
LO Input Level		–	-10	–	dBm

Notes:

10. Local oscillator input frequency twice or four times the required operating frequency.

9.1.3.3 AC Parameters – Demodulator

For the following conditions unless otherwise specified:
V_{DD} = V_{CC} = 3.3V; V_{SS} = V_{RFGND} = V_{LOGND} = 0V. LO Level = -10dBm and T_{AMB}= +25ºC.

IF/RF Amplifier and Quadrature Demodulator	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Gain	20,21	–	56	–	dB(V/V)
Noise Figure	20,21	–	10	–	dB
Input Third Order Intercept Point	20, 24	–	-15	–	dBm
Input Frequency Range		20	–	300	MHz
Input Impedance	21	–	1000	–	Ω
Output Impedance		–	200	–	Ω
Output Load					
Resistance (differential)	23	10	–	–	kΩ
Capacitance per Pin	23	–	–	10	pF
Differential Output Voltage	23	2	–	–	Vp-p
Output Common Mode Voltage		V_{CC}-1.9	V_{CC} – 1.7	V_{CC} – 1.5	V
LO Leakage at Input		–	-80	-40	dBm
Input 1dB Compression Point	20, 24,25	–	-41	–	dBm
VGA Control Range	22	–	18	–	dB
VGA Step Size		4	6	8	dB
VGB Control Range	22	–	30	–	dB
VGB Step Size		4	6	8	dB
I/Q Gain Matching Error		–	0.1	0.5	dB
I/Q Phase Matching Error		–	0.1	1	degree
I/Q Output Bandwidth (-3dB)	23	5	10	–	MHz

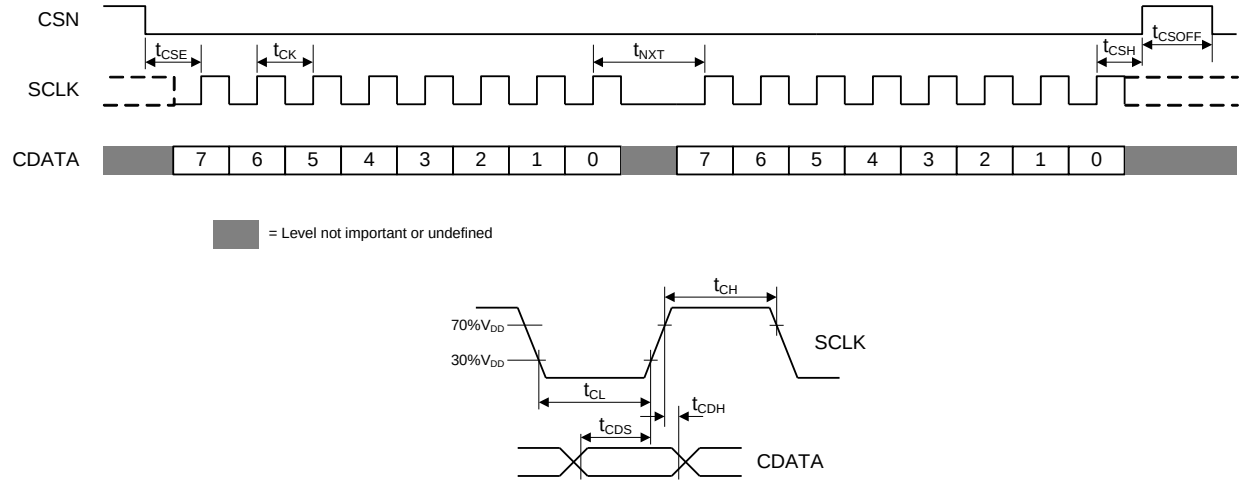
Notes:

20. Measured from an un-matched 50Ω input source to a differential I or Q output voltage; test frequency = 45MHz. Note that values include combined response of IF/RF amplifier, quadrature demodulator and I/Q amplifier stages; at maximum VGA and VGB setting (0dB);
21. See also section 8.1.
22. 4 x VGA steps and 6 x VGB steps, see Control register $1C, section 6.3.1.
23. Differential Output Voltage is achieved with default output drive setting (register $1C, b7='0', see section 6.3.1), for given output load and for at least the minimum I/Q output bandwidth; typical I/Q output bandwidth is achieved with increased drive capability selected (register $1C, b7='1', see section 6.3.1) and with the same output load specification.
24. With increased output drive setting (register $1C, b7='1').
25. With IMD5 – IMD0 (b7 – b2 of register $2F) set to '111111'

9.1.3.4 C-BUS

C-BUS Timings (See Figure 16)		Notes	Min.	Typ.	Max.	Units
t_{CSE}	CSN-Enable to Clock-High Time		100	-	-	ns
t_{CSH}	Last Clock-High to CSN-High Time		100	-	-	ns
t_{CSOFF}	CSN-High Time between transactions		1.0	-	-	µs
t_{NXT}	Inter-Byte Time		200	-	-	ns
t_{CK}	Clock-Cycle Time		200	-	-	ns
t_{CH}	Serial Clock (SCLK) - High Time		100	-	-	ns
t_{CL}	Serial Clock (SCLK) - Low Time		100	-	-	ns
t_{CDS}	Command Data (CDATA) - Set-Up Time		75.0	-	-	ns
t_{CDH}	Command Data (CDATA) - Hold Time		25.0	-	-	ns

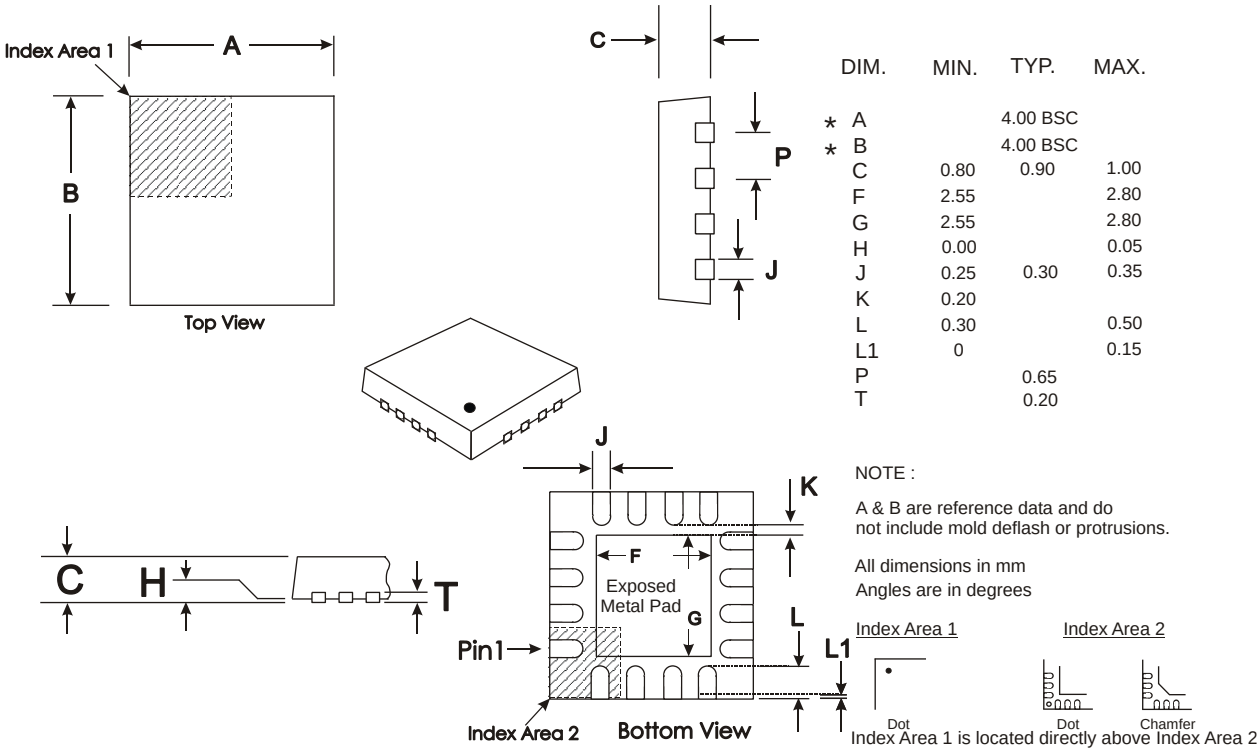
Maximum 30pF load on each C-BUS interface line.



Note: *Only 1 byte of data is used in* CMX970 *C-BUS transactions.*

Figure 16 C-BUS Timing

9.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A		4.00 BSC	
* B		4.00 BSC	
C	0.80	0.90	1.00
F	2.55		2.80
G	2.55		2.80
H	0.00		0.05
J	0.25	0.30	0.35
K	0.20		
L	0.30		0.50
L1	0		0.15
P		0.65	
T		0.20	

NOTE :

A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 17 Q7 Mechanical Outline: *Order as part no.* CMX970*Q7*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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