

1. General description

Planar passivated SCR with sensitive gate in a SOT223 (SC-73) surface mountable plastic package. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- Adapters
- Battery powered applications
- Industrial automation

4. Quick reference data

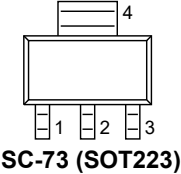
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage		-	-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq 112\text{ °C}$; Fig. 1	-	-	0.6	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 112\text{ °C}$; Fig. 2 ; Fig. 3	-	-	1	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	10	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	-	11	A
T_j	junction temperature	[1]	-	-	125	°C
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 9	-	50	200	μA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 100\text{ Ω}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 14	-	50	-	V/μs

[1] Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 SC-73 (SOT223)	 sym037
2	A	anode		
3	G	gate		
4	mb	mb; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT148W-600R	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

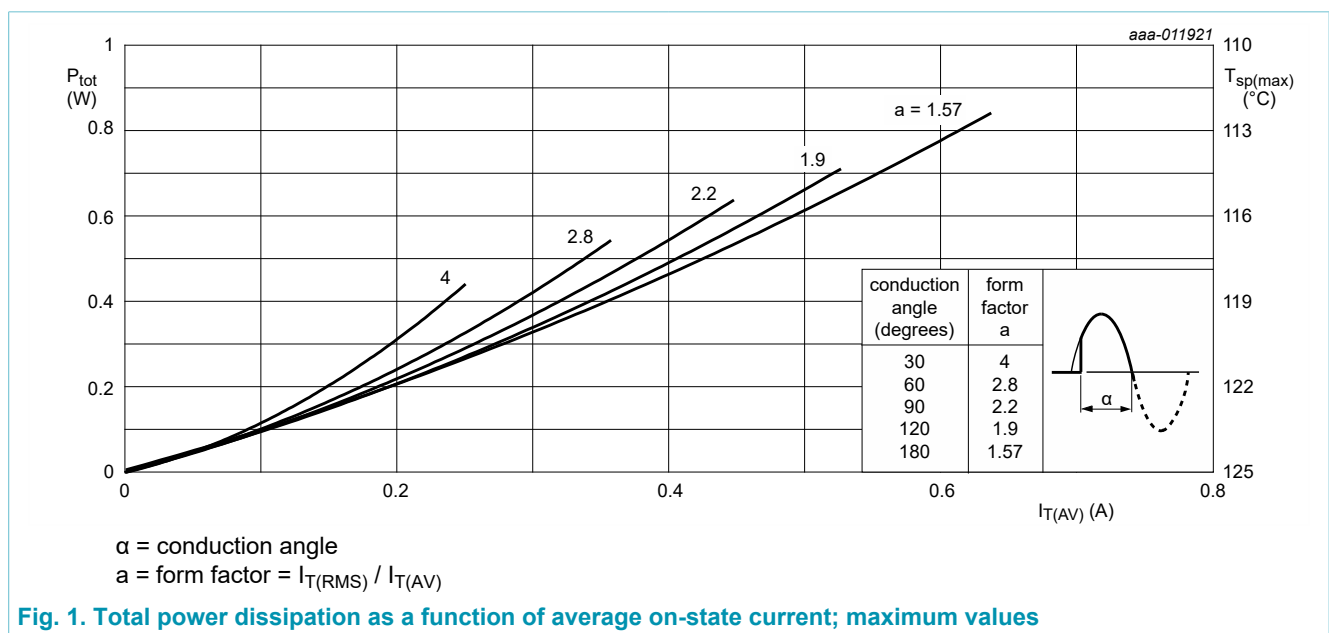
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	600	V
V_{RRM}	repetitive peak reverse voltage			-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq 112^\circ\text{C}$; Fig. 1		-	0.6	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 112^\circ\text{C}$; Fig. 2; Fig. 3		-	1	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 10\text{ ms}$; Fig. 4; Fig. 5		-	10	A
		half sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 8.3\text{ ms}$		-	11	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN		-	0.5	A^2s
dl_T/dt	rate of rise of on-state current	$I_G = 400\text{ }\mu\text{A}$		-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current			-	1	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	1.2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.12	W
T_{stg}	storage temperature			-40	150	$^\circ\text{C}$
T_j	junction temperature		[2]	-	125	$^\circ\text{C}$

- [1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state.
 [2] Operation above 110°C may require the use of a gate to cathode resistor of $1\text{ k}\Omega$ or less.



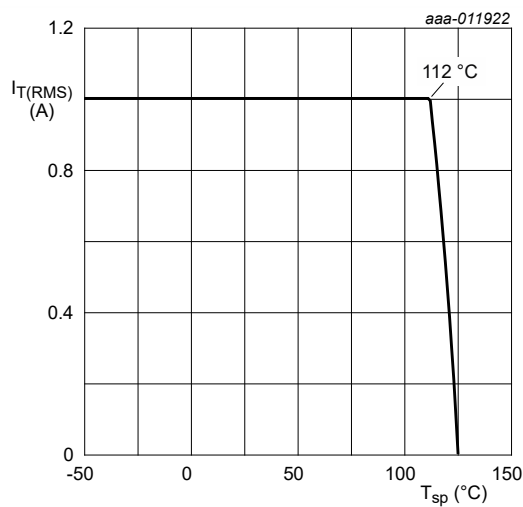


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values

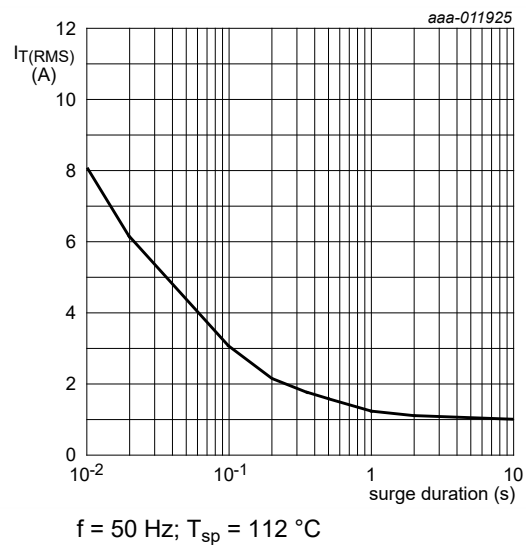


Fig. 3. RMS on-state current as a function of surge duration; maximum values

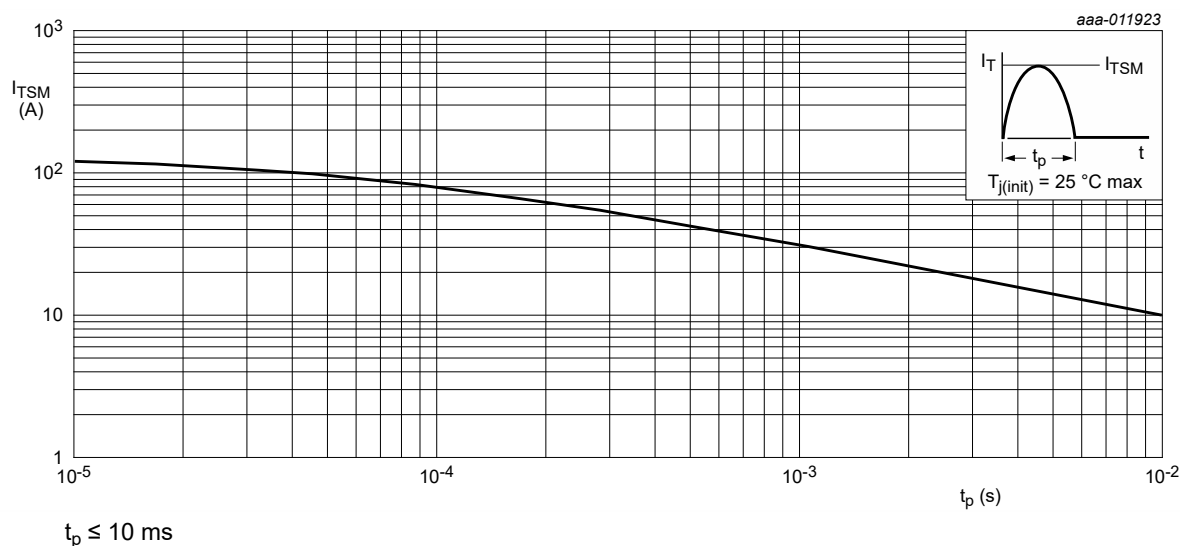
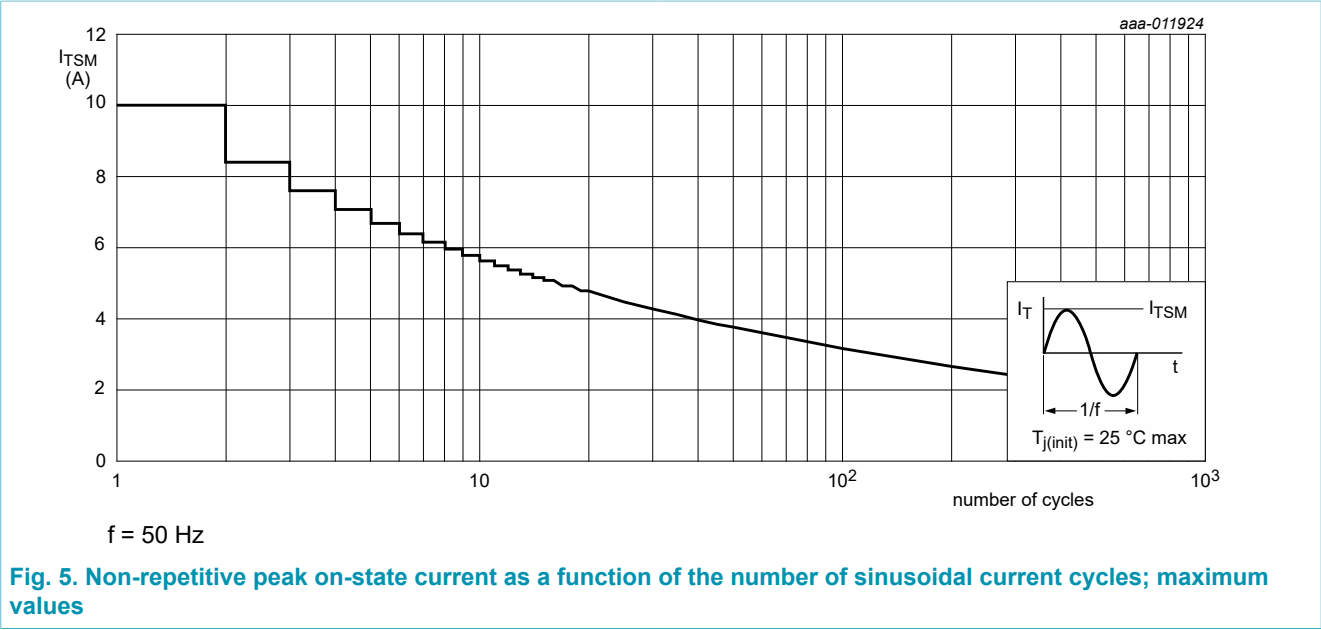


Fig. 4. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 6		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted; pad area; Fig. 7		-	70	-	K/W
		printed circuit board mounted; minimum footprint; Fig. 8		-	156	-	K/W

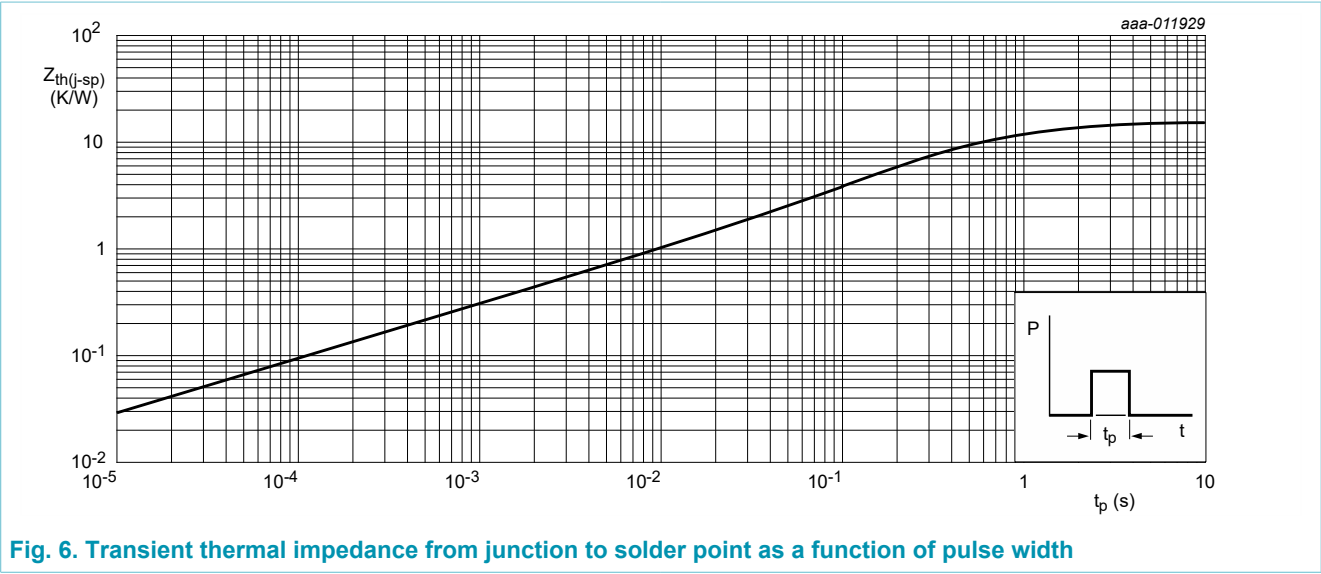
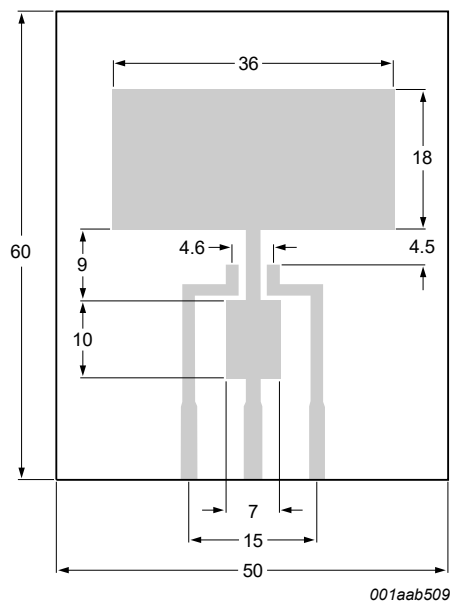
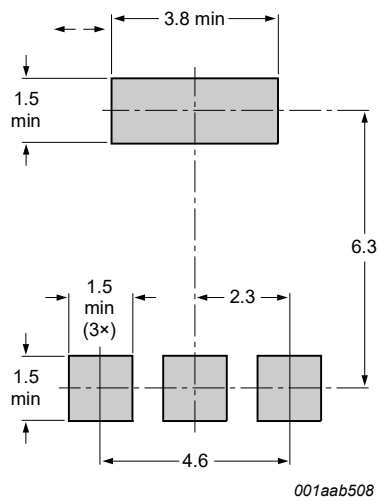


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width



All dimensions are in mm
Printed circuit board:
FR4 epoxy glass (1.6 mm thick), copper laminate
(35 um thick)

Fig. 7. Printed circuit board pad area: SOT223



All dimensions are in mm

Fig. 8. Minimum footprint SOT223

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	50	200	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	0.17	10	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	0.1	6	mA
V_T	on-state voltage	$I_T = 2\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12	-	1.3	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 13	-	0.4	1	V
		$V_D = 600\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 13	0.1	0.2	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
I_R	reverse current	$V_R = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 100\text{ }\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 14	-	50	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 4\text{ A}$; $V_D = 600\text{ V}$; $I_G = 5\text{ mA}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; $T_j = 25\text{ }^\circ\text{C}$	-	2	-	μs
t_q	commutated turn-off time	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{TM} = 4\text{ A}$; $V_R = 35\text{ V}$; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 2\text{ V}/\mu\text{s}$; $R_{GK(EXT)} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM})	-	100	-	μs

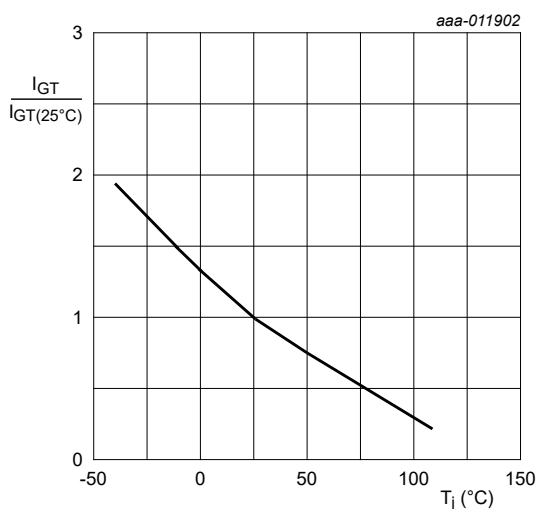


Fig. 9. Normalized gate trigger current as a function of junction temperature

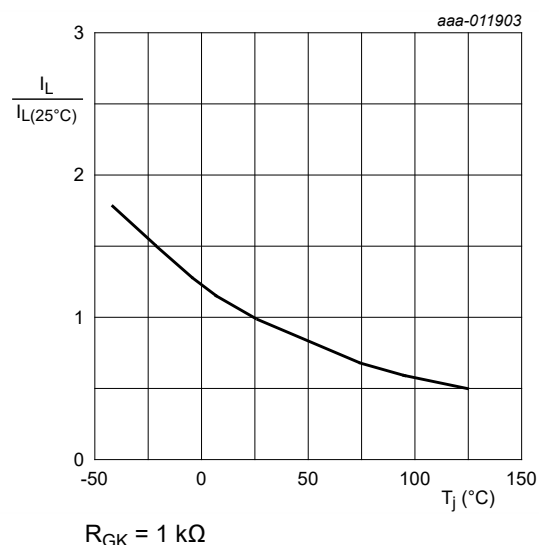


Fig. 10. Normalized latching current as a function of junction temperature

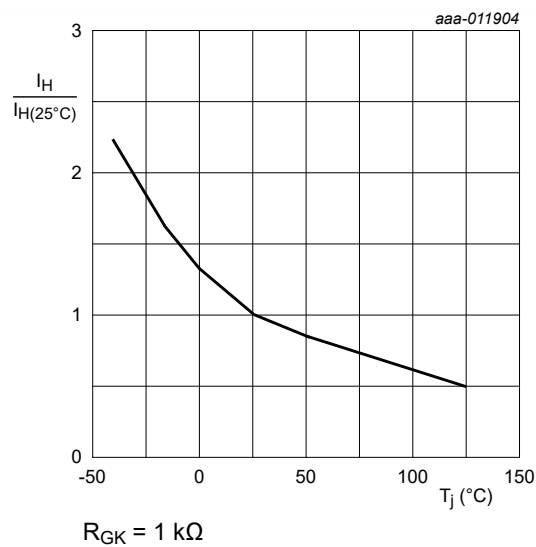


Fig. 11. Normalized holding current as a function of junction temperature

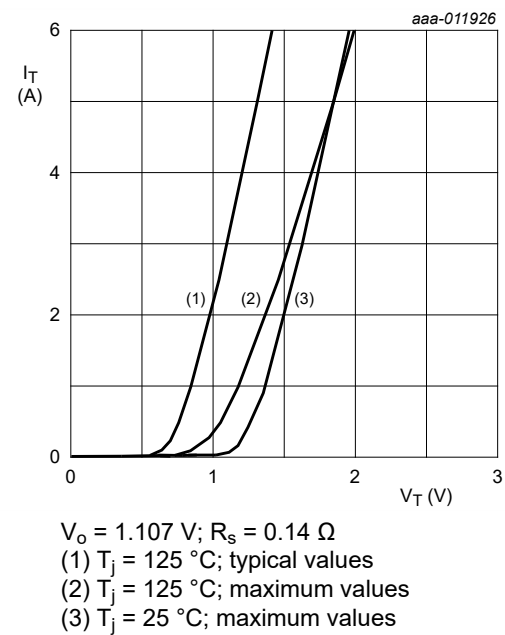


Fig. 12. On-state current as a function of on-state voltage

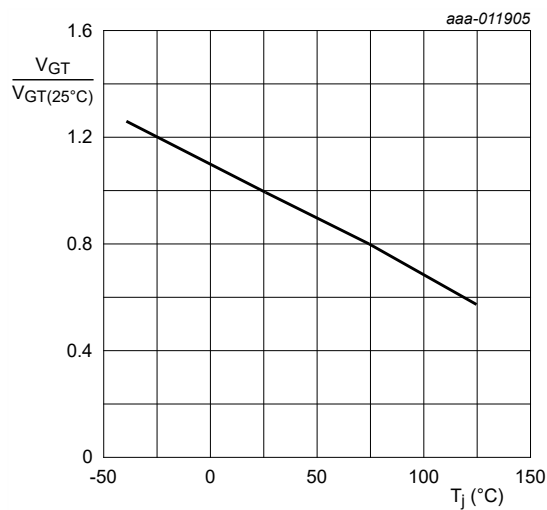


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

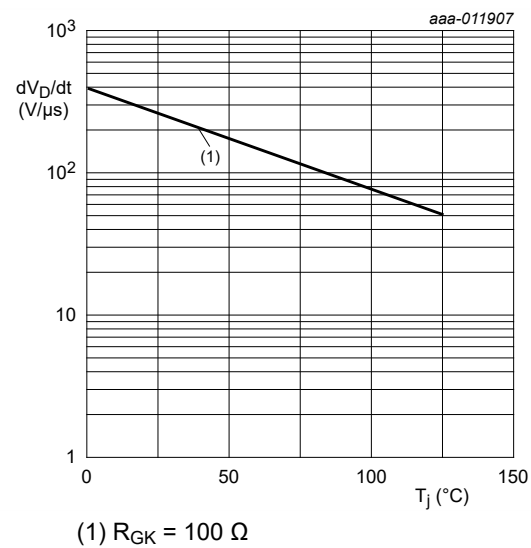


Fig. 14. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

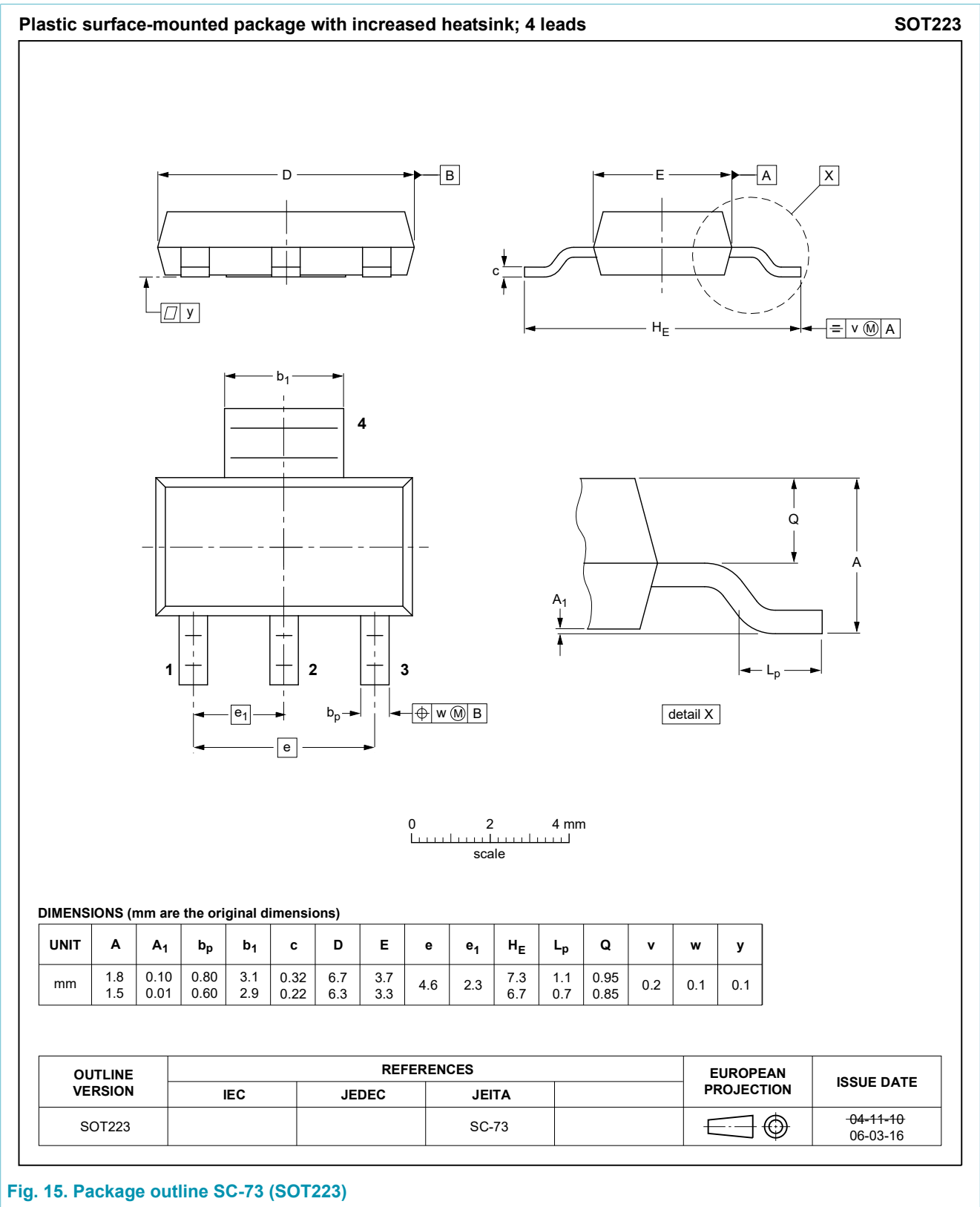


Fig. 15. Package outline SC-73 (SOT223)

11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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