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LSM6DSV16BX

Datasheet

iNEMO 3-axis accelerometer and 3-axis gyroscope: inertial module for UI and bone conduction with embedded machine learning core and Qvar specification



LGA 14L
(2.5 x 3.0 x 0.71 mm) typ.



Product status link
LSM6DSV16BX

Product summary		
Order code	LSM6DSV16BX	LSM6DSV16BXTR
Temperature range [°C]	-40 to +85	
Package	LGA-14L (2.5 x 3.0 x 0.71 mm)	
Packing	Tray	Tape and reel

Product resources
TN0018 (Design and soldering)

Product label
SUSTAINABLE TECHNOLOGY

Features

- Triple core for UI, bone conduction, and Qvar sensing
- Power consumption: 0.95 mA in combo high-performance mode
- “Always-on" experience with low power consumption for both accelerometer and gyroscope
- Smart FIFO up to 4.5 KB
- ±2/±4/±8/±16 *g* full scale
- ±125/±250/±500/±1000/±2000/±4000 dps full scale
- Analog supply voltage: 1.71 V to 3.6 V
- Independent IO supply (extended range: 1.08 V to 3.6 V)
- Compact footprint: 2.5 mm x 3 mm x 0.71 mm
- SPI / I²C & MIPI I3C® v1.1 serial interface with main processor data synchronization
- TDM slave interface
- Advanced pedometer, step detector, and step counter
- Significant motion detection, tilt detection
- Standard interrupts: free-fall, wakeup, 6D orientation, click and double-click
- Programmable finite state machine for accelerometer, gyroscope, and Qvar sensor data processing with high rate @ 960 Hz
- Machine learning core with exportable features and filters for AI applications
- Embedded Qvar: electric charge variation detection
- Embedded analog hub for ADC and processing analog input data
- Embedded sensor fusion low-power algorithm
- Embedded temperature sensor
- ECOPACK and RoHS compliant

Applications

- Motion tracking and gesture detection
- Wearables
- TWS (true wireless stereo)
- IoT and connected devices
- Handheld devices
- Vibration detection for bone conduction

Description

The LSM6DSV16BX is a system-in-package featuring a 3-axis digital accelerometer and a 3-axis digital gyroscope with a triple core for processing acceleration, angular rate, and Qvar sensing data on three separate channels with dedicated configuration, processing, and filtering.

The LSM6DSV16BX integrates a UI sensor, audio accelerometer, and Qvar sensor in a compact package (2.5 x 3.0 x 0.71 mm).

The UI in high-performance mode runs at 0.6 mA and enables always-on low-power features for an optimal motion experience for wearable and TWS applications.

The LSM6DSV16BX embeds advanced dedicated features and data processing for audio and motion processing like the finite state machine and machine learning core with exportable AI features/filters for IoT applications.

The LSM6DSV16BX embeds Qvar (electric charge variation detection) sensing which allows detecting and improving presence and motion activity with external electrodes. The device also embeds an analog hub, which is able to connect an external analog input and convert it to a digital signal for processing.

1 Overview

The LSM6DSV16BX is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

The LSM6DSV16BX delivers best-in-class motion sensing that can detect orientation and gestures in order to empower application developers and consumers with features and capabilities that are more sophisticated than simply orienting their devices to portrait and landscape mode.

The event-detection interrupts enable efficient and reliable motion tracking and contextual awareness, implementing hardware recognition of free-fall events, 6D orientation, click and double-click sensing, activity or inactivity, stationary/motion detection and wakeup events. Machine Learning and Finite State Machine processing allows moving some algorithms from the application processor to the LSM6DSV16BX sensor, enabling consistent reduction of power consumption.

The LSM6DSV16BX supports main OS requirements, offering real, virtual and batch mode sensors. In addition, the LSM6DSV16BX can efficiently run the sensor-related features specified in Android, saving power and enabling faster reaction time. In particular, the LSM6DSV16BX has been designed to implement hardware features such as significant motion detection, stationary/motion detection, tilt, pedometer functions and timestamping.

Core 1 has been designed for user interface data processing for motion tracking. Data are available on the primary output of I²C / SPI / MIPI I3C® for the accelerometer and gyroscope with independent ODR and FS.

Core 2 has been designed for audio acceleration data processing for bone conduction and speech-enhanced applications. Data are available on the TDM interface at 8 kHz or 16 kHz.

The LSM6DSV16BX embeds a dedicated Core 3 for Qvar functionality which is an electrical potential sensor able to measure the variation of the quasi electrostatic potential. The Qvar sensing channel can be used for applications such as human motion detection.

Up to 4.5 KB of FIFO with compression and dynamic allocation of significant data (that is, Qvar, timestamp, and so forth) allows overall power saving of the system.

Like the entire portfolio of MEMS sensor modules, the LSM6DSV16BX leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DSV16BX embeds an analog hub which is able to connect an external analog input and convert it to a digital signal for processing as well as advanced dedicated features like a finite state machine and data filtering for motion processing.

The LSM6DSV16BX embeds Qvar functionality which is an electrostatic sensor able to measure the variation of the quasi electrostatic potential. The Qvar sensing channel can be used for user interface applications like tap, double-tap, triple-tap, long press, L/R – R/L swipe.

Human body motion is detected by the variation of the electric potential induced on electrodes by the continuous redistribution of electrostatic charges during motion activities.

The LSM6DSV16BX is available in a small plastic land grid array (LGA) package of 2.5 x 3.0 x 0.71 mm to address ultra-compact solutions.

2 Embedded low-power features

The LSM6DSV16BX has been designed to be fully compliant with Android, featuring the following on-chip functions:

- 4.5 KB FIFO data buffering, data can be compressed two or three times
  - 100% efficiency with flexible configurations and partitioning
  - Possibility to store timestamp
- Event-detection interrupts (fully configurable)
  - Free-fall
  - Wakeup
  - 6D orientation
  - Click and double-click sensing
  - Activity/inactivity recognition
  - Stationary/motion detection
- Specific IP blocks (called "embedded functions") with negligible power consumption and high-performance
  - Pedometer functions: step detector and step counters
  - Tilt
  - Significant motion detection
  - Finite state machine (FSM)
  - Machine learning core (MLC) with exportable features and filters for AI applications
  - Embedded sensor fusion low-power (SFLP) algorithm
- Analog hub for processing external analog input data
- Qvar: electric charge variation detection

2.1 Pedometer functions: step detector and step counters

The LSM6DSV16BX embeds an advanced pedometer with an algorithm running in an ultra-low-power domain in order to ensure extensive battery life in battery-constrained applications.

Leveraging on enhanced configurability, the advanced embedded pedometer is suitable for a large range of applications from mobile to wearable devices.

The algorithm processes and analyzes the accelerometer waveform in order to count the user's steps during walking and running activities.

The pedometer works at 30 Hz and it is not affected by the selected device power mode (ultra-low-power, low-power, high-performance), thus guaranteeing an ultra-low-power experience and extreme flexibility in conjunction with other device functionalities.

The accelerometer operating mode can be changed at runtime and is based on user requirements without impacting the performance of the pedometer.

The pedometer output can be batched in the device's FIFO buffer, in order to decrease overall system current consumption.

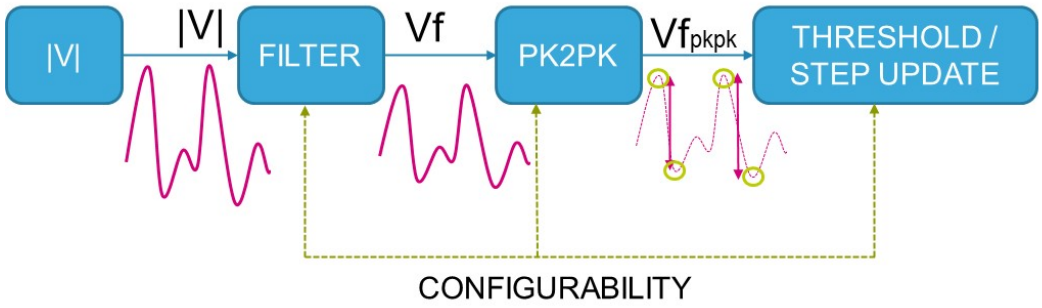
ST freely provides the support and the tools for easily configuring the device and tuning the algorithm configuration for a best-in-class user experience.

2.2 Pedometer algorithm

The pedometer algorithm is composed of a cascade of four stages:

1. Computation of the acceleration magnitude signal in order to detect the signal independently from device orientation
2. FIR filter to extract relevant frequency components and to smooth the signal by cutting off high frequencies
3. Peak detector to find the maximum and minimum of the waveform and compute the peak-to-peak value
4. Step count: if the peak-to-peak value is greater than the settled threshold, a step is counted

Figure 1. Four-stage pedometer algorithm



The LSM6DSV16BX embeds a dynamic internal threshold for step detection that is updated after each peak-to-peak evaluation: the internal threshold is increased with a configurable speed if a step is detected or decreased with a configurable speed if a step is not detected.

This approach ensures high accuracy when the user starts to walk and a false peak rejection when the user is walking or running.

An internal configurable debounce algorithm can be also set to filter false walks: indeed, an accelerometer pattern is recognized as a walk or run only if a minimum number of steps are counted.

The LSM6DSV16BX has been designed to reject a false-positive signal inside the algorithm core.

On top of the mechanisms detailed above, the LSM6DSV16BX allows enabling and configuring a dedicated false-positive rejection block to further boost pedometer accuracy.

2.3 Tilt detection

The tilt function helps to detect activity change and has been implemented in hardware using only the accelerometer to achieve targets of both ultra-low power consumption and robustness during the short duration of dynamic accelerations.

The tilt function is based on a trigger of an event each time the device's tilt changes and can be used with different scenarios, for example:

- Triggers when phone is in a front pants pocket and the user goes from sitting to standing or standing to sitting
- Doesn’t trigger when phone is in a front pants pocket and the user is walking, running or going upstairs

2.4 Significant motion detection

The significant motion detection (SMD) function generates an interrupt when a ‘significant motion’, that could be due to a change in user location, is detected. In the LSM6DSV16BX device this function has been implemented in hardware using only the accelerometer.

SMD functionality can be used in location-based applications in order to receive a notification indicating when the user is changing location.

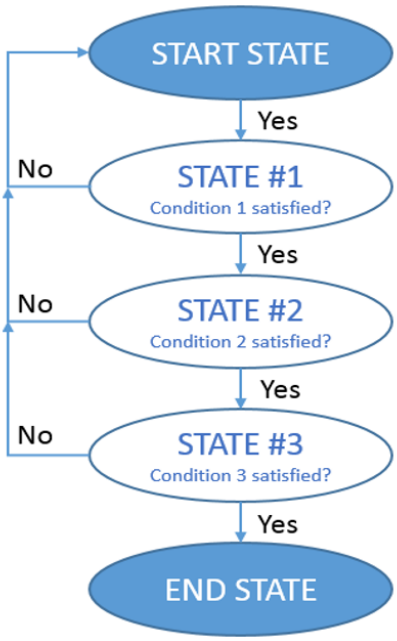
2.5 Finite state machine

The LSM6DSV16BX can be configured to generate interrupt signals activated by user-defined motion patterns. To do this, up to 8 embedded finite state machines can be programmed independently for motion detection such as glance gestures, absolute wrist tilt, shake and double-shake detection.

Definition of finite state machine

A state machine is a mathematical abstraction used to design logic connections. It is a behavioral model composed of a finite number of states and transitions between states, similar to a flow chart in which one can inspect the way logic runs when certain conditions are met. The state machine begins with a start state, goes to different states through transitions dependent on the inputs, and can finally end in a specific state (called stop state). The current state is determined by the past states of the system. The following figure shows a generic state machine.

Figure 2. Generic state machine



Finite state machine in the LSM6DSV16BX

The LSM6DSV16BX works as a combo accelerometer-gyroscope sensor, generating acceleration and angular rate output data. These data, along with analog hub / Qvar sensor data, can be used as input of up to 8 programs in the embedded finite state machine (Figure 3. State machine in the LSM6DSV16BX).

All 8 finite state machines are independent: each one has its dedicated memory area and it is independently executed. An interrupt is generated when the end state is reached or when some specific command is performed.

Figure 3. State machine in the LSM6DSV16BX



2.6 Machine learning core

The LSM6DSV16BX embeds a dedicated core for machine learning processing that provides system flexibility, allowing some algorithms run in the application processor to be moved to the MEMS sensor with the advantage of consistent reduction in power consumption.

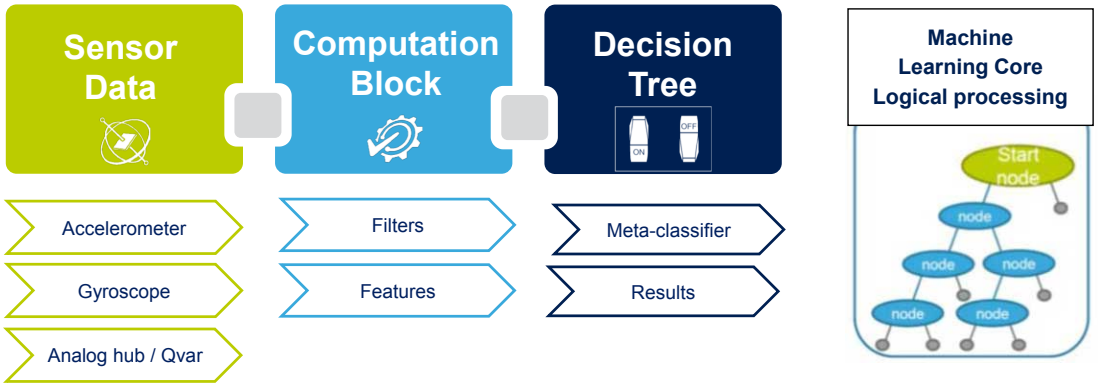
Machine learning core logic allows identifying if a data pattern (for example, motion) matches a user-defined set of classes. Typical examples of applications could be activity detection like running, walking, driving, and so forth.

The LSM6DSV16BX machine learning core works on data patterns coming from the accelerometer and gyroscope sensors, but it is also possible to connect and process analog hub / Qvar sensor data.

The input data can be filtered using a dedicated configurable computation block containing filters and features computed in a fixed time window defined by the user. Computed feature values and filtered data values can also be read through the FIFO buffer.

Machine learning processing is based on logical processing composed of a series of configurable nodes characterized by "if-then-else" conditions where the "feature" values are evaluated against defined thresholds.

Figure 4. Machine learning core in the LSM6DSV16BX



The LSM6DSV16BX can be configured to run up to 4 decision trees simultaneously and independently and every decision tree can generate up to 16 results. The total number of nodes can be up to 128.

The results of the machine learning processing are available in dedicated output registers readable from the application processor at any time.

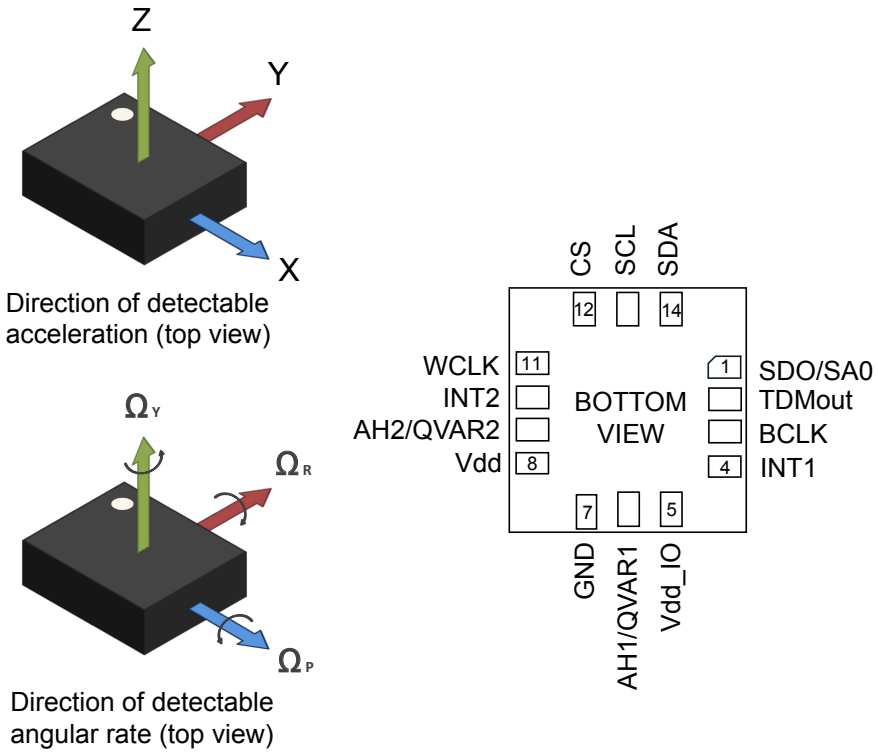
The LSM6DSV16BX machine learning core can be configured to generate an interrupt when a change in the result occurs.

2.7 Adaptive self-configuration (ASC)

The LSM6DSV16BX supports the adaptive self-configuration (ASC) feature, which allows the FSM to automatically reconfigure the device in real time based on the detection of a specific motion pattern or based on the output of a specific decision tree configured in the MLC, without any intervention from the host processor. The FSM can write a subset of the device registers using the SETR command, which allows indicating the register address and the new value to be written in such a register. The access to these device registers is mutually exclusive to the host.

3 Pin description

Figure 5. Pin connections

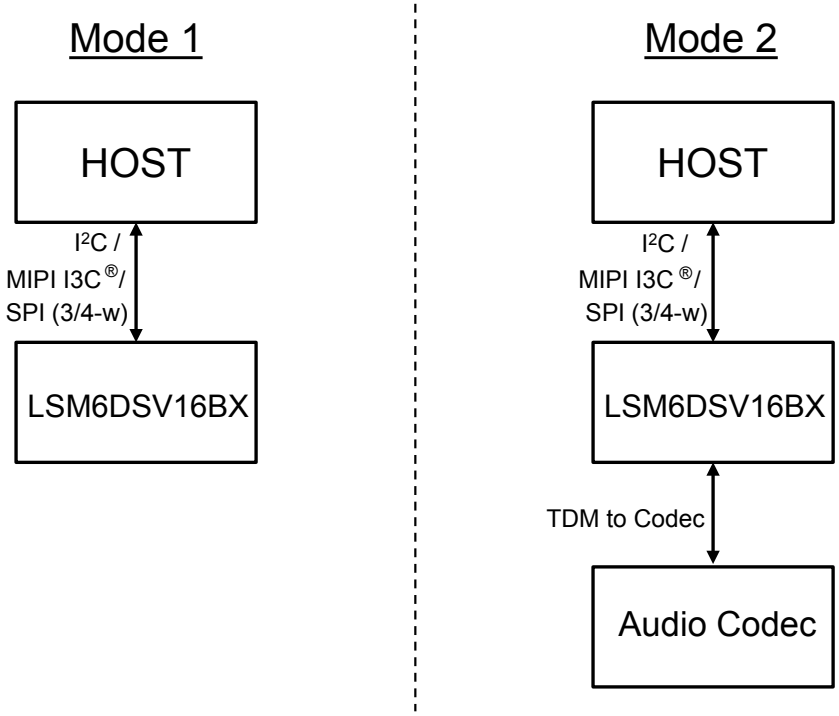


3.1 Pin connections

The LSM6DSV16BX offers flexibility to connect the pins in order to have two different mode connections and functionalities. In detail:

- **Mode 1**: I²C / MIPI I3C® slave interface or SPI (3- and 4-wire) serial interface is available.
- **Mode 2**: I²C / MIPI I3C® slave interface or SPI (3- and 4-wire) serial interface and TDM interface are available.

Figure 6. LSM6DSV16BX connection modes



In the following table each mode is described for the pin connections and function.

Table 1. Pin description

Pin#	Name	Mode 1 function	Mode 2 function
1	SDO/SA0(1)	SPI 4-wire interface serial data output (SDO) I²C least significant bit of the device address (SA0)	SPI 4-wire interface serial data output (SDO) I²C least significant bit of the device address (SA0)
2	TDMout	Connect to GND or Vdd_IO	TDM out
3	BCLK	Connect to GND or Vdd_IO	TDM bit clock
4	INT1	Programmable interrupt in I²C and SPI	Programmable interrupt in I²C and SPI
5	Vdd_IO(2)	Power supply for I/O pins	
6	AH1/QVAR1	Connect to Vdd or GND if the analog hub and Qvar are disabled. AH input 1 (or Qvar electrode 1) is connected if the analog hub (or Qvar functionality) is enabled.	Connect to Vdd or GND if the analog hub and Qvar are disabled. AH input 1 (or Qvar electrode 1) is connected if the analog hub (or Qvar functionality) is enabled.
7	GND	0 V supply	
8	Vdd(2)	Power supply	
9	AH2/QVAR2	Connect to Vdd or GND if the analog hub and Qvar are disabled. AH input 2 (or Qvar electrode 2) is connected if the analog hub (or Qvar functionality) is enabled.	Connect to Vdd or GND if the analog hub and Qvar are disabled. AH input 2 (or Qvar electrode 2) is connected if the analog hub (or Qvar functionality) is enabled.
10	INT2	Programmable interrupt 2 in I²C and SPI	Programmable interrupt 2 in I²C and SPI
11	WCLK	Connect to Vdd_IO or leave unconnected	TDM word clock
12	CS(1)	I²C / MIPI I3C® / SPI mode selection (1: SPI idle mode / I²C / MIPI I3C® communication enabled; 0: SPI communication mode / I²C / MIPI I3C® disabled)	I²C / MIPI I3C® / SPI mode selection (1: SPI idle mode / I²C / MIPI I3C® communication enabled; 0: SPI communication mode / I²C / MIPI I3C® disabled)
13	SCL(1)	I²C / MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)	I²C / MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)
14	SDA(1)	I²C / MIPI I3C® serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	I²C / MIPI I3C® serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

1. *SPI 3/4-wire interface not available with the analog hub / Qvar functionality enabled.*
2. *Recommended 100 nF filter capacitor.*

4 Module specifications

4.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25 °C, unless otherwise noted.

Table 2. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
				±16		
G_FS	Angular rate measurement range			±125		dps
				±250		
				±500		
				±1000		
				±2000		
				±4000		
LA_So	Linear acceleration sensitivity(2)	FS = ±2 *g*		0.061		mg/LSB
		FS = ±4 *g*		0.122		
		FS = ±8 *g*		0.244		
		FS = ±16 *g*		0.488		
G_So	Angular rate sensitivity(2)	FS = ±125 dps		4.375		mdps/LSB
		FS = ±250 dps		8.75		
		FS = ±500 dps		17.50		
		FS = ±1000 dps		35		
		FS = ±2000 dps		70		
		FS = ±4000 dps		140		
G_So%	Sensitivity tolerance(3)	at component level		±1		%
LA_SoDr	Linear acceleration sensitivity change vs. temperature(4)	from -40° to +85°		±0.01		%/°C
G_SoDr	Angular rate sensitivity change vs. temperature(4)	from -40° to +85°		±0.01		%/°C
LA_TyOff	Linear acceleration zero-*g* level offset accuracy(3)			±20		mg
G_TyOff	Angular rate zero-rate level(3)			±2		dps
LA_OffDr	Linear acceleration zero-*g* level change vs. temperature(4)			±0.1		mg/°C
G_OffDr	Angular rate typical zero-rate level change vs. temperature(4)			±0.008		dps/°C
Rn	Rate noise density in high-performance mode(5)			3.5		mdps/√Hz
RnRMS	Gyroscope RMS noise in low-power mode(6)			70		mdps
An	Primary interface - acceleration noise density in high-performance mode(7)	FS independent		70		µg/√Hz
	TDM interface - acceleration noise density(8)	FS independent		30		
RMS	Accelerometer RMS noise in low-power mode(9)	LPM1		2.6		mg RMS
		LPM2		2.1		
		LPM3		1.4		

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_ODR	Linear acceleration output data rate			1.875(10) 7.5 15 30 60 120 240 480 960 1.92 k 3.84 k 7.68 k		Hz
G_ODR	Angular rate output data rate			7.5 15 30 60 120 240 480 960 1.92 k 3.84 k 7.68 k		
TDMBW	First -3 dB cut point for accelerometer TDM channel		1			kHz
Vst	Linear acceleration self-test output change(11)(12)		20		1700	mg
	Angular rate self-test output change(13)	FS = ±250 dps	20		80	dps
		FS = ±2000 dps	150		700	dps
Top	Operating temperature range		-40		+85	°C

1. *Typical specifications are not guaranteed.*
2. *Sensitivity values after factory calibration test and trimming.*
3. *Value after calibration.*
4. *Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples. Not measured during final test for production.*
5. *Gyroscope rate noise density in high-performance mode is independent of the ODR and FS setting. Gyroscope noise density is computed starting from measured noise RMS and considering BW = ODR/2.*
6. *Gyroscope RMS noise in low-power mode is independent of the ODR and FS setting.*
7. *Accelerometer noise density in high-performance mode is independent of the selected ODR and FS. Accelerometer noise density is computed starting from measured noise RMS and considering BW = ODR/2.*
8. *Noise density is between 10 Hz and 1 kHz.*
9. *Accelerometer RMS noise in low-power mode is independent of the ODR and FS setting.*
10. *This ODR is available when the accelerometer is in low-power mode.*
11. *The sign of the linear acceleration self-test output change is defined by the ST_XL_[1:0] bits in a dedicated register for all axes.*
12. *Accelerometer self-test limits are full-scale independent.*
13. *The sign of the angular rate self-test output change is defined by the ST_G_[1:0] bits in a dedicated register for all axes.*

4.2 Electrical characteristics

@ Vdd = 1.8 V, T = 25 °C, unless otherwise noted.

Table 3. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.71	1.8	3.6	V
Vdd_IO	Power supply for I/O		1.08		3.6	V
IddHP	Gyroscope and accelerometer current consumption in high-performance mode (UI only)			0.6		mA
IddHPT	Gyroscope and accelerometer current consumption in high-performance mode (UI + TDM)			0.95		mA
LA_IddHP	Accelerometer current consumption in high-performance mode (UI only)			190		µA
LA_IddHPT	Accelerometer current consumption in high-performance mode & TDM			0.6		mA
LA_IddLPM2	Accelerometer current consumption in low-power mode (LPM2)	ODR = 60 Hz		20		µA
LA_IddLPM1	Accelerometer current consumption in low-power mode (LPM1)	ODR = 60 Hz		17		µA
IddPD	Gyroscope and accelerometer current consumption during power-down			2.6		µA
Ton	Turn-on time - gyroscope			30		ms
V_{IH}	Digital high-level input voltage		0.7 * Vdd_IO			V
V_{IL}	Digital low-level input voltage				0.3 * Vdd_IO	V
V_{OH}	High-level output voltage	I_{OH} = 4 mA(2)	Vdd_IO - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA(2)			0.2	V
Top	Operating temperature range		-40		+85	°C

1. *Typical specifications are not guaranteed.*
2. *4 mA is the maximum driving capability, that is, the maximum DC current that can be sourced/sunk by the digital pin in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.*

Table 4. Electrical parameters of Qvar (@Vdd = 1.8 V, T = 25 °C)

Parameter	Typ.(1)	Unit
Power consumption	15(2)	µA
Offset (shorted inputs)	3	mV
Noise (shorted inputs)	54	µV
Qvar gain	78	LSB/mV
CMRR	54	dB
Input impedance	Configurable (from 235 M to 2.4 G)	Ω
Input range	±460	mV

1. *Vdd_IO = 1.8 V, Zin = 235 MOhm. Typical values are based on characterization and are not guaranteed.*
2. *Extra power consumption when only the analog hub / Qvar function is enabled. In this condition the accelerometer must be set to high-performance mode or normal mode.*

4.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ. (1)	Max.	Unit
TODR(2)	Temperature refresh rate			60		Hz
Toff	Temperature offset(3)		-15		+15	°C
TSen	Temperature sensitivity			256		LSB/°C
TST	Temperature stabilization time(4)				500	µs
T_ADC_res	Temperature ADC resolution			16		bit
Top	Operating temperature range		-40		+85	°C

1. *Typical specifications are not guaranteed*
2. *When the accelerometer is in low-power mode and the gyroscope part is turned off, the TODR value is equal to the accelerometer ODR.*
3. *The output of the temperature sensor is 0 LSB (typ.) at 25 °C.*
4. *Time from power ON to valid data based on characterization data.*

4.4 Communication interface characteristics

4.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top. @ Vdd_IO = 1.8 V, T = 25 °C unless otherwise noted.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)			Unit
		Min	Typ	Max	
$f_{c(SPC)}$	SPI clock frequency			10	MHz
$t_{c(SPC)}$	SPI clock period	100			ns
$t_{high(SPC)}$	SPI clock high	45			
$t_{low(SPC)}$	SPI clock low	45			
$t_{su(CS)}$	CS setup time (mode 3)	5			
	CS setup time (mode 0)	20			
$t_{h(CS)}$	CS hold time (mode 3)	20			
	CS hold time (mode 0)	20			
$t_{su(SI)}$	SDI input setup time	5			
$t_{h(SI)}$	SDI input hold time	15			
$t_{v(SO)}$	SDO valid output time		15	25	
$t_{dis(SO)}$	SDO output disable time			50	
C_{load}	Bus capacitance			100	pF

1. *Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production*

Figure 7. SPI slave timing in mode 0

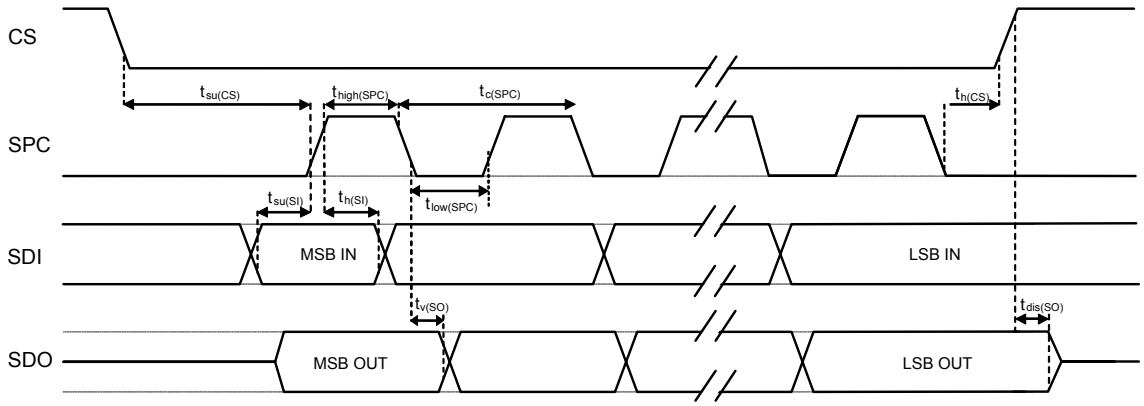
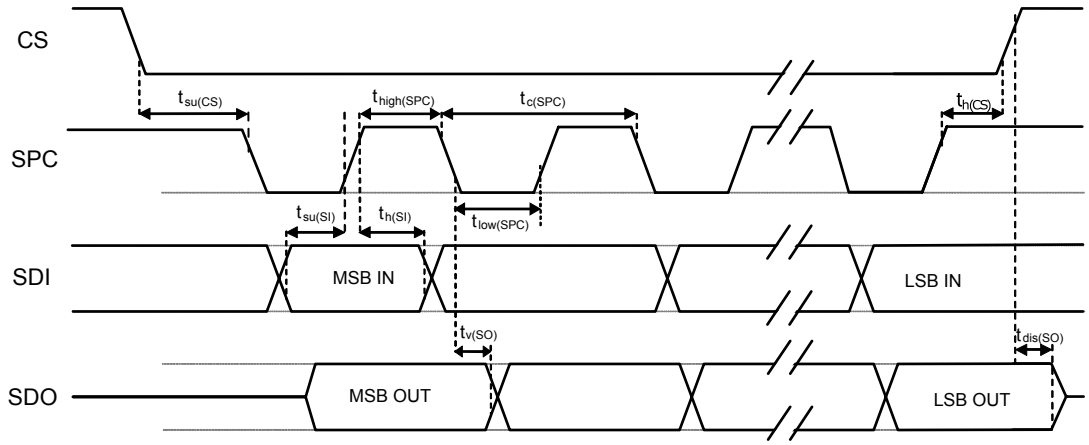


Figure 8. SPI slave timing in mode 3



Note: Measurement points are done at 0.3·Vdd_IO and 0.7·Vdd_IO for both input and output ports.

4.4.2 I²C - inter-IC control interface

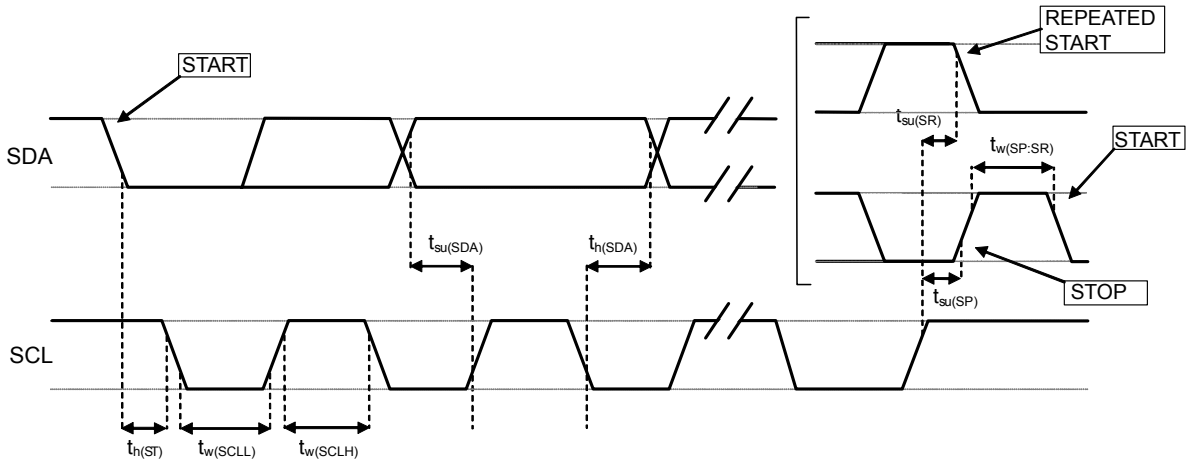
Subject to general operating conditions for Vdd and Top. @ Vdd_IO = 1.8 V, T = 25 °C unless otherwise noted.

Table 7. I²C slave timing values

Symbol	Parameter	I²C fast mode(1)(2)		I²C fast mode plus(1)(2)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	400	0	1000	kHz
$t_{w(SCLL)}$	SCL clock low time	1.3		0.5		µs
$t_{w(SCLH)}$	SCL clock high time	0.6		0.26		
$t_{su(SDA)}$	SDA setup time	100		50		ns
$t_{h(SDA)}$	SDA data hold time	0	0.9	0		µs
$t_{h(ST)}$	START/REPEATED START condition hold time	0.6		0.26		
$t_{su(SR)}$	REPEATED START condition setup time	0.6		0.26		
$t_{su(SP)}$	STOP condition setup time	0.6		0.26		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	1.3		0.5		
	Data valid time		0.9		0.45	
	Data valid acknowledge time		0.9		0.45	
C_B	Capacitive load for each bus line		400		550	pF

1. *Data based on standard I²C protocol requirement, not tested in production.*
2. *Data for I²C fast mode and I²C fast mode plus have been validated by characterization, not tested in production.*

Figure 9. I²C slave timing diagram



Note: Measurement points are done at 0.3·Vdd_IO and 0.7·Vdd_IO for both ports.

4.4.3 TDM - time-division multiplexing interface

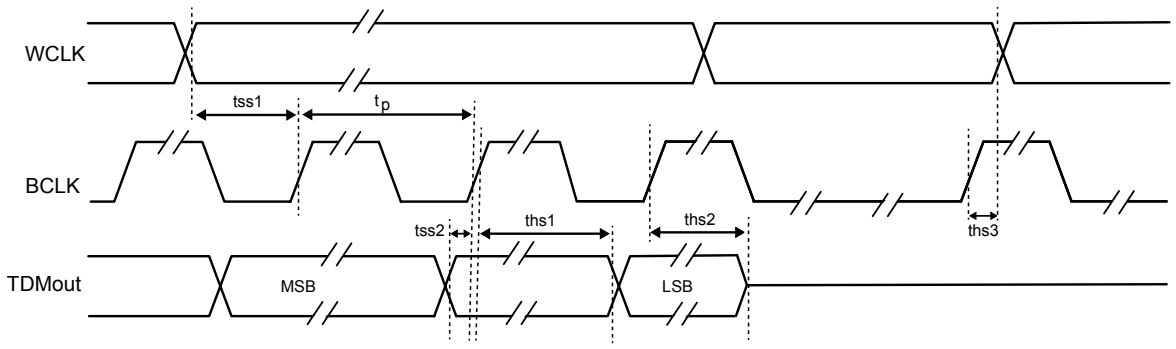
@ Vdd_IO = 1.8 V, T = 25 °C unless otherwise noted. Refer to Section 5.3 TDM interface for additional details.

Table 8. TDM timing values

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BCLK_f$	BCLK frequency ($1/t_p$)	WCLK = 16 kHz		2.048		MHz
BWCLKA	BCLK/WCLK frequency accuracy		-0.1		+0.1	%
$BCLK_j$	BCLK jitter				4	ns (peak to peak)
WCLK8	8 kHz WCLK mode			8		kHz
WCLK16	16 kHz WCLK mode			16		
PDC	All clock pin duty cycle - referred to BCLK (except WCLK)		45		55	%
WST	WCLK setup time before BCLK rising/falling edge (tss1)		20			ns
WHT	WCLK hold time after BCLK rising/falling edge (ths3)		20			ns
TDMST	TDMout setup time before BCLK rising/falling edge (tss2)		15			ns
TDMHTR	TDMout hold time after BCLK rising/falling edge (ths1)		15			ns
TDMHTZ	TDMout hold time of LSB after BCLK rising/falling edge (ths2)		15		65	ns
C_{BCLK}	BCLK pin capacitance				10	pF
C_{TDMout}	TDMout load capacitance				60	

Note: All setup times and hold times in Table 8 and in Figure 10 are valid for BCLK polarity set to "clock on rising". If BCLK polarity is set to "clock on falling", then all setup and hold times will refer to the falling edge of BCLK instead. Please refer to Section 5.3 TDM interface for additional details.

Figure 10. TDM timing diagram



4.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.2 ms	20,000	*g*
ESD	Electrostatic discharge protection (HBM)	2	kV
Vin	Input voltage on any control pin (including SDO/SA0, BCLK, WCLK, CS, SCL,SDA)	-0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4.6 Terminology

4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 g acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see Table 2).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see Table 2).

4.6.2 Zero-*g* and zero-rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0 *g* on both the X-axis and Y-axis, whereas the Z-axis measures 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in Table 2. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see Table 2).

5 Digital interfaces

5.1 I²C/SPI interface

The registers embedded inside the LSM6DSV16BX may be accessed through both the I²C and SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped to the same pins. To select/exploit the I²C interface, the CS line must be tied high (that is, connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS	Enables SPI I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO/SA0	SPI serial data output (SDO) I²C less significant bit of the device address

5.1.1 I²C serial interface

The LSM6DSV16BX I²C is a bus slave. The I²C is employed to write the data to the registers, whose content can also be read back.

The relevant I²C terminology is provided in the table below.

Table 11. I²C terminology

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both the lines are high.

The I²C interface is implemented with fast mode (400 kHz) I²C standards as well as with fast mode plus (1000 kHz).

In order to disable the I²C block, I2C_I3C_disable = 1 must be written in IF_CFG (03h).

5.1.2 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LSM6DSV16BX is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is 1 (address 1101011b). If the SDO/SA0 pin is connected to ground, the LSb value is 0 (address 1101010b). This solution permits to connect and address two different inertial modules to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the high period of the acknowledge clock pulse. A receiver that has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM6DSV16BX behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit subaddress (SUB) is transmitted. The increment of the address is configured by the CTRL3 (12h) (IF_INC).

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes. If the bit is 0 (write) the master transmits to the slave with direction unchanged. Table 12 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 12. SAD+read/write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 13. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 14. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 15. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 16. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+ W		SUB		SR	SAD+ R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

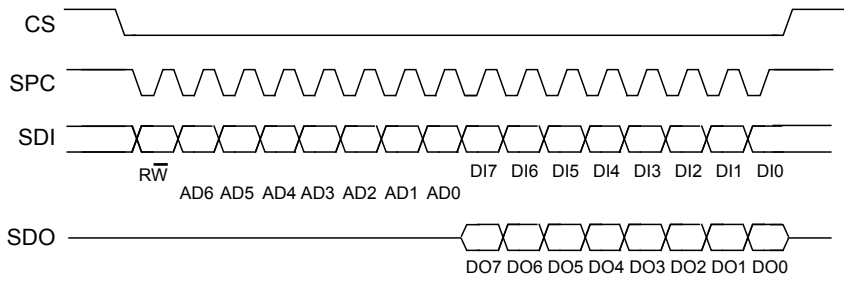
Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a slave receiver does not acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

In the presented communication format, MAK is master acknowledge and NMAK is no master acknowledge.

5.1.3 SPI bus interface

The SPI on the LSM6DSV16BX is a bus slave which allows writing and reading the registers of the device.

Figure 11. Read and write protocol (in mode 3)



CS enables the serial port and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: $\overline{RW}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

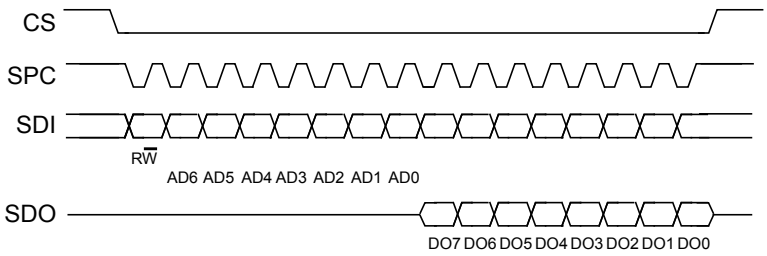
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the CTRL3 (12h) (IF_INC) bit is 0, the address used to read/write data remains the same for every block. When the CTRL3 (12h) (IF_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.1.3.1 SPI read

Figure 12. SPI read protocol (in mode 3)



The SPI Read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

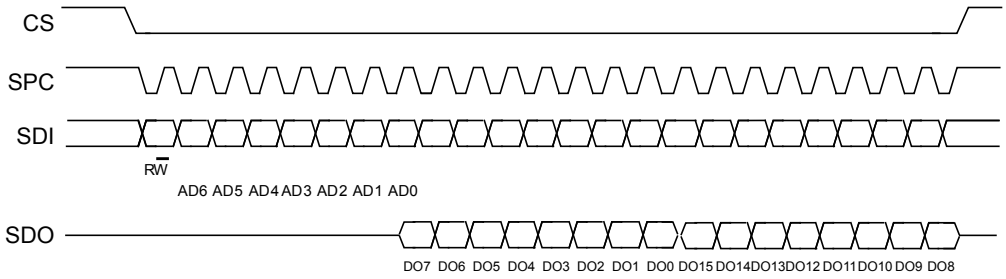
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

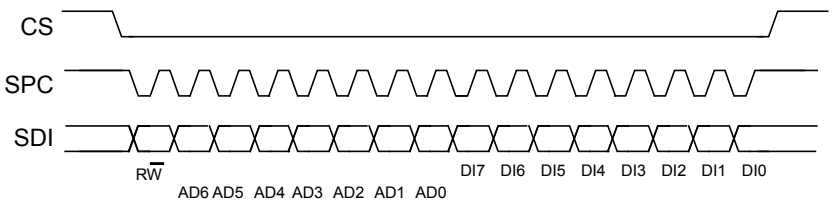
bit 16-...: data DO(...-8). Further data in multiple byte reads.

Figure 13. Multiple byte SPI read protocol (2-byte example) (in mode 3)



5.1.3.2 SPI write

Figure 14. **SPI write protocol (in mode 3)**



The SPI Write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

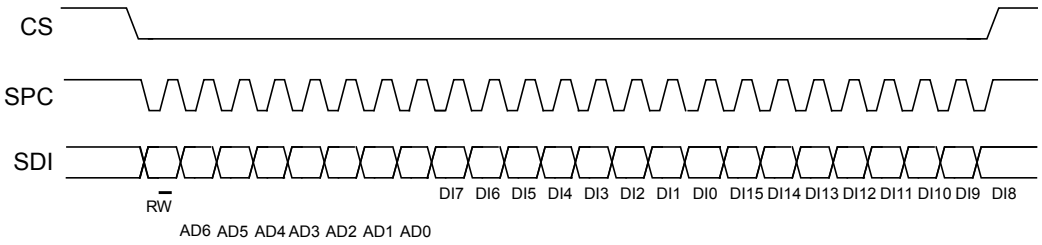
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

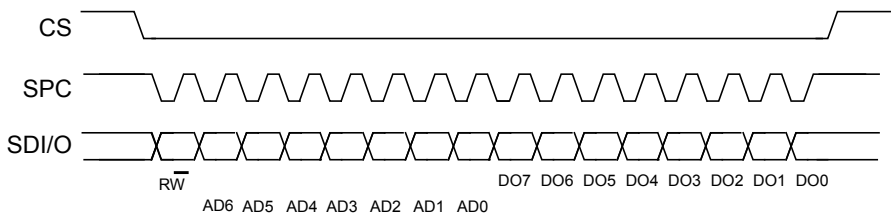
Figure 15. **Multiple byte SPI write protocol (2-byte example) (in mode 3)**



5.1.3.3 SPI read in 3-wire mode

3-wire mode is entered by setting the IF_CFG (03h) (SIM) bit equal to 1 (SPI serial interface mode selection).

Figure 16. **SPI read protocol in 3-wire mode (in mode 3)**



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

5.2 MIPI I3C® interface

5.2.1 MIPI I3C® slave interface

The LSM6DSV16BX interface includes an MIPI I3C® SDR only slave interface (compliant with release 1.1 of the specification) with MIPI I3C® SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- In-band interrupt request
- Slave reset pattern
- Group address
- Full range Vdd_IO support
- Asynchronous modes 0 and 1
- Error detection and recovery methods (S0-S6)

In order to disable the MIPI I3C® block, I2C_I3C_disable = 1 must be written in IF_CFG (03h).

5.2.2 MIPI I3C® CCC supported commands

The list of MIPI I3C® CCC commands supported by the device is detailed in the following table.

Table 17. MIPI I3C® CCC commands

Command	Command code	Default	Description
ENTDAA	0x07		DAA procedure
SETDASA	0x87		Assign dynamic address using static address 0x6B/0x6A depending on SDO pin
ENEC	0x80 / 0x00		Slave activity control (direct and broadcast)
DISEC	0x81/ 0x01		Slave activity control (direct and broadcast)
ENTAS0	0x82 / 0x02		Enter activity state (direct and broadcast)
SETXTIME	0x98 / 0x28		Timing information exchange
GETXTIME	0x99	0x06 0x00 0x06 0x92	Timing information exchange
RSTDAA	0x06		Reset the assigned dynamic address (broadcast only)
SETMWL	0x89 / 0x08		Define maximum write length during private write (direct and broadcast)
SETMRL	0x8A / 0x09		Define maximum read length during private read (direct and broadcast)
SETNEWDA	0x88		Change dynamic address
GETMWL	0x8B	0x00 0x08 (2 byte)	Get maximum write length during private write
GETMRL	0x8C	0x00 0x10 0x0A (3 byte)	Get maximum read length during private read

Command	Command code	Default	Description
GETPID	0x8D	0x02 0x08 0x00 0x71 0x92 0x0B	SDO = 1
		0x02 0x08 0x00 0x71 0x12 0x0B	SDO = 0
GETBCR	0x8E	0x27 (1 byte)	Bus characteristics register
GETDCR	0x8F	0x44 default	MIPI I3C® device characteristics register
GETSTATUS	0x90	0x00 0x00 (2 byte)	Status register
GETMXDS	0x94	0x08 0x60	Return max write and read speed
GETCAPS	0x95	0x00 0x11 0x18 0x00	Provide information about device capabilities and supported extended features
SETGRPA	0x9B		Group address assignment command
RSTGRPA	0x2C / 0x9C		Reset the group address
RSTACT	0x9A / 0x2A		Configure slave reset action

5.2.3 Overview of anti-spike filter management

The device acts as a standard I²C target as long as it has an I²C static address. The device is capable of detecting and disabling the I²C anti-spike filter after detecting the broadcast address (7'h7E/W). In order to guarantee proper behavior of the device, the I3C master must emit the first START, 7'h7E/W at open-drain speed using I²C fast mode plus reference timing.

After detecting the broadcast address, the device can receive the I3C dynamic address following the I3C push-pull timing. If the device is not assigned a dynamic address, then the device will continue to operate as an I²C device with no anti-spike filter. For the case in which the host decides to keep the device as I²C with anti-spike filter, there is a configuration required to keep the anti-spike filter active. This configuration is done by writing the ASF_CTRL bit to 1 in the IF_CFG (03h) register. This configuration forces the anti-spike filter to always be turned on instead of being managed by the communication on the bus.

5.3 TDM interface

Time-division multiplexing (TDM) is a method of putting multiple data streams in one data signal by separating the signal into many frames. There are many ways to accomplish this.

5.3.1 Frame synchronization (WCLK)

The function of the WCLK is simply to identify the beginning of a frame. In particular the frame starts at the rising edge of WCLK and the WCLK widths supported are:

- 50% duty cycle
- One slot width (16 BCLK)
- One BCLK width

In TDM mode, LSM6DSV16BX shall output accelerometer data on the TDMout pin at the following sampling rates:

- WCLK = 8 kHz
- WCLK = 16 kHz

5.3.2 Serial clock (BCLK)

The sole purpose of the serial clock BCLK is to shift the data out of the serial TDMout port. To this purpose, the TDM interface uses an internal counter that is set to one when the rising edge of the WCLK is detected, and it is reset to zero when the maximum number of BCLK in a WCLK period is reached.

The maximum number of BCLK contained in a WCLK period can be expressed as a function of both the BCLK and WCLK frequencies and can be computed using the following equation:

(1)

$$c\max = \frac{BCLK}{WCLK} - 1$$

5.3.3 Mapping the TDM axes

Within one frame, the data signal (DOUT) is divided into multiple segments. We call each segment a slot in this document.

The data slot width is fixed and equal to 16 bits.

In each slot, data should be left-justified (MSB first).

The number of slots in a WCLK frame can be variable and it depends on the ratio between BCLK and WCLK. However, as depicted in Table 18 and Table 19, only the slots 0, 1, 2 and 4, 5, 6 can be used to send accelerometer data, all the other slots are always set in high-impedance.

The mapping between the input data and the TDM output slots is flexible and can be configured through the I²C/SPI/I3C register mapping (TDM_CFG0 (6Ch)).

In particular two possible configurations can be selected:

- Axes data (Z, Y, X) mapped to TDM slots (0, 1, 2) (mapping = 0)
- Axes data (Z, Y, X) mapped to TDM slots (4, 5, 6) (mapping = 1)

Table 18. Axes Z, Y, X mapped to SLOT0, SLOT1, SLOT2

SLOT0	SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7	...	SLOTN
Z-axis	Y-axis	X-axis	HiZ	HiZ	HiZ	HiZ	HiZ		HiZ

Table 19. Axes Z, Y, X mapped to SLOT4, SLOT5, SLOT6

SLOT0	SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7	...	SLOTN
HiZ	HiZ	HiZ	HiZ	Z-axis	Y-axis	X-axis	HiZ		HiZ

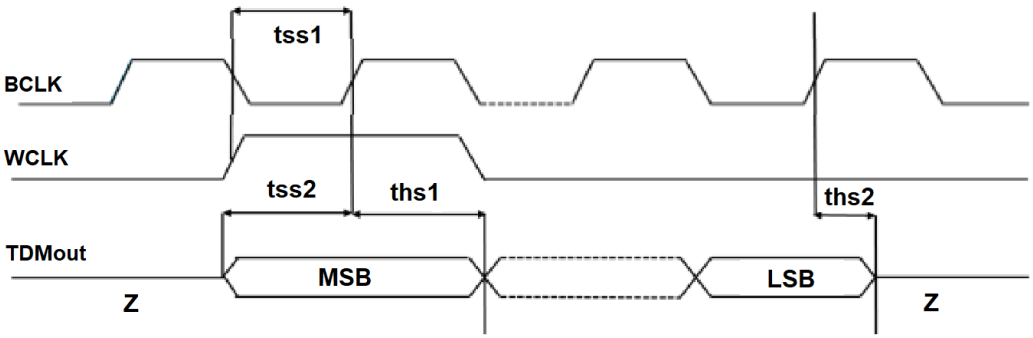
5.3.4 TDM configurations

All the LSM6DSV16BX TDM configurations programmable through the I²C/SPI/I3C interface are detailed in the following subsections.

5.3.4.1 Configuration 1

- No delay: SLOT0 data MSB is sampled on the first rising edge of BCLK after rising edge of WCLK (delayed I²C register TDM_CFG0 (6Ch) bit 6 equal to zero)
- Data valid: data valid on the rising edge of BCLK (data_valid I²C register TDM_CFG0 (6Ch) bit 5 equal to zero)

Figure 17. WCLK, TDMout change on the falling edge of BCLK and are valid on the rising edge of BCLK, no delay

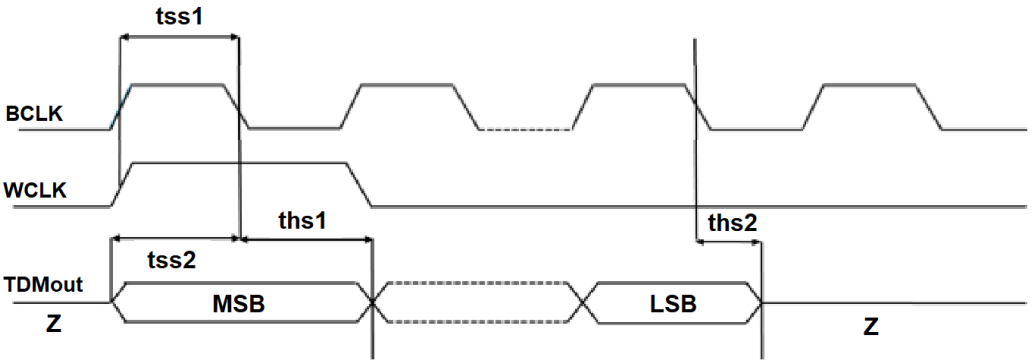


Note: Setup and hold times are defined in Table 8. TDM timing values.

5.3.4.2 Configuration 2

- No delay: SLOT0 data MSB is sampled on the first falling edge of BCLK after rising edge of WCLK (delayed I²C register TDM_CFG0 (6Ch) bit 6 equal to zero)
- Data valid: data valid on the falling edge of BCLK (data_valid I²C register TDM_CFG0 (6Ch) bit 5 equal to one)

Figure 18. WCLK, TDMout change on the rising edge of BCLK and are valid on the falling edge of BCLK, no delay

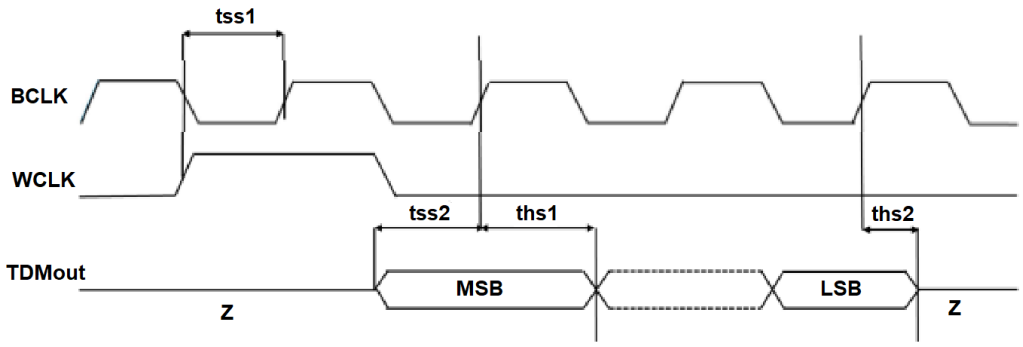


Note: Setup and hold times are defined in Table 8. TDM timing values.

5.3.4.3 Configuration 3

- Delayed: SLOT0 data MSB is sampled on the second rising edge of BCLK after rising edge of WCLK (delayed I²C register TDM_CFG0 (6Ch) bit 6 equal to one)
- Data valid: data valid on the rising edge of BCLK (data_valid I²C register TDM_CFG0 (6Ch) bit 5 equal to zero)

Figure 19. WCLK, TDMout change on the falling edge of BCLK and are valid on the rising edge of BCLK, delayed

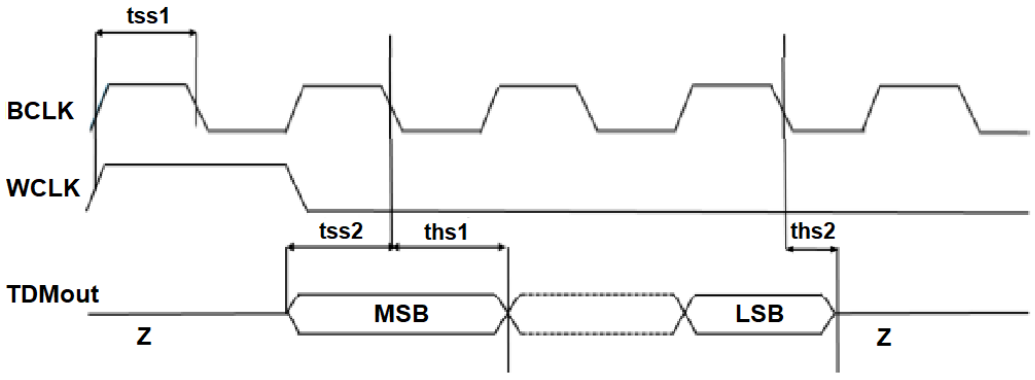


Note: Setup and hold times are defined in Table 8. TDM timing values.

5.3.4.4 Configuration 4

- Delayed: SLOT0 data MSB is sampled on the second falling edge of BCLK after rising edge of WCLK (delayed I²C register TDM_CFG0 (6Ch) bit 6 equal to one)
- Data valid: data valid on the falling edge of BCLK (data_valid I²C register TDM_CFG0 (6Ch) bit 5 equal to one)

Figure 20. WCLK, TDMout change on the rising edge of BCLK and are valid on the falling edge of BCLK, delayed



Note: Setup and hold times are defined in Table 8. TDM timing values.

6 Functionality

6.1 Operating modes

In the LSM6DSV16BX, the accelerometer and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

The LSM6DSV16BX has three operating modes available:

- only accelerometer active and gyroscope in power-down
- only gyroscope active and accelerometer in power-down
- both accelerometer and gyroscope sensors active with independent ODR and power mode

The accelerometer is activated from power-down by writing ODR_XL_[3:0] in CTRL1 (10h) while the gyroscope is activated from power-down by writing ODR_G_[3:0] in CTRL2 (11h). For combo mode the ODRs are totally independent.

In addition to the accelerometer mode above, a dedicated TDM output can be used for the audio accelerometer output.

6.2 Accelerometer power modes

In the LSM6DSV16BX, the accelerometer can be configured in three different operating modes: power-down mode, low-power mode and high-performance mode.

The operating mode selected depends on the value of the OP_MODE_XL_[2:0] bits in CTRL1 (10h).

If the value of the OP_MODE_XL_[2:0] bits is 000 (default), high-performance mode is valid for all ODRs (from 7.5 Hz up to 7.68 kHz).

In high-performance mode the analog anti-aliasing filter is active.

Low-power mode is available for lower ODRs (1.875 Hz, 15 Hz, 30 Hz, 60 Hz, 120 Hz, 240 Hz). The three low-power modes are enabled by setting OP_MODE_XL_[2:0] to 100 (LPM1), 101 (LPM2), 110 (LPM3).

The embedded functions based on accelerometer data (free-fall, 6D, tap/double-tap, wake-up, activity/inactivity, stationary/motion, step counter, step detection, significant motion, tilt) and the FIFO batching functionality are supported in all modes.

6.3 Accelerometer dual-channel mode

The LSM6DSV16BX accelerometer block has a dual-channel architecture able to work with two different full scales simultaneously. By default, the device operates in single-channel mode supporting FS scale values from ±2 *g* through ±16 *g* and different power modes, as described in Section 6.2 Accelerometer power modes. The block diagrams in the following figures show the configuration of acceleration data processing in the two different modes.

Figure 21. Single-channel mode (XL_DualC_EN = 0)

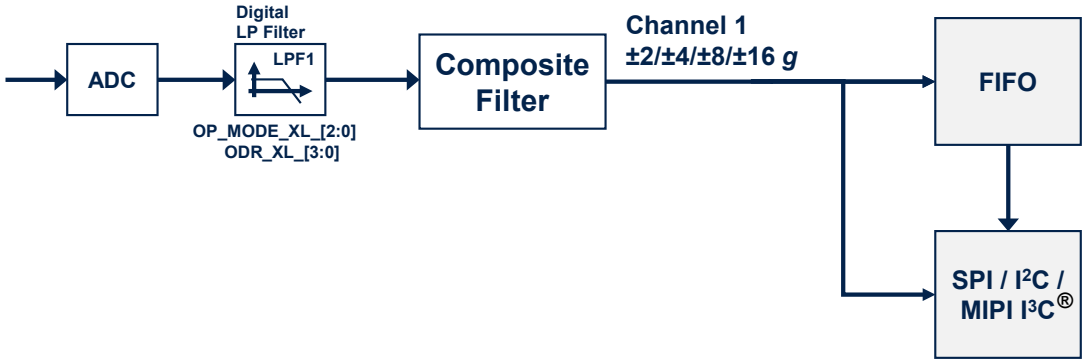
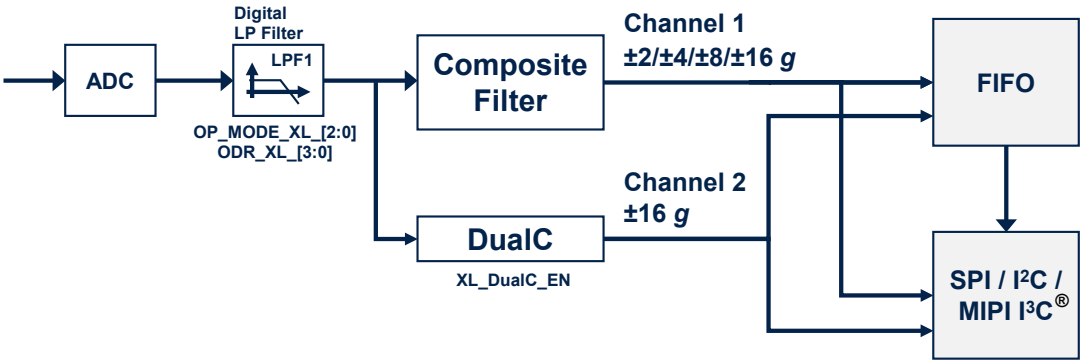


Figure 22. Dual-channel mode (XL_DualC_EN = 1)



The dual-channel functionality can be enabled/disabled by configuring the bit XL_DualC_EN to 1 (enable) or to 0 (disable) in CTRL8 (17h).

Referring to Figure 22. Dual-channel mode (XL_DualC_EN = 1), when the dual-channel mode has been activated:

1. Channel 1 supports user-selectable full-scale acceleration range of ±2/±4/±8/±16 *g* based on the value of the FS_XL_[1:0] bits in the CTRL8 (17h) register.
2. Channel 2 full scale is set to ±16 *g*. Acceleration data are available in the output registers from UI_OUTZ_L_A_DualC (34h) and UI_OUTZ_H_A_DualC (35h) through UI_OUTX_L_A_DualC (38h) and UI_OUTX_H_A_DualC (39h)).

6.4 Gyroscope power modes

In the LSM6DSV16BX, the gyroscope can be configured in four different operating modes: power-down mode, sleep mode, low-power mode and high-performance mode.

The operating mode selected depends on the value of the OP_MODE_G_[2:0] bits in CTRL2 (11h).

If the value of the OP_MODE_G_[2:0] bits is 000 (default), high-performance mode is valid for all ODRs (from 7.5 Hz up to 7.68 kHz).

Low-power mode is available for lower ODRs (7.5 Hz, 15 Hz, 30 Hz, 60 Hz, 120 Hz, 240 Hz) and it is enabled by setting the the OP_MODE_G_[2:0] bits to 101.

6.5 Analog hub functionality

The LSM6DSV16BX embeds an analog hub sensing functionality which is able to connect an analog input and convert it to a digital signal for embedded processing.

In the LSM6DSV16BX, the analog hub has a dedicated channel that can be activated by setting the AH_QVAR_EN bit and the AH_QVAR1_EN / AH_QVAR2_EN bits to 1 in the CTRL7 (16h) register.

The accelerometer sensor must be set in high-performance mode or in normal mode when the analog hub channel is enabled.

The analog hub data-ready signal is represented by the AH_QVARDA bit of the STATUS_REG (1Eh) register. This signal can be driven to the INT2 pin by setting the INT2_DRDY_AH_QVAR bit to 1 in the CTRL7 (16h) register.

Analog hub data are available as a 16-bit word in two's complement in the AH_QVAR_OUT_L (3Ah) and AH_QVAR_OUT_H (3Bh) registers.

Analog signal data can be also processed by MLC/FSM logic.

The AH_QVAR_LPF bit in the CTRL9 (18h) register and the AH_QVAR_HPF bit in the CTRL8 (17h) register are used to enable/disable, respectively, the embedded digital notch filter and the embedded digital high-pass filter and to set the analog hub data rate and the overall bandwidth of the analog hub channel as shown in Table 20.

Analog hub data can be stored in FIFO (by setting the AH_QVAR_BATCH_EN bit to 1 in the COUNTER_BDR_REG1 (0Bh) register) and can also be processed by MLC/FSM logic.

The equivalent input impedance of the analog hub buffers can be selected by properly setting the AH_QVAR_C_ZIN_[1:0] bits in the CTRL7 (16h) register.

Finally, the AH_QVAR_SW bit in the CTRL7 (16h) register allows internally swapping the input connected to the AH1/QVAR1 and AH2/QVAR2 pins.

6.6 Qvar functionality

The LSM6DSV16BX embeds a Qvar sensor which is able to detect electric charge variations in the proximity of the external electrodes connected to the device.

In the LSM6DSV16BX, Qvar has a dedicated channel that can be activated by setting the AH_QVAR_EN bit and the AH_QVAR1_EN / AH_QVAR2_EN bits to 1 in the CTRL7 (16h) register.

The accelerometer sensor must be set in high-performance mode when the Qvar channel is enabled.

The Qvar data-ready signal is represented by the AH_QVARDA bit of the STATUS_REG (1Eh) register. This signal can be driven to the INT2 pin by setting the INT2_DRDY_AH_QVAR bit to 1 in the CTRL7 (16h) register.

Qvar data are available as a 16-bit word in two's complement in the AH_QVAR_OUT_L (3Ah) and AH_QVAR_OUT_H (3Bh) registers.

The AH_QVAR_LPF bit in the CTRL9 (18h) register and the AH_QVAR_HPF bit in the CTRL8 (17h) register are used to enable/disable, respectively, the embedded digital notch filter and the embedded digital high-pass filter and to set the Qvar data rate and the overall bandwidth of the Qvar channel as shown in Table 20.

Table 20. Analog hub / Qvar channel ODR and bandwidth configuration

AH_QVAR_LPF	AH_QVAR_HPF	AH / Qvar ODR (typ.)(1)	AH / Qvar bandwidth (typ.) [low, high]
0	0	240 Hz	[0 Hz, 318 Hz]
0	1	240 Hz	[0.15 Hz, 318 Hz]
1	0	120 Hz	[0 Hz, 14.8 Hz](2)
1	1	120 Hz	[0.08 Hz, 14.8 Hz](2)

1. *The analog hub / Qvar channel ODR is equal to 240 Hz if the notch filter is disabled, otherwise the ODR is equal to 120 Hz.*
2. *First -3 dB crossing point*

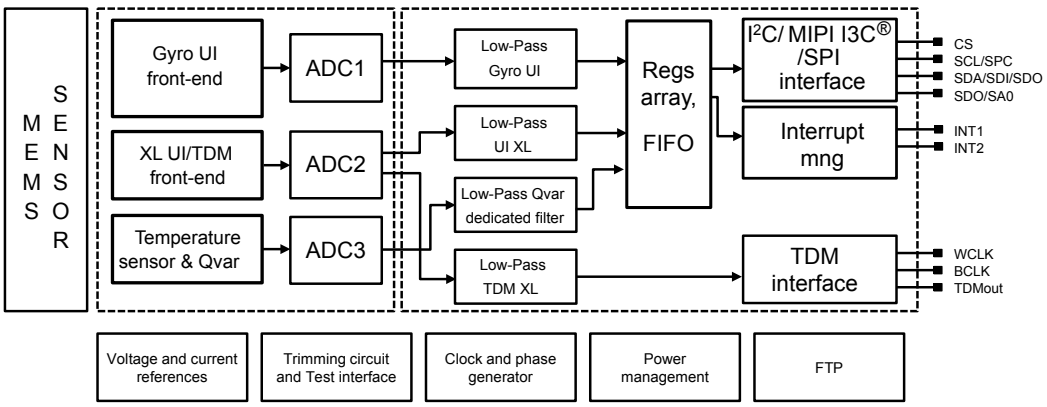
Qvar data can be stored in FIFO (by setting the AH_QVAR_BATCH_EN bit to 1 in the COUNTER_BDR_REG1 (0Bh) register) and can also be processed by MLC/FSM logic.

The equivalent input impedance of the Qvar buffers can be selected by properly setting the AH_QVAR_C_ZIN_[1:0] bits in the CTRL7 (16h) register.

Finally, the AN_QVAR_SW bit in the CTRL10 (19h) register allows internally swapping the input electrodes connected to the AH1/QVAR1 and AH2/QVAR2 pins.

6.7 Block diagram of filters

Figure 23. Block diagram of filters



6.7.1 Block diagrams of the accelerometer filters

In the LSM6DSV16BX, the filtering chain for the accelerometer part is composed of the following:

- Digital filter (LPF1)
- Composite filter

Details of the block diagram appear in the following figure.

Figure 24. Accelerometer UI chain

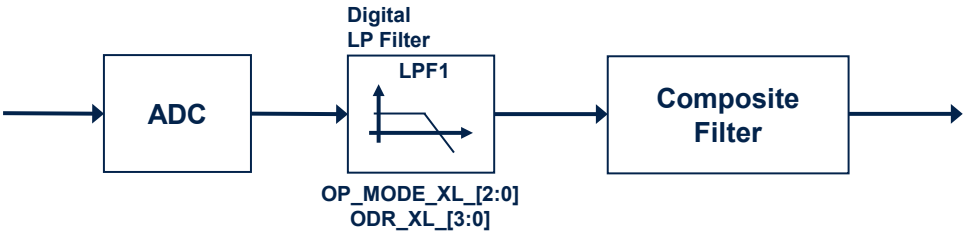
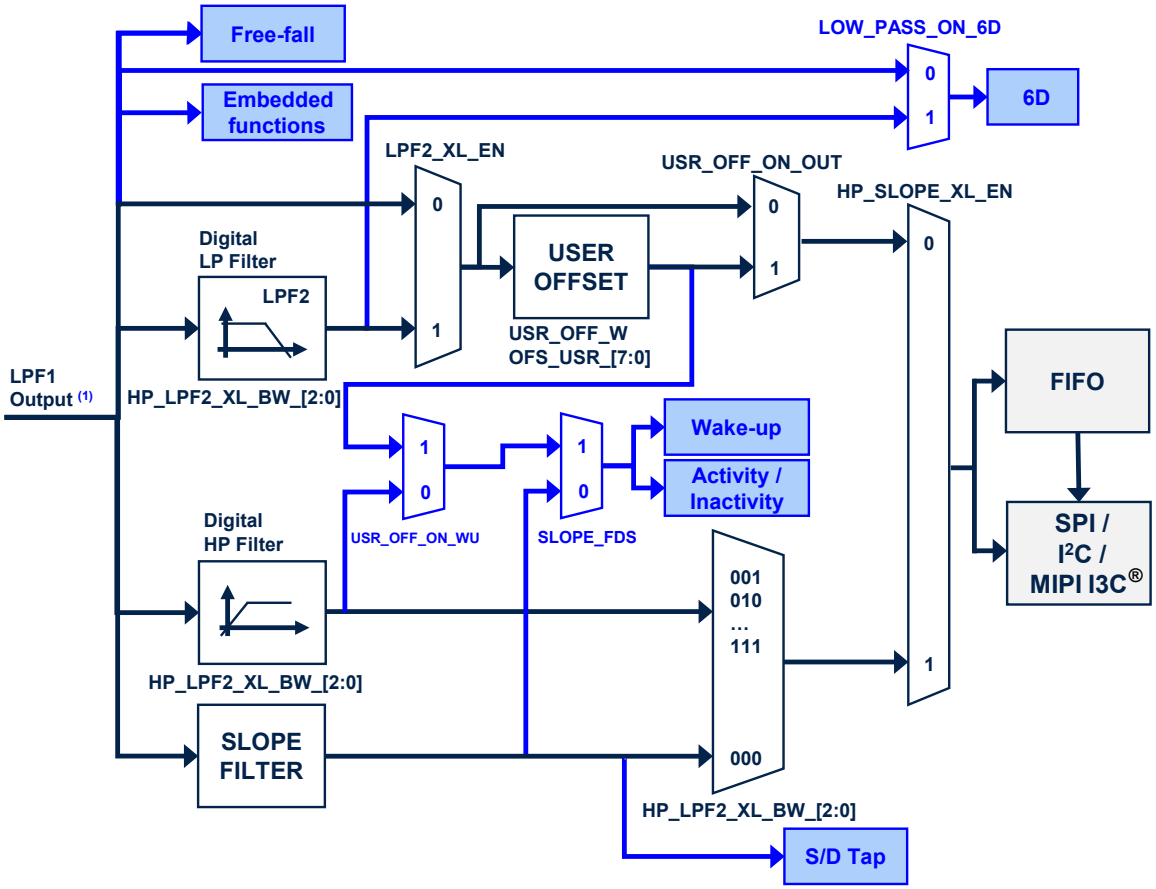


Figure 25. Accelerometer composite filter



1. *The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode. This value is equal to 3100 Hz when the accelerometer is in low-power mode 1 (2 mean), 912 Hz in low-power mode 2 (4 mean) or 431 Hz in low-power mode 3 (8 mean).*

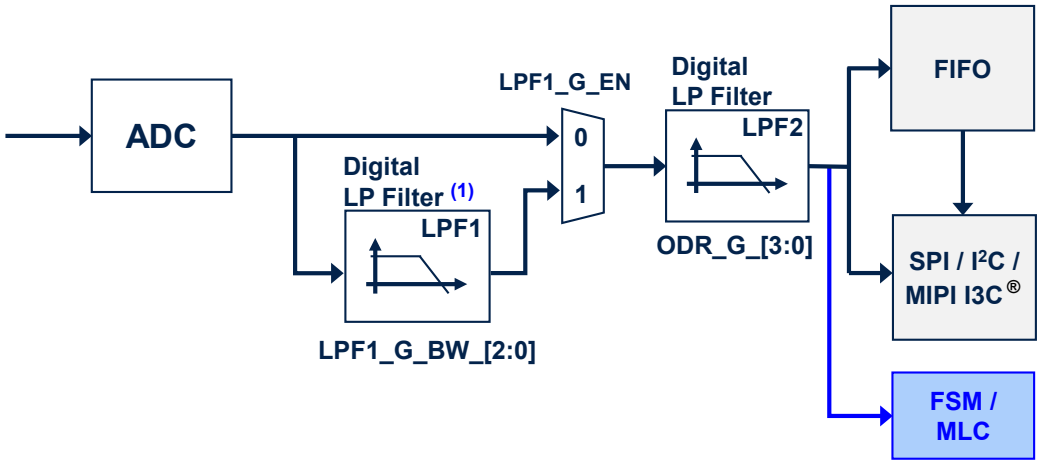
Note: Embedded functions include finite state machine, machine learning core, pedometer, step detector and step counter, significant motion detection, and tilt functions.

6.7.2 Block diagrams of the gyroscope filters

In the LSM6DSV16BX, the gyroscope filtering chain depends on the mode configuration:

- Mode 1 (for user interface (UI) functionality through primary interface) and mode 2

Figure 26. Gyroscope digital chain - mode 1 (UI) and mode 2



1. *The LPF1 filter is available in high-performance mode only. If the gyroscope is configured in low-power mode, the LPF1 filter is bypassed.*

In this configuration, the gyroscope ODR is selectable from 7.5 Hz up to 7.68 kHz. A low-pass filter (LPF1) is available, for more details about the filter characteristics see Table 61. Gyroscope LPF1 bandwidth selection.

The digital LPF2 filter's cutoff frequency depends on the selected gyroscope ODR, as indicated in the following table.

Table 21. Gyroscope LPF2 bandwidth selection

Gyroscope ODR [Hz]	LPF2 cutoff [Hz]
7.5	3.4
15	6.6
30	13.0
60	24.6
120	49
240	96
480	185
960	353
1.92 kHz	491
3.84 kHz	528
7.68 kHz	537

Note: Data can be acquired from the output registers and FIFO over the primary I²C/MIPI I3C®/SPI interface.

6.8 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but It can wake up only when needed and burst the significant data out from the FIFO.

The LSM6DSV16BX embeds 1.5 KB of data in FIFO (up to 4.5 KB with the compression feature enabled) to store the following data:

- Gyroscope
- Accelerometer
- Qvar
- Step counter
- Timestamp
- Temperature
- MLC features and filters
- SFLP output data (quaternion, gyroscope bias, gravity vector)

Writing data in the FIFO can be configured to be triggered by the:

- Accelerometer / gyroscope data-ready signal
- Step detection signal

The applications have maximum flexibility in choosing the rate of batching for physical sensors with FIFO-dedicated configurations: accelerometer, gyroscope and temperature sensor batch rates can be selected by the user. The step counter can be stored in FIFO with associated timestamp each time a step is detected. It is possible to select decimation for timestamp batching in FIFO with a factor of 1, 8, or 32.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO_DATA_OUT_TAG byte that allows recognizing the meaning of a word in FIFO.

FIFO allows correct reconstruction of the timestamp information for each sensor stored in FIFO. If a change in the ODR or BDR (batch data rate) configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

Finally, FIFO embeds a compression algorithm that the user can enable in order to have up to 4.5 KB data stored in FIFO and take advantage of interface communication length for FIFO flushing and communication power consumption.

The programmable FIFO watermark threshold can be set in the FIFO_CTRL1 (07h) register using the WTM[7:0] bits. To monitor the FIFO status, dedicated registers (FIFO_STATUS1 (1Bh), FIFO_STATUS2 (1Ch)) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO watermark status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pins of these status events, the configuration can be set in INT1_CTRL (0Dh) and INT2_CTRL (0Eh).

The FIFO buffer can be configured according to seven different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- ContinuousWTM-to-full mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

Each mode is selected by the FIFO_MODE_[2:0] bits in the FIFO_CTRL4 (0Ah) register.

6.8.1 Bypass mode

In Bypass mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 000), the FIFO is not operational and it remains empty. Bypass mode is also used to reset the FIFO when in FIFO mode.

6.8.2 FIFO mode

In FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, bypass mode should be selected by writing FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0]) to 000. After this reset command, it is possible to restart FIFO mode by writing FIFO_CTRL4 (0Ah) (FIFO_MODE_[2:0]) to 001.

The FIFO buffer memorizes up to 4.5 KB of data (with compression enabled) but the depth of the FIFO can be resized by setting the WTM[7:0] bits in FIFO_CTRL1 (07h). If the STOP_ON_WTM bit in FIFO_CTRL2 (08h) is set to 1, FIFO depth is limited up to the WTM[7:0] bits in the FIFO_CTRL1 (07h) register.

6.8.3 Continuous mode

Continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag FIFO_STATUS2 (1Ch)(FIFO_WTM_IA) is asserted when the number of unread samples in FIFO is greater than or equal to FIFO_CTRL1 (07h) (WTM[7:0]).

It is possible to route the FIFO_WTM_IA flag to the INT1 pin by writing in register INT1_CTRL (0Dh) (INT1_FIFO_TH) = 1 or to the INT2 pin by writing in register INT2_CTRL (0Eh)(INT2_FIFO_TH) = 1.

A full-flag interrupt can be enabled, INT1_CTRL (0Dh)(INT1_FIFO_FULL) = 1 or INT2_CTRL (0Eh) (INT2_FIFO_FULL) = 1, in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the FIFO_OVR_IA flag in FIFO_STATUS2 (1Ch) is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in FIFO_STATUS1 (1Bh) and FIFO_STATUS2 (1Ch)(DIFF_FIFO_[8:0]).

6.8.4 Continuous-to-FIFO mode

In continuous-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to 1, FIFO operates in FIFO mode.

When the selected trigger bit is equal to 0, FIFO operates in continuous mode.

6.8.5 ContinuousWTM-to-full mode

In continuousWTM-to-full mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 010), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to 0, FIFO operates in continuous mode with the FIFO size limited to the FIFO watermark level (defined by the WTM[7:0] bits in the FIFO_CTRL1 (07h) register).

When the selected trigger bit is equal to 1, FIFO continues to store data until it is full.

6.8.6 Bypass-to-continuous mode

In bypass-to-continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 100), data measurement storage inside FIFO operates in continuous mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

6.8.7 Bypass-to-FIFO mode

In bypass-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 111), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

6.8.8 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (FIFO_DATA_OUT_TAG (78h), in order to identify the sensor, and 6 bytes of fixed data (FIFO_DATA_OUT registers from (79h) to (7Eh)).

The DIFF_FIFO_[8:0] field in the FIFO_STATUS1 (1Bh) and FIFO_STATUS2 (1Ch) registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

In addition, it is possible to configure a counter of the batch events of accelerometer or gyroscope sensors. The flag COUNTER_BDR_IA in FIFO_STATUS2 (1Ch) alerts that the counter reaches a selectable threshold (CNT_BDR_TH_[9:0] field in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch)). This allows triggering the reading of FIFO with the desired latency of one single sensor. The sensor is selectable using the TRIG_COUNTER_BDR_[1:0] bits in COUNTER_BDR_REG1 (0Bh). As for the other FIFO status events, the flag COUNTER_BDR_IA can be routed on the INT1 or INT2 pins by asserting the corresponding bits (INT1_CNT_BDR of INT1_CTRL (0Dh) and INT2_CNT_BDR of INT2_CTRL (0Eh)).

In order to maximize the amount of accelerometer and gyroscope data in FIFO, the user can enable the compression algorithm by setting to 1 both the FIFO_COMPR_EN bit in EMB_FUNC_EN_B (05h) (embedded functions registers bank) and the FIFO_COMPR_RT_EN bit in FIFO_CTRL2 (08h). When compression is enabled, it is also possible to force writing non-compressed data at a selectable rate using the UNCOMPR_RATE_[1:0] field in FIFO_CTRL2 (08h).

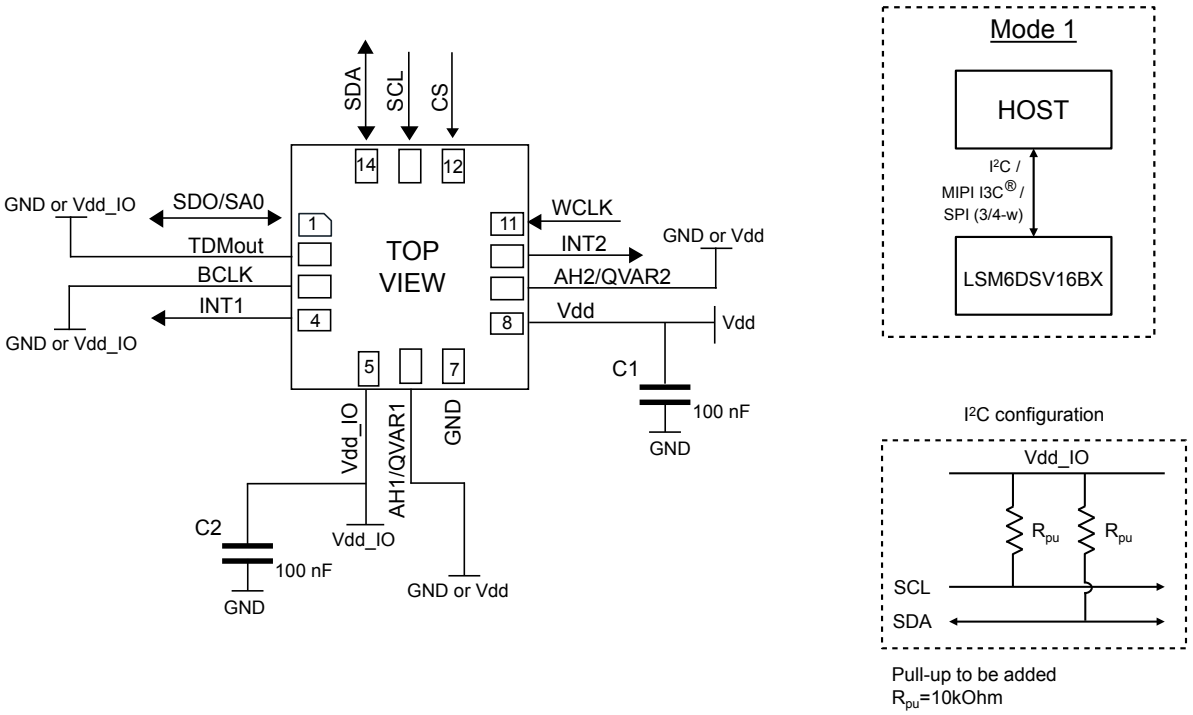
Meta information about accelerometer and gyroscope sensor configuration changes can be managed by enabling the ODR_CHG_EN bit in FIFO_CTRL2 (08h).

7 Application hints

7.1 LSM6DSV16BX electrical connections in mode 1

In this specific example, Qvar is not used.

Figure 27. LSM6DSV16BX electrical connections in mode 1



1. *Leave pin electrically unconnected and soldered to PCB.*

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

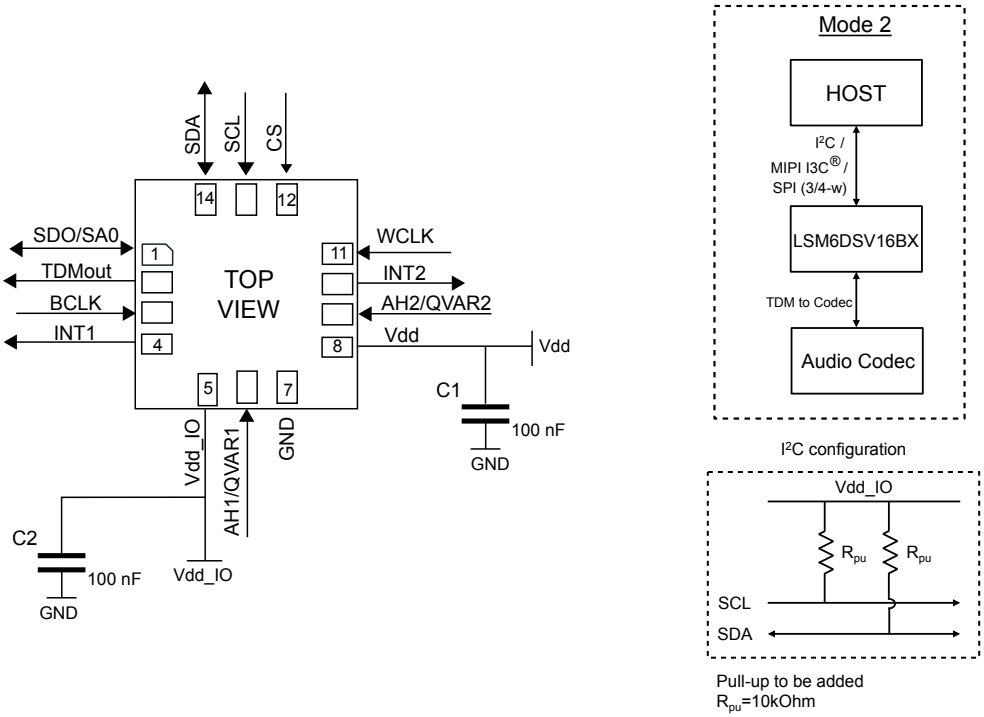
The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C® interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C® interface.

7.2 LSM6DSV16BX electrical connections in mode 2

In this specific example, Qvar is used.

Figure 28. LSM6DSV16BX electrical connections in mode 2



The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C® primary interface.

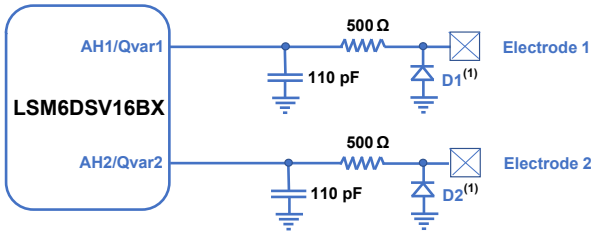
The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C® primary interface.

7.3 LSM6DSV16BX electrical connections for Qvar

The Qvar core is available in both mode 1 and mode 2 connection modes. It can be enabled by setting to 1 the AH_QVAR_EN bit and the AH_QVAR1_EN / AH_QVAR2_EN bit in the CTRL7 (16h) register.

The Qvar external electrode connections are illustrated in the following figure.

Figure 29. Qvar external connections to pin 6, 9 (Qvar input)



(1) ST ESDALCL5-1BM2 is referenced as an ST catalog product but similar features of other ESD diodes also can be used.

Note: Figure 29 provides an example of a test circuit. For a specific application, refer to the related application note.

7.4 LSM6DSV16BX internal pin status

Table 22. Internal pin status

Pin#	Name	Mode 1 function	Mode 2 function	Pin status mode 1	Pin status mode 2
1	SDO	SPI 4-wire interface serial data output (SDO)	SPI 4-wire interface serial data output (SDO)	Default: input without pull-up. Pull-up is enabled if bit SDO_PU_EN = 1 in reg 02h.	Default: input without pull-up. Pull-up is enabled if bit SDO_PU_EN = 1 in reg 02h.
	SA0	I²C least significant bit of the device address (SA0) MIPI I3C® least significant bit of the static address (SA0)	I²C least significant bit of the device address (SA0) MIPI I3C® least significant bit of the static address (SA0)		
2	TDMout	Connect to GND or Vdd_IO	TDM out	Default : input without pull-up. Pull-up is enabled if TDM_OUT_PU_EN =1 in reg. 03h.	Default : input without pull-up. Pull-up is enabled if TDM_OUT_PU_EN =1 in reg. 03h.
3	BCLK	Connect to GND or Vdd_IO	TDM bit clock	Input without pull-up	Input without pull-up
4	INT1	Programmable interrupt in I²C and SPI	Programmable interrupt in I²C and SPI	Default: output forced to ground	Default: output forced to ground
5	Vdd_IO	Power supply for I/O pins	Power supply for I/O pins		
6	AH1/QVAR1	Connect to Vdd or GND if the analog hub and/or Qvar are disabled. Connect to the analog input or Qvar electrode 1 if the AH/Qvar function is enabled.(1)	Connect to Vdd or GND if the analog hub and/or Qvar are disabled. Connect to the analog input or Qvar electrode 1 if the AH/Qvar function is enabled.(1)		
7	GND	0 V supply	0 V supply		
8	Vdd	Power supply	Power supply		
9	AH2/QVAR2	Connect to Vdd or GND if the analog hub and/or Qvar are disabled. Connect to the analog input or Qvar electrode 2 if the AH/Qvar function is enabled.(1)	Connect to Vdd or GND if the analog hub and/or Qvar are disabled. Connect to the analog input or Qvar electrode 2 if the AH/Qvar function is enabled.(1)		
10	INT2	Programmable interrupt in I²C and SPI	Programmable interrupt in I²C and SPI	Default: output forced to ground	Default: output forced to ground
11	WCLK	Connect to Vdd_IO or leave unconnected	TDM word clock	Default : input with pull up. Pull-up is disabled if TDM_WCLK_PU_DIS = 1 in reg. 02h.	Default : input with pull-up. Pull-up is disabled if TDM_WCLK_PU_DIS = 1 in reg. 02h.
12	CS	I²C/SPI mode selection (1:SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)	I²C/SPI mode selection (1:SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)	Default: input with pull-up. Pull-up is disabled if bit I2C_I3C_disable = 1 in reg 03h.	Default: input with pull-up. Pull-up is disabled if bit I2C_I3C_disable = 1 in reg 03h.
13	SCL	I²C/MIPI I3C® serial clock (SCL) / SPI serial port clock (SPC)	I²C/MIPI I3C® serial clock (SCL) / SPI serial port clock (SPC)	Default: input without pull-up	Default: input without pull-up
14	SDA	I²C/MIPI I3C® serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	I²C/MIPI I3C® serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	Default: input without pull-up. Pull-up is enabled if bit SDA_PU_EN = 1 in reg 03h.	Default: input without pull-up. Pull-up is enabled if bit SDA_PU_EN = 1 in reg 03h.

1. *The analog hub and Qvar functions are enabled by setting the AH_QVAR_EN bit to 1 in CTRL7 (16h).*

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on Vdd_IO.

8 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

All these registers are accessible from the primary SPI/I²C/MIPI I3C® interface only.

Table 23. Registers address map

Name	Type	Register address		Default
		Hex	Binary	
FUNC_CFG_ACCESS	R/W	01	00000001	00000000
PIN_CTRL	R/W	02	00000010	00100011
IF_CFG	R/W	03	00000011	00000000
RESERVED	-	04-06		
FIFO_CTRL1	R/W	07	00000111	00000000
FIFO_CTRL2	R/W	08	00001000	00000000
FIFO_CTRL3	R/W	09	00001001	00000000
FIFO_CTRL4	R/W	0A	00001010	00000000
COUNTER_BDR_REG1	R/W	0B	00001011	00000000
COUNTER_BDR_REG2	R/W	0C	00001100	00000000
INT1_CTRL	R/W	0D	00001101	00000000
INT2_CTRL	R/W	0E	00001110	00000000
WHO_AM_I	R	0F	00001111	01110001
CTRL1	R/W	10	00010000	00000000
CTRL2	R/W	11	00010001	00000000
CTRL3	R/W	12	00010010	01000100
CTRL4	R/W	13	00010011	00000000
CTRL5	R/W	14	00010100	00000000
CTRL6	R/W	15	00010101	00000000
CTRL7	R/W	16	00010110	00000000
CTRL8	R/W	17	0001 0111	00000000
CTRL9	R/W	18	00011000	00000000
CTRL10	R/W	19	00011001	00000000
CTRL_STATUS	R	1A	00011010	output
FIFO_STATUS1	R	1B	00011011	output
FIFO_STATUS2	R	1C	00011100	output
ALL_INT_SRC	R	1D	00011101	output
STATUS_REG	R	1E	00011110	output
RESERVED	-	1F	00011111	
OUT_TEMP_L	R	20	00100000	output
OUT_TEMP_H	R	21	00100001	output
OUTX_L_G	R	22	00100010	output
OUTX_H_G	R	23	00100011	output
OUTY_L_G	R	24	00100100	output

Name	Type	Register address		Default
		Hex	Binary	
OUTY_H_G	R	25	00100101	output
OUTZ_L_G	R	26	00100110	output
OUTZ_H_G	R	27	00100111	output
OUTZ_L_A	R	28	00101000	output
OUTZ_H_A	R	29	00101001	output
OUTY_L_A	R	2A	00101010	output
OUTY_H_A	R	2B	00101011	output
OUTX_L_A	R	2C	00101100	output
OUTX_H_A	R	2D	00101101	output
RESERVED	-	2E-33		
UI_OUTZ_L_A_DualC	R	34	00110100	output
UI_OUTZ_H_A_DualC	R	35	00110101	output
UI_OUTY_L_A_DualC	R	36	00110110	output
UI_OUTY_H_A_DualC	R	37	00110111	output
UI_OUTX_L_A_DualC	R	38	00111000	output
UI_OUTX_H_A_DualC	R	39	00111001	output
AH_QVAR_OUT_L	R	3A	00111010	output
AH_QVAR_OUT_H	R	3B	00111011	output
RESERVED	-	3C-3F		
TIMESTAMP0	R	40	01000000	output
TIMESTAMP1	R	41	01000001	output
TIMESTAMP2	R	42	01000010	output
TIMESTAMP3	R	43	01000011	output
RESERVED	-	44	01000100	
WAKE_UP_SRC	R	45	01000101	output
TAP_SRC	R	46	01000110	output
D6D_SRC	R	47	01000111	output
RESERVED	-	48	01001000	
EMB_FUNC_STATUS_ MAINPAGE	R	49	01001001	output
FSM_STATUS_MAINPAGE	R	4A	01001010	output
MLC_STATUS_MAINPAGE	R	4B	01001011	output
RESERVED	-	4C-4E		
INTERNAL_FREQ_FINE	R	4F	01001111	output
FUNCTIONS_ENABLE	R/W	50	01010000	00000000
RESERVED	-	51-53		
INACTIVITY_DUR	R/W	54	01010100	00000100
INACTIVITY_THS	R/W	55	01010101	00000000
TAP_CFG0	R/W	56	01010110	00000000
TAP_CFG1	R/W	57	01010111	00000000
TAP_CFG2	R/W	58	01011000	00000000

Name	Type	Register address		Default
		Hex	Binary	
TAP_THS_6D	R/W	59	01011001	00000000
TAP_DUR	R/W	5A	01011010	00000000
WAKE_UP_THS	R/W	5B	01011011	00000000
WAKE_UP_DUR	RW	5C	01011100	00000000
FREE_FALL	R/W	5D	01011101	00000000
MD1_CFG	R/W	5E	01011110	00000000
MD2_CFG	R/W	5F	01011111	00000000
RESERVED	-	60-62		
EMB_FUNC_CFG	R/W	63	01100011	00000000
RESERVED	-	64-6B		
TDM_CFG0	R/W	6C	01101100	10000000
TDM_CFG1	R/W	6D	01101101	11100000
TDM_CFG2	R/W	6E	01101110	00000001
RESERVED	-	6F-72		
Z_OFS_USR	R/W	73	01110011	00000000
Y_OFS_USR	R/W	74	01110100	00000000
X_OFS_USR	R/W	75	01110101	00000000
RESERVED	-	76-77		
FIFO_DATA_OUT_TAG	R	78	01111000	output
FIFO_DATA_OUT_BYTE_0	R	79	01111001	output
FIFO_DATA_OUT_BYTE_1	R	7A	01111010	output
FIFO_DATA_OUT_BYTE_2	R	7B	01111011	output
FIFO_DATA_OUT_BYTE_3	R	7C	01111100	output
FIFO_DATA_OUT_BYTE_4	R	7D	01111101	output
FIFO_DATA_OUT_BYTE_5	R	7E	01111110	output

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.
The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate, temperature and Qvar data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

9.1 FUNC_CFG_ACCESS (01h)

Enable embedded functions register (R/W)

Table 24. FUNC_CFG_ACCESS register

EMB_FUNC_ REG_ACCESS	0(1)	0(1)	0(1)	FSM_WR_ CTRL_EN	SW_POR	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 25. FUNC_CFG_ACCESS register description

EMB_FUNC_REG_ACCESS	Enables access to the embedded functions configuration registers. (1) Default value: 0
FSM_WR_CTRL_EN	Enables the control of the CTRL registers to FSM (FSM can change some configurations of the device autonomously). Default value: 0 (0: disabled; 1: enabled)
SW_POR	Global reset of the device. Default value: 0

1. *Details concerning the embedded functions configuration registers are available in Section 10 Embedded functions register mapping and Section 11 Embedded functions register description.*

9.2 PIN_CTRL (02h)

WCLK and SDO pin pull-up register (R/W). This register is not reset during the software reset procedure (see bit 0 of the CTRL3 (12h) register).

Table 26. PIN_CTRL register

TDM_WCLK _PU_DIS	SDO_ PU_EN	IBHR_ POR_EN	0(1)	0(1)	0(1)	1(2)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 27. PIN_CTRL register description

TDM_WCLK_PU_DIS	Disables pull-up on WCLK pin. Default value: 0 (0: WCLK pin with pull-up; 1: WCLK pin pull-up disconnected)
SDO_PU_EN	Enables pull-up on SDO pin. Default value: 0 (0: SDO pin pull-up disconnected; 1: SDO pin with pull-up)
IBHR_POR_EN	Selects the action the device performs after "reset whole chip" I3C pattern. Default value: 1 (0: Configuration reset (SW reset + dynamic address reset); (1: Global reset (POR reset))

9.3 IF_CFG (03h)

Interface configuration register (R/W). This register is not reset during the software reset procedure (see bit 0 of the CTRL3 (12h) register).

Table 28. IF_CFG register

SDA_PU_EN	TDM_OUT_PU_EN	ASF_CTRL	H_LACTIVE	PP_OD	SIM	0(1)	I2C_I3C_disable

1. *This bit must be set to 0 for the correct operation of the device.*

Table 29. IF_CFG register description

SDA_PU_EN	Enables pull-up on SDA pin. Default value: 0 (0: SDA pin pull-up disconnected; 1: SDA pin with pull-up)
TDM_OUT_PU_EN	Enables pull-up on TDMout pin. Default value: 0 (0: TDMout pin pull-up disconnected; 1: TDMout pin with pull-up)
ASF_CTRL	Enables anti-spike filters. Default value: 0 (0: anti-spike filters are managed by the protocol and turned off after the broadcast address; 1: anti-spike filters on SCL and SDA lines are always enabled)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low)
PP_OD	Push-pull/open-drain selection on INT1 and INT2 pins. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
I2C_I3C_disable	Disables I²C and MIPI I3C® interfaces. Default value: 0 (0: SPI, I²C, and MIPI I3C® interfaces enabled; 1: I²C and MIPI I3C® interfaces disabled)

9.4 FIFO_CTRL1 (07h)

FIFO control register 1 (R/W)

Table 30. FIFO_CTRL1 register

WTM_7	WTM_6	WTM_5	WTM_4	WTM_3	WTM_2	WTM_1	WTM_0

Table 31. FIFO_CTRL1 register description

WTM_[7:0]	FIFO watermark threshold: 1 LSB = TAG (1 byte) + 1 sensor (6 bytes) written in FIFO. Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level.

9.5 FIFO_CTRL2 (08h)

FIFO control register 2 (R/W)

Table 32. FIFO_CTRL2 register

STOP_ON_WTM	FIFO_COMPR_RT_EN	0(1)	ODR_CHG_EN	0(1)	UNCOMPR_RATE_1	UNCOMPR_RATE_0	XL_DualC_BATCH_FROM_FSM

1. *This bit must be set to 0 for the correct operation of the device.*

Table 33. FIFO_CTRL2 register description

STOP_ON_WTM	Sensing chain FIFO stop values memorization at threshold level. Default value: 0 (0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level, defined in FIFO_CTRL1 (07h))
FIFO_COMPR_RT_EN(1)	Enables/disables compression algorithm runtime. Default value: 0 (0: FIFO compression algorithm disabled; 1: FIFO compression algorithm enabled)
ODR_CHG_EN	Enables ODR CHANGE virtual sensor to be batched in FIFO. Default value: 0 (0: ODR CHANGE virtual sensor not batched in FIFO; 1: ODR CHANGE virtual sensor batched in FIFO)
UNCOMPR_RATE_[1:0]	This field configures the compression algorithm to write uncompressed data at each rate. (0: uncompressed data writing is not forced (default); 1: uncompressed data every 8 batch data rate; 2: uncompressed data every 16 batch data rate; 3: uncompressed data every 32 batch data rate)
XL_DualC_BATCH_FROM_FSM	When dual-channel mode is enabled, this bit enables FSM-triggered batching in FIFO of accelerometer channel 2. Default value: 0 (0: disabled; 1: enabled)

1. *This bit is active when the FIFO_COMPR_EN bit of EMB_FUNC_EN_B (05h) is set to 1.*

9.6 FIFO_CTRL3 (09h)

FIFO control register 3 (R/W)

Table 34. FIFO_CTRL3 register

BDR_GY_3	BDR_GY_2	BDR_GY_1	BDR_GY_0	BDR_XL_3	BDR_XL_2	BDR_XL_1	BDR_XL_0

Table 35. FIFO_CTRL3 register description

BDR_GY_[3:0]	Selects batch data rate (write frequency in FIFO) for gyroscope data. (0000: gyroscope not batched in FIFO (default); 0001: 1.875 Hz; 0010: 7.5 Hz; 0011: 15 Hz; 0100: 30 Hz; 0101: 60 Hz; 0110: 120 Hz; 0111: 240 Hz; 1000: 480 Hz; 1001: 960 Hz; 1010: 1.92 kHz; 1011: 3.84 kHz; 1100: 7.68 kHz 1101-1111: reserved)
BDR_XL_[3:0]	Selects batch data rate (write frequency in FIFO) for accelerometer data. (0000: accelerometer not batched in FIFO (default); 0001: 1.875 Hz; 0010: 7.5 Hz; 0011: 15 Hz; 0100: 30 Hz; 0101: 60 Hz; 0110: 120 Hz; 0111: 240 Hz; 1000: 480 Hz; 1001: 960 Hz; 1010: 1.92 kHz; 1011: 3.84 kHz; 1100: 7.68 kHz 1101-1111: reserved)

9.7 FIFO_CTRL4 (0Ah)

FIFO control register 4 (R/W)

Table 36. FIFO_CTRL4 register

DEC_TS_ BATCH_1	DEC_TS_ BATCH_0	ODR_T_ BATCH_1	ODR_T_ BATCH_0	0(1)	FIFO_ MODE_2	FIFO_ MODE_1	FIFO_ MODE_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 37. FIFO_CTRL4 register description

DEC_TS_BATCH_[1:0]	Selects decimation for timestamp batching in FIFO. Write rate is the maximum rate between the accelerometer and gyroscope BDR divided by decimation decoder. (00: Timestamp not batched in FIFO (default); 01: decimation 1: max(BDR_XL[Hz],BDR_GY[Hz]) [Hz]; 10: decimation 8: max(BDR_XL[Hz],BDR_GY[Hz])/8 [Hz]; 11: decimation 32: max(BDR_XL[Hz],BDR_GY[Hz])/32 [Hz])
ODR_T_BATCH_[1:0]	Selects batch data rate (write frequency in FIFO) for temperature data (00: temperature not batched in FIFO (default); 01: 1.875 Hz; 10: 15 Hz; 11: 60 Hz)
FIFO_MODE_[2:0]	FIFO mode selection (000: bypass mode: FIFO disabled (default); 001: FIFO mode: stops collecting data when FIFO is full; 010: continuousWTM-to-full mode: continuous mode with FIFO watermark size until trigger is deasserted, then data are stored in FIFO until the buffer is full; 011: continuous-to-FIFO mode: continuous mode until trigger is 011: continuous-to-FIFO mode: continuous mode until trigger is deasserted, then FIFO mode; 100: bypass-to-continuous mode: bypass mode until trigger is deasserted, then continuous mode; 101: reserved; 110: continuous mode: if the FIFO is full, the new sample overwrites the older one; 111: bypass-to-FIFO mode: bypass mode until trigger is deasserted, then FIFO mode.)

9.8 COUNTER_BDR_REG1 (0Bh)

Counter batch data rate register 1 (R/W)

Table 38. COUNTER_BDR_REG1 register

0(1)	TRIG_COUNTER_BDR_1	TRIG_COUNTER_BDR_0	0(1)	0(1)	AH_QVAR_BATCH_EN	CNT_BDR_TH_9	CNT_BDR_TH_8

1. *This bit must be set to 0 for the correct operation of the device.*

Table 39. COUNTER_BDR_REG1 register description

TRIG_COUNTER_BDR_[1:0]	Selects the trigger for the internal counter of batch events between the accelerometer and gyroscope. (00: accelerometer batch event; 01: gyroscope batch event; 10 – 11: reserved)
AH_QVAR_BATCH_EN	Enables analog hub / Qvar batching in FIFO. Default value: 0 (0: disabled; 1: enabled)
CNT_BDR_TH_[9:8]	In conjunction with CNT_BDR_TH_[7:0] in COUNTER_BDR_REG2 (0Ch), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (1Ch) is set to 1.

9.9 COUNTER_BDR_REG2 (0Ch)

Counter batch data rate register 2 (R/W)

Table 40. COUNTER_BDR_REG2 register

CNT_BDR_TH_7	CNT_BDR_TH_6	CNT_BDR_TH_5	CNT_BDR_TH_4	CNT_BDR_TH_3	CNT_BDR_TH_2	CNT_BDR_TH_1	CNT_BDR_TH_0

Table 41. COUNTER_BDR_REG2 register description

CNT_BDR_TH_[7:0]	In conjunction with CNT_BDR_TH_[9:8] in COUNTER_BDR_REG1 (0Bh), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (1Ch) is set to 1.

9.10 INT1_CTRL (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1 when the MIPI I3C® dynamic address is not assigned (I²C or SPI is used). Some bits can be also used to trigger an IBI (in-band interrupt) when the MIPI I3C® interface is used. The output of the pin is the OR combination of the signals selected here and in MD1_CFG (5Eh).

Table 42. INT1_CTRL register

0(1)	INT_1 CNT_BDR	INT1_ FIFO_FULL	INT1_ FIFO_OVR	INT1_ FIFO_TH	0(1)	INT1_ DRDY_G	INT1_ DRDY_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 43. INT1_CTRL register description

INT1_CNT_BDR	Enables COUNTER_BDR_IA interrupt on INT1 pin. Default value: 0
INT1_FIFO_FULL	Enables FIFO full flag interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0
INT1_FIFO_OVR	Enables FIFO overrun interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0
INT1_FIFO_TH	Enables FIFO threshold interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0
INT1_DRDY_G	Enables gyroscope data-ready interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0
INT1_DRDY_XL	Enables accelerometer data-ready interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0

9.11 INT2_CTRL (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2 when the MIPI I3C® dynamic address is not assigned (I²C or SPI is used). Some bits can be also used to trigger an IBI when the MIPI I3C® interface is used. The output of the pin is the OR combination of the signals selected here and in MD2_CFG (5Fh).

Table 44. INT2_CTRL register

INT2_EMB_FUNC_ENDOP	INT2_CNT_BDR	INT2_FIFO_FULL	INT2_FIFO_OVR	INT2_FIFO_TH	0(1)	INT2_DRDY_G	INT2_DRDY_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 45. INT2_CTRL register description

INT2_EMB_FUNC_ENDOP	Enables routing the embedded functions end of operations signal to the INT2 pin. Default value: 0
INT2_CNT_BDR	Enables COUNTER_BDR_IA interrupt on INT2. Default value: 0
INT2_FIFO_FULL	Enables FIFO full flag interrupt on INT2 pin.Default value: 0
INT2_FIFO_OVR	Enables FIFO overrun interrupt on INT2 pin. Default value: 0
INT2_FIFO_TH	Enables FIFO threshold interrupt on INT2 pin. Default value: 0
INT2_DRDY_G	Gyroscope data-ready interrupt on INT2 pin. Default value: 0
INT2_DRDY_XL	Accelerometer data-ready interrupt on INT2 pin. Default value: 0

9.12 WHO_AM_I (0Fh)

WHO_AM_I register (R). This is a read-only register. Its value is fixed at 71h.

Table 46. WhoAmI register

0	1	1	1	0	0	0	1

9.13 CTRL1 (10h)

Accelerometer control register 1 (R/W)

Table 47. CTRL1 register

0(1)	OP_MODE_XL_2	OP_MODE_XL_1	OP_MODE_XL_0	ODR_XL_3	ODR_XL_2	ODR_XL_1	ODR_XL_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 48. CTRL1 register description

OP_MODE_XL_[2:0]	Accelerometer operating mode selection. (000: high-performance mode (default); 001: reserved; 010: high-performance mode + TDM; 011: reserved; 100: low-power mode 1 (2 mean); 101: low-power mode 2 (4 mean); 110: low-power mode 3 (8 mean); 111: reserved)
ODR_XL_[3:0]	Accelerometer ODR selection (see Table 49)

Table 49. Accelerometer ODR selection

ODR_XL_3	ODR_XL_2	ODR_XL_1	ODR_XL_0	ODR selection [Hz]
0	0	0	0	Power-down (default)
0	0	0	1	1.875 Hz (low-power mode)
0	0	1	0	7.5 Hz (high-performance mode)
0	0	1	1	15 Hz (low-power, high-performance mode)
0	1	0	0	30 Hz (low-power, high-performance mode)
0	1	0	1	60 Hz (low-power, high-performance mode)
0	1	1	0	120 Hz (low-power, high-performance mode)
0	1	1	1	240 Hz (low-power, high-performance mode)
1	0	0	0	480 Hz (high-performance mode)
1	0	0	1	960 Hz (high-performance mode)
1	0	1	0	1.92 kHz (high-performance mode)
1	0	1	1	3.84 kHz (high-performance mode)
1	1	0	0	7.68 kHz (high-performance mode)
Others				Reserved

9.14 CTRL2 (11h)

Gyroscope control register 2 (R/W)

Table 50. CTRL2 register

0(1)	OP_MODE_G_2	OP_MODE_G_1	OP_MODE_G_0	ODR_G_3	ODR_G_2	ODR_G_1	ODR_G_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 51. CTRL2 register description

OP_MODE_G_[2:0]	Gyroscope operating mode selection. (000: high-performance mode (default); 001: reserved; 010: reserved; 011: reserved; 100: sleep mode; 101: low-power mode; 110-111: reserved)
ODR_G_[3:0]	Gyroscope output data rate selection. (See Table 52)

Table 52. Gyroscope ODR selection

ODR_G_3	ODR_G_2	ODR_G_1	ODR_G_0	ODR [Hz]
0	0	0	0	Power-down (default)
0	0	1	0	7.5 Hz (low-power, high-performance mode)
0	0	1	1	15 Hz (low-power, high-performance mode)
0	1	0	0	30 Hz (low-power, high-performance mode)
0	1	0	1	60 Hz (low-power, high-performance mode)
0	1	1	0	120 Hz (low-power, high-performance mode)
0	1	1	1	240 Hz (low-power, high-performance mode)
1	0	0	0	480 Hz (high-performance mode)
1	0	0	1	960 Hz (high-performance mode)
1	0	1	0	1.92 kHz (high-performance mode)
1	0	1	1	3.84 kHz (high-performance mode)
1	1	0	0	7.68 kHz (high-performance mode)
Others				Reserved

9.15 CTRL3 (12h)

Control register 3 (R/W)

Table 53. CTRL3 register

BOOT	BDU	0(1)	0(1)	0(1)	IF_INC	0(1)	SW_RESET

1. *This bit must be set to 0 for the correct operation of the device.*

Table 54. CTRL3 register description

BOOT	Reboots memory content (the accelerometer must not be in power-down mode). This bit is automatically cleared. Default value: 0 (0: normal mode; 1: reboot memory content) This bit is automatically cleared.
BDU	Block data update. Default value: 1 (0: continuous update; 1: output registers are not updated until LSB and MSB have been read)
IF_INC	Register address automatically incremented during a multiple byte access with a serial interface (I²C, MIPI I3C, or SPI). Default value: 1 (0: disabled; 1: enabled)
SW_RESET	Software reset, resets all control registers to their default value. This bit is automatically cleared. Default value: 0 (0: normal mode; 1: reset device)

9.16 CTRL4 (13h)

Control register 4 (R/W)

Table 55. CTRL4 register

0(1)	0(1)	0(1)	INT2_on_INT1	DRDY_MASK	INT2_DRDY_TEMP	DRDY_PULSED	INT2_IN_LH

1. *This bit must be set to 0 for the correct operation of the device.*

Table 56. CTRL4 register description

INT2_on_INT1	Enables routing the embedded functions interrupt signals to the INT1 pin. Default value: 0 • The corresponding bits in the INT2 control registers need to be enabled. • These interrupts are in OR with those enabled on the INT1 pin. • They are not fed to the INT2 pin. • The movable interrupts are: – INT2_EMB_FUNC_ENDOP enabled through INT2_CTRL (0Eh) – INT2_TIMESTAMP enabled through MD2_CFG (5Fh) – INT2_DRDY_TEMP enabled through CTRL4 (13h) – INT2_DRDY_AH_QVAR enabled through CTRL7 (16h)
DRDY_MASK	Enables / masks data-ready signal. Default value: 0 (0: disabled; 1: masks DRDY on pin (both accelerometer and gyroscope) until filter settling ends (accelerometer and gyroscope independently masked))
INT2_DRDY_TEMP	Enables temperature sensor data-ready interrupt on the INT2 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used and INT2_ON_INT1 = 1 in CTRL4_C (13h). Default value: 0 (0: disabled; 1: enabled)
DRDY_PULSED	Enables pulsed data-ready mode. Default value: 0 (0: data-ready latched mode (returns to 0 only after the higher part of the associated output register has been read); 1: data-ready pulsed mode (the data-ready pulses are 75 µs long))
INT2_IN_LH	Set to 1 in order to change the polarity of the INT2 pin input trigger for embedded functions. Default value: 0 (0: trigger for embedded functions pin is active low; 1: trigger for embedded functions pin is active high)

9.17 CTRL5 (14h)

Control register 5 (R/W)

Table 57. CTRL5 register

0(1)	0(1)	0(1)	0(1)	0(1)	BUS_ACT_SEL_1	BUS_ACT_SEL_0	INT_EN_I3C

1. *This bit must be set to 0 for the correct operation of the device.*

Table 58. CTRL5 register description

BUS_ACT_SEL_[1:0]	Bus available time selection for IBI (in-band interrupt): 00: 2 µs; 01: 50 µs (default); 10: 1 ms; 11: 25 ms)
INT_EN_I3C	Enables INT pin when I3C is enabled. Default value: 0 (0: disabled; 1: enabled)

9.18 CTRL6 (15h)

Control register 6 (R/W)

Table 59. CTRL6 register

LPF1_G_BW_3	LPF1_G_BW_2	LPF1_G_BW_1	LPF1_G_BW_0	FS_G_3	FS_G_2	FS_G_1	FS_G_0

Table 60. CTRL6 register description

LPF1_G_BW_[3:0]	Gyroscope low-pass filter (LPF1) bandwidth selection Table 61 shows the selectable bandwidth values.
FS_G_[3:0]	Gyroscope UI chain full-scale selection: (0000: ±125 dps (default); 0001: ±250 dps; 0010: ±500 dps; 0011: ±1000 dps; 0100: ±2000 dps; 1100: ±4000 dps Others: reserved)

Table 61. **Gyroscope LPF1 bandwidth selection**

LPF1_G_BW_[3:0]	60 Hz	120 Hz	240 Hz	480 Hz	960 Hz	1.92 kHz	3.84 kHz	7.68 kHz
000	N.A.	N.A.	N.A.	174	353	273	280	282
001	N.A.	N.A.	N.A.	157	194	209	211	212
010	N.A.	N.A.	N.A.	131	148	154	156	156
011	N.A.	N.A.	N.A.	186	313	405	428	434
100	N.A.	N.A.	78	94	99	101	102	102
101	N.A.	43	53	57	58	58	58	58
110	18.0	24.2	27.3	28.4	28.7	28.8	N.A.	N.A.
111	12.1	13.7	14.2	14.3	14.4	14.4	N.A.	N.A.

9.19 CTRL7 (16h)

Control register 7 (R/W)

Table 62. **CTRL7 register**

AH_QVAR_EN	INT2_DRDY_AH_QVAR	AH_QVAR_C_ZIN_1	AH_QVAR_C_ZIN_0	AH_QVAR1_EN	AH_QVAR2_EN	0(1)	LPF1_G_EN

1. *This bit must be set to 0 for the correct operation of the device.*

Table 63. **CTRL7 register description**

AH_QVAR_EN	Enables the analog hub and Qvar chain. When this bit is set to 1, the analog hub Qvar buffers are connected to the AH/QVAR1 and AH/QVAR2 pins. Before setting this bit to 1, the accelerometer and gyroscope sensors have to be configured in power-down mode. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_AH_QVAR	Analog hub and Qvar data-ready interrupt on the INT2 pin. Default value: 0 (0: disabled; 1: enabled)
AH_QVAR_C_ZIN_[1:0]	Configures the equivalent input impedance of the analog hub and Qvar buffers. (00: 2.4 GΩ (default); 01: 730 MΩ; 10: 300 MΩ; 11: 235 MΩ)
AH_QVAR1_EN	Enables the AH1/QVAR1 pin. Default value: 0 (0: disabled; 1: enabled)
AH_QVAR2_EN	Enables the AH2/QVAR2 pin. Default value: 0 (0: disabled; 1: enabled)
LPF1_G_EN	Enables the gyroscope digital LPF1 filter

9.20 CTRL8 (17h)

Control register 8 (R/W)

Table 64. CTRL8 register

HP_LPF2_ XL_BW_2	HP_LPF2_ XL_BW_1	HP_LPF2_ XL_BW_0	AH_QVAR _HPF	XL_DualC_EN	0(1)	FS_XL_1	FS_XL_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 65. CTRL8 register description

HP_LPF2_XL_BW_[2:0]	Accelerometer LPF2 and HP filter configuration and cutoff setting. Refer to Table 66.
AH_QVAR_HPF	Enables the analog hub / Qvar high-pass filter (refer to Table 20 in Section 6.6 Qvar functionality). Default value: 0 (0: disabled; 1: enabled)
XL_DualC_EN	Enables dual-channel mode. When this bit is set to 1, data with the maximum full scale are sent to the output registers at addresses 34h to 39h. The UI processing chain is used. Default value: 0 (0: disabled; 1: enabled)
FS_XL_[1:0]	Accelerometer full-scale selection: (00: ±2 *g*; 01: ±4 *g*; 10: ±8 *g*; 11: ±16 *g*)

Table 66. Accelerometer bandwidth configurations

Filter type	HP_SLOPE_ XL_EN	LPF2_XL_EN	HP_LPF2_XL_BW_[2:0]	Bandwidth
Low pass	0	0	-	ODR/2(1)
		1	000	ODR/4
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800
High pass	1	-	000	SLOPE (ODR/4)
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800

1. *This value is ODR/2 when the accelerometer is in high-performance mode. It is equal to 3100 Hz when the accelerometer is in low-power mode 1 (2 mean), 912 Hz in low-power mode 2 (4 mean) and 431 Hz in low-power mode 3 (8 mean).*

9.21 CTRL9 (18h)

Control register 9 (R/W)

Table 67. CTRL9 register

AH_QVAR _LPF	HP_REF_ MODE_XL	XL_FASTSET TL_MODE	HP_SLOPE_ XL_EN	LPF2_XL_EN	0(1)	USR_OFF_W	USR_OFF_ ON_OUT

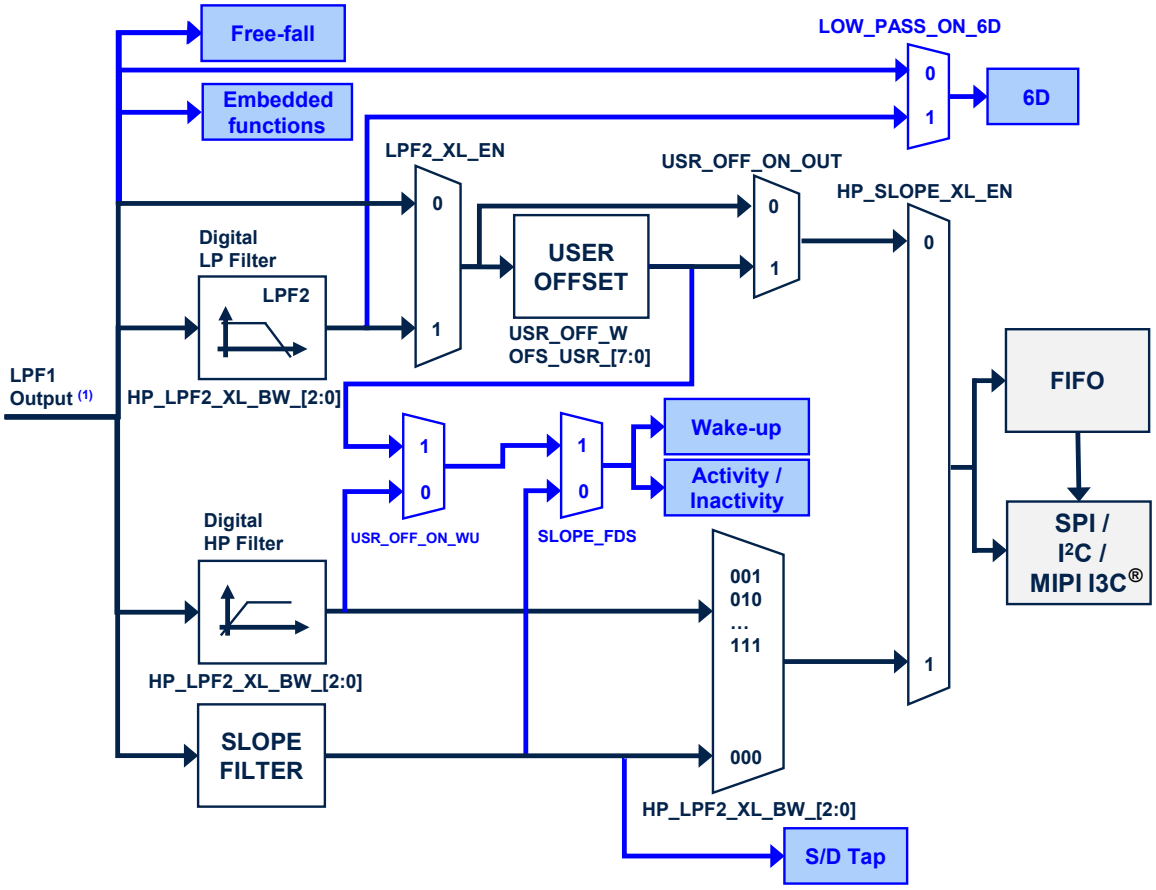
1. *This bit must be set to 0 for the correct operation of the device.*

Table 68. CTRL9 register description

AH_QVAR_LPF	Enables the analog hub / Qvar notch filter (refer to Table 20 in Section 6.6 Qvar functionality). The ODR is switched to 120 Hz. Default value: 0 (0: disabled; 1: enabled)
HP_REF_MODE_XL	Enables accelerometer high-pass filter reference mode (valid for high-pass path - HP_SLOPE_XL_EN bit must be 1). Default value: 0 (0: disabled, 1: enabled)(1)
XL_FASTSETTL_MODE	Enables accelerometer LPF2 and HPF fast-settling mode. The filter sets the first sample after writing this bit. Active only during device exit from power-down mode. Default value: 0 (0: disabled, 1: enabled)
HP_SLOPE_XL_EN	Accelerometer slope filter / high-pass filter selection. Refer to Figure 30. Default value: 0 (0: low-pass filter path selected; 1: high-pass filter path selected)
LPF2_XL_EN	Accelerometer high-resolution selection. Refer to Figure 30. Default value: 0 (0: output from first stage digital filtering selected; 1: output from LPF2 second filtering stage selected)
USR_OFF_W	Weight of XL user offset bits of registers Z_OFS_USR (73h), Y_OFS_USR (74h), X_OFS_USR (75h). Default value: 0 (0: 2^{-10} *g*/LSB; 1: 2^{-6} *g*/LSB)
USR_OFF_ON_OUT	Enables the accelerometer user offset correction block; it is valid for the low-pass path. Refer to Figure 30. Default value: 0 (0: accelerometer user offset correction block bypassed; 1: accelerometer user offset correction block enabled)

1. *When enabled, the first output data has to be discarded.*

Figure 30. **Accelerometer block diagram**



1. *The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode. This value is equal to 3100 Hz when the accelerometer is in low-power mode 1 (2 mean), 912 Hz in low-power mode 2 (4 mean) or 431 Hz in low-power mode 3 (8 mean).*

9.22 CTRL10 (19h)

Control register 10 (R/W)

Table 69. CTRL10 register

0(1)	EMB_FUNC_DEBUG	AH_QVAR_SW	XL_ST_OFFSET	ST_G_1	ST_G_0	ST_XL_1	ST_XL_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 70. CTRL10 register description

EMB_FUNC_DEBUG	Enables debug mode for the embedded functions. (0: disabled; 1: enabled)
AH_QVAR_SW	Swaps the input electrodes of Qvar. Default value: 0 (0: swap disabled; 1: swap enabled)
XL_ST_OFFSET	To be used during the accelerometer self-test procedure. When this bit is set to 1, only the offset is measured; when set to 0, the offset plus the self-test signal is measured. The final self-test output is obtained by the difference between the outputs with XL_ST_OFFSET 1 and 0.
ST_G_[1:0]	Gyroscope self-test selection (00: normal mode (default); 01: positive sign self-test; 10: negative sign self-test; 11: reserved)
ST_XL_[1:0]	Accelerometer self-test selection (00: normal mode (default); 01: positive sign self-test; 10: negative sign self-test; 11: reserved)

9.23 CTRL_STATUS (1Ah)

(R)

Table 71. CTRL_STATUS register

0	0	0	0	0	FSM_WR_CTRL_STATUS	-	0

Table 72. CTRL_STATUS register description

FSM_WR_CTRL_STATUS	This flag indicates the current controller of the device configuration registers. This flag must be used as an acknowledge flag when the value of the FSM_WR_CTRL_EN bit in the FUNC_CFG_ACCESS (01h) register is changed. Default value: 0 (0: all registers and configurations are writable from the standard interface; 1: some registers and configurations are under FSM control and are in read-only mode from the standard interface).

9.24 FIFO_STATUS1 (1Bh)

FIFO status register 1 (R)

Table 73. FIFO_STATUS1 register

DIFF_ FIFO_7	DIFF_ FIFO_6	DIFF_ FIFO_5	DIFF_ FIFO_4	DIFF_ FIFO_3	DIFF_ FIFO_2	DIFF_ FIFO_1	DIFF_ FIFO_0

Table 74. FIFO_STATUS1 register description

DIFF_FIFO_[7:0]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO In conjunction with DIFF_FIFO_8 in FIFO_STATUS2 (1Ch).

9.25 FIFO_STATUS2 (1Ch)

FIFO status register 2 (R)

Table 75. FIFO_STATUS2 register

FIFO_ WTM_IA	FIFO_ OVR_IA	FIFO_ FULL_IA	COUNTER_ BDR_IA	FIFO_OVR_ LATCHED	0	0	DIFF_ FIFO_8

Table 76. FIFO_STATUS2 register description

FIFO_WTM_IA	FIFO watermark status. Default value: 0 (0: FIFO filling is lower than WTM; 1: FIFO filling is equal to or greater than WTM) Watermark is set through bits WTM[7:0] in FIFO_CTRL1 (07h).
FIFO_OVR_IA	FIFO overrun status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled)
FIFO_FULL_IA	Smart FIFO full status. Default value: 0 (0: FIFO is not full; 1: FIFO will be full at the next ODR)
COUNTER_BDR_IA	Counter BDR reaches the CNT_BDR_TH_[10:0] threshold set in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch). Default value: 0 This bit is reset when these registers are read.
FIFO_OVR_LATCHED	Latched FIFO overrun status. Default value: 0 This bit is reset when this register is read.
DIFF_FIFO_8	Number of unread sensor data (TAG + 6 bytes) stored in FIFO. Default value: 00 In conjunction with DIFF_FIFO[7:0] in FIFO_STATUS1 (1Bh)

9.26 ALL_INT_SRC (1Dh)

Source register for all interrupts (R)

Table 77. ALL_INT_SRC register

EMB_ FUNC_IA	0	SLEEP_ CHANGE_IA	D6D_IA	0	TAP_IA	WU_IA	FF_IA

Table 78. ALL_INT_SRC register description

EMB_FUNC_IA	Embedded functions interrupt status. Default value: 0 (0: embedded functions event not detected; 1: embedded functions event detected)
SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
D6D_IA	Interrupt active for change in position of portrait, landscape, face-up, face-down. Default value: 0 (0: change in position not detected; 1: change in position detected)
TAP_IA	Single or double-tap event detection status depending on SINGLE_DOUBLE_TAP_bit value (see WAKE_UP_THS (5Bh) register). Default value: 0 (0: tap event not detected; 1: tap event detected)
WU_IA	Wake-up event status. Default value: 0 (0: event not detected, 1: event detected)
FF_IA	Free-fall event status. Default value: 0 (0: event not detected, 1: event detected)

9.27 STATUS_REG (1Eh)

The STATUS_REG register is read by the primary interface SPI/I²C & MIPI I3C® (R).

Table 79. STATUS_REG register

TIMESTAMP_ ENDCOUNT	0	0	0	AH_QVARDA	TDA	GDA	XLDA

Table 80. STATUS_REG register description

TIMESTAMP_ENDCOUNT	Alerts timestamp overflow within 5.6 ms
AH_QVARDA	Analog hub or Qvar new data available. Default value: 0 (0: no set of data available at the analog hub or Qvar output; 1: a new set of data is available at the analog hub or Qvar output)
TDA	Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output)
GDA	Gyroscope new data available. Default value: 0 (0: no set of data available at gyroscope output; 1: a new set of data is available at gyroscope output)
XLDA	Accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output)

9.28 OUT_TEMP_L (20h), OUT_TEMP_H (21h)

Temperature data output register (R). L and H registers together express a 16-bit word in two's complement.

Table 81. OUT_TEMP_L register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 82. OUT_TEMP_H register

Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8

Table 83. OUT_TEMP register description

Temp[15:0]	Temperature sensor output data The value is expressed in two's complement.

9.29 OUTX_L_G (22h) and OUTX_H_G (23h)

Angular rate sensor pitch axis (X) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL6 (15h)) and ODR settings (CTRL2 (11h)) of the gyroscope user interface.

Table 84. OUTX_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 85. OUTX_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 86. OUTX_G register description

D[15:0]	Gyroscope UI chain pitch axis (X) angular rate output value

9.30 OUTY_L_G (24h) and OUTY_H_G (25h)

Angular rate sensor roll axis (Y) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL6 (15h)) and ODR settings (CTRL2 (11h)) of the gyroscope user interface.

Table 87. OUTY_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 88. OUTY_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 89. OUTY_G register description

D[15:0]	Gyroscope UI chain roll axis (Y) angular rate output value

9.31 OUTZ_L_G (26h) and OUTZ_H_G (27h)

Angular rate sensor yaw axis (Z) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL6 (15h)) and ODR settings (CTRL2 (11h)) of the gyroscope user interface.

Table 90. OUTZ_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 91. OUTZ_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 92. OUTZ_H_G register description

D[15:0]	Gyroscope UI chain yaw axis (Z) angular rate output value

9.32 OUTZ_L_A (28h) and OUTZ_H_A (29h)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL8 (17h)) and ODR settings (CTRL1 (10h)) of the accelerometer user interface.

Table 93. OUTZ_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 94. OUTZ_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 95. OUTZ_A register description

D[15:0]	Accelerometer UI chain Z-axis linear acceleration output value

9.33 OUTY_L_A (2Ah) and OUTY_H_A (2Bh)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL8 (17h)) and ODR settings (CTRL1 (10h)) of the accelerometer user interface.

Table 96. OUTY_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 97. OUTY_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 98. OUTY_A register description

D[15:0]	Accelerometer UI chain Y-axis linear acceleration output value

9.34 OUTX_L_A (2Ch) and OUTX_H_A (2Dh)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL8 (17h)) and ODR settings (CTRL1 (10h)) of the accelerometer user interface.

Table 99. OUTX_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 100. OUTX_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 101. OUTX_A register description

D[15:0]	Accelerometer UI chain X-axis linear acceleration output value

9.35 UI_OUTZ_L_A_DualC (34h) and UI_OUTZ_H_A_DualC (35h)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the accelerometer full-scale and ODR settings of the accelerometer dual-channel mode configuration.

Table 102. UI_OUTZ_L_A_DualC register

D7	D6	D5	D4	D3	D2	D1	D0

Table 103. UI_OUTZ_H_A_DualC register

D15	D14	D13	D12	D11	D10	D9	D8

Table 104. UI_OUTZ_A_DualC register description

D[15:0]	Accelerometer Z-axis DualC output expressed in two's complement

9.36 UI_OUTY_L_A_DualC (36h) and UI_OUTY_H_A_DualC (37h)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the accelerometer full-scale and ODR settings of the accelerometer dual-channel mode configuration.

Table 105. UI_OUTY_L_A_DualC register

D7	D6	D5	D4	D3	D2	D1	D0

Table 106. UI_OUTY_H_A_DualC register

D15	D14	D13	D12	D11	D10	D9	D8

Table 107. UI_OUTY_A_DualC register description

D[15:0]	Accelerometer Y-axis DualC output expressed in two's complement

9.37 UI_OUTX_L_A_DualC (38h) and UI_OUTX_H_A_DualC (39h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the accelerometer full-scale and ODR settings of the accelerometer dual-channel mode configuration.

Table 108. UI_OUTX_L_A_DualC register

D7	D6	D5	D4	D3	D2	D1	D0

Table 109. UI_OUTX_H_A_DualC register

D15	D14	D13	D12	D11	D10	D9	D8

Table 110. UI_OUTX_A_DualC register description

D[15:0]	Accelerometer X-axis DualC output expressed in two's complement

9.38 AH_QVAR_OUT_L (3Ah) and AH_QVAR_OUT_H (3Bh)

Analog hub and Qvar data output register (R). L and H registers together express a 16-bit word in two's complement.

Table 111. AH_QVAR_OUT_L register

AH_Qvar_7	AH_Qvar_6	AH_Qvar_5	AH_Qvar_4	AH_Qvar_3	AH_Qvar_2	AH_Qvar_1	AH_Qvar_0

Table 112. AH_QVAR_OUT_H register

AH_Qvar_15	AH_Qvar_14	AH_Qvar_13	AH_Qvar_12	AH_Qvar_11	AH_Qvar_10	AH_Qvar_9	AH_Qvar_8

Table 113. AH_QVAR_OUT register description

AH_Qvar_[15:0]	When the analog hub or Qvar is enabled (by setting the AH_QVAR_EN bit to 1 in CTRL7 (16h)), these registers contain the analog hub or Qvar sensor ouput data. Data are expressed in two's complement.

9.39 TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)

Timestamp first data output register (R). The value is expressed as a 32-bit word and the bit resolution is 21.75 µs (typical).

Table 114. TIMESTAMP output registers

D31	D30	D29	D28	D27	D26	D25	D24
D23	D22	D21	D20	D19	D18	D17	D16
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 115. TIMESTAMP output register description

D[31:0]	Timestamp output registers: 1LSB = 21.75 µs (typical)

9.40 WAKE_UP_SRC (45h)

Wake-up interrupt source register (R)

Table 116. WAKE_UP_SRC register

0	SLEEP_ CHANGE_IA	FF_IA	SLEEP_ STATE	WU_IA	Z_WU	Y_WU	X_WU

Table 117. WAKE_UP_SRC register description

SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
FF_IA	Free-fall event detection status. Default: 0 (0: free-fall event not detected; 1: free-fall event detected)
SLEEP_STATE	Sleep status bit. Default value: 0 (0: Activity status; 1: Inactivity status)
WU_IA	Wake-up event detection status. Default value: 0 (0: wake-up event not detected; 1: wake-up event detected.)
Z_WU	Wake-up event detection status on Z-axis. Default value: 0 (0: wake-up event on Z-axis not detected; 1: wake-up event on Z-axis detected)
Y_WU	Wake-up event detection status on Y-axis. Default value: 0 (0: wake-up event on Y-axis not detected; 1: wake-up event on Y-axis detected)
X_WU	Wake-up event detection status on X-axis. Default value: 0 (0: wake-up event on X-axis not detected; 1: wake-up event on X-axis detected)

9.41 TAP_SRC (46h)

Tap source register (R)

Table 118. TAP_SRC register

TAP_IA	SINGLE_ TAP	DOUBLE_ TAP	0	TAP_SIGN	Z_TAP	Y_TAP	X_TAP

Table 119. TAP_SRC register description

TAP_IA	Tap event detection status. Default: 0 (0: tap event not detected; 1: tap event detected)
SINGLE_TAP	Single-tap event status. Default value: 0 (0: single tap event not detected; 1: single tap event detected)
DOUBLE_TAP	Double-tap event detection status. Default value: 0 (0: double-tap event not detected; 1: double-tap event detected.)
TAP_SIGN	Sign of acceleration detected by tap event. Default: 0 (0: positive sign of acceleration detected by tap event; 1: negative sign of acceleration detected by tap event)
Z_TAP	Tap event detection status on Z-axis. Default value: 0 (0: tap event on Z-axis not detected; 1: tap event on Z-axis detected)
Y_TAP	Tap event detection status on Y-axis. Default value: 0 (0: tap event on Y-axis not detected; 1: tap event on Y-axis detected)
X_TAP	Tap event detection status on X-axis. Default value: 0 (0: tap event on X-axis not detected; 1: tap event on X-axis detected)

9.42 D6D_SRC (47h)

Portrait, landscape, face-up, and face-down source register (R)

Table 120. D6D_SRC register

0	D6D_IA	XH	XL	YH	YL	ZH	ZL

Table 121. D6D_SRC register description

D6D_IA	Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0 (0: change position not detected; 1: change position detected)
XH	X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
XL	X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
YH	Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over-threshold) detected)
YL	Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
ZH	Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
ZL	Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)

9.43 EMB_FUNC_STATUS_MAINPAGE (49h)

Embedded function status register (R)

Table 122. EMB_FUNC_STATUS_MAINPAGE register

IS_FSM_LC	0	IS_ SIGMOT	IS_TILT	IS_ STEP_DET	0	0	0

Table 123. EMB_FUNC_STATUS_MAINPAGE register description

IS_FSM_LC	Interrupt status bit for FSM long counter timeout interrupt event. (1: interrupt detected; 0: no interrupt)
IS_SIGMOT	Interrupt status bit for significant motion detection (1: interrupt detected; 0: no interrupt)
IS_TILT	Interrupt status bit for tilt detection (1: interrupt detected; 0: no interrupt)
IS_STEP_DET	Interrupt status bit for step detection (1: interrupt detected; 0: no interrupt)

9.44 FSM_STATUS_MAINPAGE (4Ah)

Finite state machine status register (R)

Table 124. FSM_STATUS_MAINPAGE register

IS_FSM8	IS_FSM7	IS_FSM6	IS_FSM5	IS_FSM4	IS_FSM3	IS_FSM2	IS_FSM1

Table 125. FSM_STATUS_MAINPAGE register description

IS_FSM8	Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM7	Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM6	Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM5	Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM4	Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM3	Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM2	Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM1	Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt)

9.45 MLC_STATUS_MAINPAGE (4Bh)

Machine learning core status register (R)

Table 126. MLC_STATUS _MAINPAGE register

0	0	0	0	IS_MLC4	IS_MLC3	IS_MLC2	IS_MLC1

Table 127. MLC_STATUS_MAINPAGE register description

IS_MLC4	Interrupt status bit for MLC4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC3	Interrupt status bit for MLC3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC2	Interrupt status bit for MLC2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC1	Interrupt status bit for MLC1 interrupt event. (1: interrupt detected; 0: no interrupt)

9.46 INTERNAL_FREQ_FINE (4Fh)

Internal frequency register (R)

Table 128. INTERNAL_FREQ_FINE register

FREQ_ FINE_7	FREQ_ FINE_6	FREQ_ FINE_5	FREQ_ FINE_4	FREQ_ FINE_3	FREQ_ FINE_2	FREQ_ FINE_1	FREQ_ FINE_0

Table 129. INTERNAL_FREQ_FINE register description

FREQ_FINE_[7:0]	Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.13%. 8-bit format, two's complement.

The actual timestamp resolution and the actual output data rate can be calculated using the following formulas:

$$t_{actual}[s] = \frac{1}{46080 \cdot (1 + 0.0013 \cdot FREQ_FINE)}$$

$$ODR_{actual}[Hz] = \frac{7680 \cdot (1 + 0.0013 \cdot FREQ_FINE)}{ODR_{coeff}}$$

Table 130. ODRcoeff values

Selected ODR [Hz]	ODRcoeff
7.5	1024
15	512
30	256
60	128
120	64
240	32
480	16
960	8
1.92 kHz	4
3.84 kHz	2
7.68 kHz	1

9.47 FUNCTIONS_ENABLE (50h)

Enable interrupt functions register (R/W)

Table 131. FUNCTIONS_ENABLE register

INTERRUPTS_ENABLE	TIMESTAMP_EN	0(1)	0(1)	DIS_RST_LIR_ALL_INT	0(1)	INACT_EN_1	INACT_EN_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 132. FUNCTIONS_ENABLE register description

INTERRUPTS_ENABLE	Enables basic interrupts (6D, free-fall, wake-up, tap, activity/inactivity). Default value: 0 (0: interrupt disabled; 1: interrupt enabled)
TIMESTAMP_EN	Enables timestamp counter. The counter is readable in TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h). Default value: 0 (0: disabled; 1: enabled)
DIS_RST_LIR_ALL_INT	When this bit is set to 1, reading the ALL_INT_SRC (1Dh) register does not reset the latched interrupt signals. This can be useful in order to not reset some status flags before reading the corresponding status register. Default value: 0 (0: disabled; 1: enabled)
INACT_EN_[1:0]	Enables activity/inactivity (sleep) function. Default value: 00 (00: stationary/motion-only interrupts generated, accelerometer and gyroscope configuration do not change; 01: sets accelerometer to low-power mode 1 with accelerometer ODR selected through the XL_INACT_ODR_[1:0] bits of the INACTIVITY_DUR (54h) register, gyroscope configuration does not change; 10: sets accelerometer to low-power mode 1 with accelerometer ODR selected through the XL_INACT_ODR_[1:0] bits of the INACTIVITY_DUR (54h) register, gyroscope in sleep mode; 11: sets accelerometer to low-power mode 1 with accelerometer ODR selected through the XL_INACT_ODR_[1:0] bits of the INACTIVITY_DUR (54h) register, gyroscope in power-down mode)

9.48 INACTIVITY_DUR (54h)

Activity/inactivity configuration register (R/W)

Table 133. INACTIVITY_DUR register

SLEEP_STATUS_ON_INT	WU_INACT_THS_W_2	WU_INACT_THS_W_1	WU_INACT_THS_W_0	XL_INACT_ODR_1	XL_INACT_ODR_0	INACT_DUR_1	INACT_DUR_0

Table 134. INACTIVITY_DUR register description

SLEEP_STATUS_ON_INT	Activity/inactivity interrupt mode configuration. If the INT1_SLEEP_CHANGE or INT2_SLEEP_CHANGE bit is enabled, drives the sleep status or sleep change on the INT pin. Default value: 0 (0: sleep change notification on INT pin; 1: sleep status reported on INT pin)
WU_INACT_THS_W_[2:0]	Weight of 1 LSB of wake-up (WU_THS) and activity/inactivity (INACT_THS) threshold. (000: 7.8125 mg/LSB (default); 001: 15.625 mg/LSB; 010: 31.25 mg/LSB; 011: 62.5 mg/LSB; 100: 125 mg/LSB; 101 - 110 - 111: 250 mg/LSB)
XL_INACT_ODR_[1:0]	Selects the ODR_XL target during inactivity. (00: 1.875 Hz; 01: 15 Hz (default); 10: 30 Hz; 11: 60 Hz)
INACT_DUR_[1:0]	Duration in the transition from stationary to motion (from inactivity to activity). (00: transition to motion (activity) immediately at first overthreshold event (default); 01: transition to motion (activity) after two consecutive overthreshold events; 10: transition to motion (activity) after three consecutive overthreshold events; 11: transition to motion (activity) after four consecutive overthreshold events)

9.49 INACTIVITY_THS (55h)

Activity/inactivity threshold setting register (R/W)

Table 135. INACTIVITY_THS register

0(1)	0(1)	INACT_THS_5	INACT_THS_4	INACT_THS_3	INACT_THS_2	INACT_THS_1	INACT_THS_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 136. INACTIVITY_THS register description

INACT_THS_[5:0]	Activity/inactivity threshold. The resolution of the threshold depends on the value of WU_INACT_THS_W_[2:0] in the INACTIVITY_DUR (54h) register. Default value: 000000

9.50 TAP_CFG0 (56h)

Tap configuration register 0 (R/W)

Table 137. TAP_CFG0 register

0[1]	LOW_PASS_ ON_6D	HW_FUNC_MASK _XL_SETTL	SLOPE_ FDS	TAP_Z_EN	TAP_Y_EN	TAP_X_EN	LIR

1. *This bit must be set to 0 for the correct operation of the device.*

Table 138. TAP_CFG0 register description

LOW_PASS_ON_6D	LPF2 filter on 6D function selection. Refer to Figure 30. Default value: 0 (0: ODR/2 low-pass filtered data sent to 6D interrupt function; 1: LPF2 output data sent to 6D interrupt function)
HW_FUNC_MASK_XL_SETTL	Enables masking the execution trigger of the basic interrupt functions (6D/4D, free-fall, wake-up, tap, activity/inactivity) when accelerometer data are settling. Default value: 0 (0: disabled; 1: enabled)
SLOPE_FDS	HPF or slope filter selection on wake-up and activity/inactivity functions. Refer to Figure 30. Default value: 0 (0: slope filter applied; 1: HPF applied)
TAP_Z_EN	Enables Z direction in tap recognition. If the Z-axis is disabled, this bit must be set to 0. Default value: 0 (0: Z direction disabled; 1: Z direction enabled)
TAP_Y_EN	Enables Y direction in tap recognition. If the Y-axis is disabled, this bit must be set to 0. Default value: 0 (0: Y direction disabled; 1: Y direction enabled)
TAP_X_EN	Enables X direction in tap recognition. If the X-axis is disabled, this bit must be set to 0. Default value: 0 (0: X direction disabled; 1: X direction enabled)
LIR	Latched interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)

9.51 TAP_CFG1 (57h)

Tap configuration register 1 (R/W)

Table 139. TAP_CFG1 register

TAP_ PRIORITY_2	TAP_ PRIORITY_1	TAP_ PRIORITY_0	TAP_ THS_Z_4	TAP_ THS_Z_3	TAP_ THS_Z_2	TAP_ THS_Z_1	TAP_ THS_Z_0

Table 140. TAP_CFG1 register description

TAP_PRIORITY_[2:0]	Selection of axis priority for tap detection (see Table 141)
TAP_THS_Z_[4:0]	Z-axis tap recognition threshold. Default value: 0 1 LSB = FS_XL / (2^5)

Table 141. TAP priority decoding

TAP_PRIORITY_[2:0]	Max. priority	Mid. priority	Min. priority
000	Z	Y	X
001	Y	Z	X
010	Z	X	Y
011	X	Y	Z
100	Z	Y	X
101	Y	X	Z
110	X	Z	Y
111	X	Y	Z

9.52 TAP_CFG2 (58h)

Tap configuration register 2 (R/W)

Table 142. TAP_CFG2 register

0(1)	0(1)	0(1)	TAP_ THS_Y_4	TAP_ THS_Y_3	TAP_ THS_Y_2	TAP_ THS_Y_1	TAP_ THS_Y_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 143. TAP_CFG2 register description

TAP_THS_Y_[4:0]	Y-axis tap recognition threshold. Default value: 0 1 LSB = FS_XL / (2^5)

9.53 TAP_THS_6D (59h)

Portrait/landscape position and tap function threshold register (R/W)

Table 144. TAP_THS_6D register

0(1)	SIXD_THS_1	SIXD_THS_0	TAP_ THS_X_4	TAP_ THS_X_3	TAP_ THS_X_2	TAP_ THS_X_1	TAP_ THS_X_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 145. TAP_THS_6D register description

SIXD_THS_[1:0]	Threshold for 6D function. Default value: 00 For details, refer to Table 146.
TAP_THS_X_[4:0]	X-axis recognition threshold. Default value: 0 1 LSB = FS_XL / (2^5)

Table 146. Threshold for D6D function

SIXD_THS_[1:0]	Threshold value
00	80 degrees
01	70 degrees
10	60 degrees
11	50 degrees

9.54 TAP_DUR (5Ah)

Tap recognition function setting register (R/W)

Table 147. TAP_DUR register

DUR_3	DUR_2	DUR_1	DUR_0	QUIET_1	QUIET_0	SHOCK_1	SHOCK_0

Table 148. TAP_DUR register description

DUR_[3:0]	Duration of maximum time gap for double tap recognition. Default: 0000 When double-tap recognition is enabled, this register expresses the maximum time between two consecutive detected taps to determine a double-tap event. The default value of these bits is 0000b which corresponds to 16/ODR_XL time. If the DUR_[3:0] bits are set to a different value, 1LSB corresponds to 32/ODR_XL time.
QUIET_[1:0]	Expected quiet time after a tap detection. Default value: 00 Quiet time is the time after the first detected tap in which there must not be any overthreshold event. The default value of these bits is 00b which corresponds to 2/ODR_XL time. If the QUIET_[1:0] bits are set to a different value, 1LSB corresponds to 4/ODR_XL time.
SHOCK_[1:0]	Maximum duration of overthreshold event. Default value: 00 Maximum duration is the maximum time of an overthreshold signal detection to be recognized as a tap event. The default value of these bits is 00b which corresponds to 4/ODR_XL time. If the SHOCK_[1:0] bits are set to a different value, 1LSB corresponds to 8/ODR_XL time.

9.55 WAKE_UP_THS (5Bh)

Single/double-tap selection and wake-up configuration (R/W)

Table 149. WAKE_UP_THS register

SINGLE_ DOUBLE_TAP	USR_OFF _ON_WU	WK_THS_5	WK_THS_4	WK_THS_3	WK_THS_2	WK_THS_1	WK_THS_0

Table 150. WAKE_UP_THS register description

SINGLE_DOUBLE_TAP	Enables single/double-tap event. Default value: 0 (0: only single-tap event enabled; 1: both single and double-tap events enabled)
USR_OFF_ON_WU	Drives the low-pass filtered data with user offset correction (instead of high-pass filtered data) to the wake-up and the activity/inactivity functions. Refer to Figure 30. Default value: 0
WK_THS_[5:0]	Wake-up threshold. The resolution of the threshold depends on the value of WU_INACT_THS_W_[2:0] in the INACTIVITY_DUR (54h) register. Default value: 000000

9.56 WAKE_UP_DUR (5Ch)

Free-fall, wake-up, and sleep mode functions duration setting register (R/W)

Table 151. WAKE_UP_DUR register

FF_DUR_5	WAKE_DUR_1	WAKE_DUR_0	0(1)	SLEEP_DUR_3	SLEEP_DUR_2	SLEEP_DUR_1	SLEEP_DUR_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 152. WAKE_UP_DUR register description

FF_DUR_5	Free-fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR_[4:0] in the FREE_FALL (5Dh) configuration. 1 LSB = 1/ODR_XL time
WAKE_DUR_[1:0]	Wake-up duration event. Default: 00 1 LSB = 1/ODR_XL time
SLEEP_DUR_[3:0]	Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR) 1 LSB = 512/ODR_XL time

9.57 FREE_FALL (5Dh)

Free-fall function duration setting register (R/W)

Table 153. FREE_FALL register

FF_DUR_4	FF_DUR_3	FF_DUR_2	FF_DUR_1	FF_DUR_0	FF_THS_2	FF_THS_1	FF_THS_0

Table 154. FREE_FALL register description

FF_DUR_[4:0]	Free-fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR_5 in the WAKE_UP_DUR (5Ch) configuration.
FF_THS_[2:0]	Free-fall threshold setting. Default: 000 For details refer to Table 155.

Table 155. Threshold for free-fall function

FF_THS_[2:0]	Threshold value
000	156 mg
001	219 mg
010	250 mg
011	312 mg
100	344 mg
101	406 mg
110	469 mg
111	500 mg

9.58 MD1_CFG (5Eh)

Functions routing to INT1 pin register (R/W). Each bit in this register enables a signal to be carried over the INT1 pin. The output of the pin is the OR combination of the signals selected here and in the INT1_CTRL (0Dh) register.

Table 156. MD1_CFG register

INT1_SLEEP_CHANGE	INT1_SINGLE_TAP	INT1_WU	INT1_FF	INT1_DOUBLE_TAP	INT1_6D	INT1_EMB_FUNC	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 157. MD1_CFG register description

INT1_SLEEP_CHANGE(1)	Routing activity/inactivity recognition event to INT1. Default: 0 (0: routing activity/inactivity event to INT1 disabled; 1: routing activity/inactivity event to INT1 enabled)
INT1_SINGLE_TAP	Routing single-tap recognition event to INT1. Default: 0 (0: routing single-tap event to INT1 disabled; 1: routing single-tap event to INT1 enabled)
INT1_WU	Routing wake-up event to INT1. Default value: 0 (0: routing wake-up event to INT1 disabled; 1: routing wake-up event to INT1 enabled)
INT1_FF	Routing free-fall event to INT1. Default value: 0 (0: routing free-fall event to INT1 disabled; 1: routing free-fall event to INT1 enabled)
INT1_DOUBLE_TAP	Routing tap event to INT1. Default value: 0 (0: routing double-tap event to INT1 disabled; 1: routing double-tap event to INT1 enabled)
INT1_6D	Routing 6D event to INT1. Default value: 0 (0: routing 6D event to INT1 disabled; 1: routing 6D event to INT1 enabled)
INT1_EMB_FUNC	Routing embedded functions event to INT1. Default value: 0 (0: routing embedded functions event to INT1 disabled; 1: routing embedded functions event to INT1 enabled)

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the INACTIVITY_DUR (54h) register.*

9.59 MD2_CFG (5Fh)

Functions routing to INT2 pin register (R/W). Each bit in this register enables a signal to be carried over the INT1 pin. The output of the pin is the OR combination of the signals selected here and in the INT2_CTRL (0Eh) register.

Table 158. MD2_CFG register

INT2_SLEEP_CHANGE	INT2_SINGLE_TAP	INT2_WU	INT2_FF	INT2_DOUBLE_TAP	INT2_6D	INT2_EMB_FUNC	INT2_TIMESTAMP

Table 159. MD2_CFG register description

INT2_SLEEP_CHANGE[1]	Routing activity/inactivity recognition event to INT2. Default: 0 (0: routing activity/inactivity event to INT2 disabled; 1: routing activity/inactivity event to INT2 enabled)
INT2_SINGLE_TAP	Single-tap recognition routing to INT2. Default: 0 (0: routing single-tap event to INT2 disabled; 1: routing single-tap event to INT2 enabled)
INT2_WU	Routing wake-up event to INT2. Default value: 0 (0: routing wake-up event to INT2 disabled; 1: routing wake-up event to INT2 enabled)
INT2_FF	Routing free-fall event to INT2. Default value: 0 (0: routing free-fall event to INT2 disabled; 1: routing free-fall event to INT2 enabled)
INT2_DOUBLE_TAP	Routing tap event to INT2. Default value: 0 (0: routing double-tap event to INT2 disabled; 1: routing double-tap event to INT2 enabled)
INT2_6D	Routing 6D event to INT2. Default value: 0 (0: routing 6D event to INT2 disabled; 1: routing 6D event to INT2 enabled)
INT2_EMB_FUNC	Routing embedded functions event to INT2. Default value: 0 (0: routing embedded functions event to INT2 disabled; 1: routing embedded functions event to INT2 enabled)
INT2_TIMESTAMP	Enables routing the alert for timestamp overflow within 5.6 ms to the INT2 pin.

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the INACTIVITY_DUR (54h) register.*

9.60 EMB_FUNC_CFG (63h)

Embedded functions configuration register (R/W)

Table 160. EMB_FUNC_CFG register

0[1]	0[1]	EMB_FUNC_IRQ_MASK_G_SETTL	EMB_FUNC_IRQ_MASK_XL_SETTL	EMB_FUNC_DISABLE	0[1]	0[1]	0[1]

1. *This bit must be set to 0 for the correct operation of the device.*

Table 161. EMB_FUNC_CFG register description

EMB_FUNC_IRQ_MASK_G_SETTL	Enables / masks execution trigger of the embedded functions when gyroscope data are settling. Default value: 0 (0: disabled; 1: masks execution trigger of the embedded functions until gyroscope filter settling ends)
EMB_FUNC_IRQ_MASK_XL_SETTL	Enables / masks execution trigger of the embedded functions when accelerometer data are settling. Default value: 0 (0: disabled; 1: masks execution trigger of the embedded functions until accelerometer filter settling ends)
EMB_FUNC_DISABLE	Disables execution of the embedded functions. Default value: 0 (0: disabled; 1: embedded functions execution trigger is not generated anymore and all initialization procedures are forced when this bit is set back to 0).

9.61 TDM_CFG0 (6Ch)

TDM configuration register 0 (R/W)

Table 162. TDM_CFG0 register

1(1)	TDM_ DELAYED_CFG	TDM_BCLK _EDGE_SEL	TDM_ SLOT_SEL	0(2)	TDM_ WCLK_1	TDM_ WCLK_0	TDM_WCLK _BCLK_SEL

1. *This bit must be set to 1 for the correct operation of the device.*
2. *This bit must be set to 0 for the correct operation of the device.*

Table 163. TDM_CFG0 register description

TDM_DELAYED_CFG	Enables TDM delayed configuration. Default value: 0 (0: disabled; 1: enabled)
TDM_BCLK_EDGE_SEL	BCLK edge selection for TDM interface. Default value: 0 (0: sampling on BCLK rising edge; 1: sampling on BCLK falling edge)
TDM_SLOT_SEL	Selection of TDM slot for transmission. Default value: 0 (0: slot {0, 1, 2} is selected; 1: slot {4, 5, 6} is selected)
TDM_WCLK_[1:0]	TDM word clock frequency selection (see Table 164)
TDM_WCLK_BCLK_SEL	Selection of cross association between WCLK and BCLK frequencies (see Table 164)

Table 164. WCLK and BCLK frequencies

TDM_WCLK_BCLK_SEL	TDM_WCLK_[1:0]	WCLK	BCLK
0	01	16 kHz	2048 kHz
1	00	8 kHz	2048 kHz

9.62 TDM_CFG1 (6Dh)

TDM configuration register 1 (R/W)

Table 165. TDM_CFG1 register

TDM_XL _X_EN	TDM_XL _Y_EN	TDM_XL _Z_EN	TDM_AXES_ ORD_SEL_1	TDM_AXES_ ORD_SEL_0	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 166. TDM_CFG1 register description

TDM_XL_X_EN	Enables accelerometer X-axis elaboration and transmission (acts on both UI and TDM side). Disabling the X-axis can be done only during the initialization phase, while the accelerometer is in power-down mode and before turning on the accelerometer. The disabling of any axis is not compatible with the free-fall, 4D/6D, or SFLP features and could impact the behavior and performance of the other advanced functions also. Default value: 1 (0: disabled; 1: enabled)
TDM_XL_Y_EN	Enables accelerometer Y-axis elaboration and transmission (acts on both UI and TDM side). Disabling the Y-axis can be done only during the initialization phase, while the accelerometer is in power-down mode and before turning on the accelerometer. The disabling of any axis is not compatible with the free-fall, 4D/6D, or SFLP features and could impact the behavior and performance of the other advanced functions also. Default value: 1 (0: disabled; 1: enabled)
TDM_XL_Z_EN	Enables accelerometer Z-axis elaboration and transmission (acts on both UI and TDM side). Disabling the Z-axis can be done only during the initialization phase, while the accelerometer is in power-down mode and before turning on the accelerometer. The disabling of any axis is not compatible with the free-fall, 4D/6D, or SFLP features and could impact the behavior and performance of the other advanced functions also. Default value: 1 (0: disabled; 1: enabled)
TDM_AXES_ORD_SEL_[1:0]	Selects the order of transmission of the TDM axes (see Table 167)

Table 167. Selection of order of transmission of TDM axes

TDM_AXES_ORD_SEL_[1:0]	Order of axes
00	Z, Y, X
01	X, Z, Y
10	X, Y, Z

9.63 TDM_CFG2 (6Eh)

TDM configuration register 2 (R/W)

Table 168. TDM_CFG2 register

0(1)	0(1)	0(1)	0(1)	TDM_ DATA_MASK	0(1)	TDM_FS _XL_1	TDM_FS _XL_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 169. TDM_CFG2 register description

TDM_DATA_MASK	TDM outputs exception code (0x8000) until data is settled. Default value: 0 (0: disabled; 1: enabled)
TDM_FS_XL_[1:0]	TDM channel accelerometer full-scale selection: (00: ±2 *g*; 01: ±4 *g* (default); 10: ±8 *g*)

9.64 Z_OFS_USR (73h)

Accelerometer Z-axis user offset correction (R/W). The offset value set in the Z_OFS_USR offset register is internally subtracted from the acceleration value measured on the Z-axis.

Table 170. Z_OFS_USR register

Z_OFS_USR_7	Z_OFS_USR_6	Z_OFS_USR_5	Z_OFS_USR_4	Z_OFS_USR_3	Z_OFS_USR_2	Z_OFS_USR_1	Z_OFS_USR_0

Table 171. Z_OFS_USR register description

Z_OFS_USR_[7:0]	Accelerometer Z-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL9 (18h). The offset can be applied to the output registers (see USR_OFF_ON_OUT bit in the CTRL9 (18h) register) or to the wakeup function input data (see USR_OFF_ON_WU bit in the WAKE_UP_THS (5Bh) register). The value must be in the range [-127 127].

9.65 Y_OFS_USR (74h)

Accelerometer Y-axis user offset correction (R/W). The offset value set in the Y_OFS_USR offset register is internally subtracted from the acceleration value measured on the Y-axis.

Table 172. Y_OFS_USR register

Y_OFS_USR_7	Y_OFS_USR_6	Y_OFS_USR_5	Y_OFS_USR_4	Y_OFS_USR_3	Y_OFS_USR_2	Y_OFS_USR_1	Y_OFS_USR_0

Table 173. Y_OFS_USR register description

Y_OFS_USR_[7:0]	Accelerometer Y-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL9 (18h). The offset can be applied to the output registers (see USR_OFF_ON_OUT bit in the CTRL9 (18h) register) or to the wakeup function input data (see USR_OFF_ON_WU bit in the WAKE_UP_THS (5Bh) register). The value must be in the range [-127 127].

9.66 X_OFS_USR (75h)

Accelerometer X-axis user offset correction (R/W). The offset value set in the X_OFS_USR offset register is internally subtracted from the acceleration value measured on the X-axis.

Table 174. X_OFS_USR register

X_OFS_USR_7	X_OFS_USR_6	X_OFS_USR_5	X_OFS_USR_4	X_OFS_USR_3	X_OFS_USR_2	X_OFS_USR_1	X_OFS_USR_0

Table 175. X_OFS_USR register description

X_OFS_USR_[7:0]	Accelerometer X-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL9 (18h). The offset can be applied to the output registers (see USR_OFF_ON_OUT bit in the CTRL9 (18h) register) or to the wakeup function input data (see USR_OFF_ON_WU bit in the WAKE_UP_THS (5Bh) register). The value must be in the range [-127 127].

9.67 FIFO_DATA_OUT_TAG (78h)

FIFO tag register (R)

Table 176. FIFO_DATA_OUT_TAG register

TAG_ SENSOR_4	TAG_ SENSOR_3	TAG_ SENSOR_2	TAG_ SENSOR_1	TAG_ SENSOR_0	TAG_CNT_1	TAG_CNT_0	-

Table 177. FIFO_DATA_OUT_TAG register description

TAG_SENSOR_[4:0]	FIFO tag. Identifies the sensor in: FIFO_DATA_OUT_BYTE_0 (79h) and FIFO_DATA_OUT_BYTE_1 (7Ah), FIFO_DATA_OUT_BYTE_2 (7Bh) and FIFO_DATA_OUT_BYTE_3 (7Ch), and FIFO_DATA_OUT_BYTE_4 (7Dh) and FIFO_DATA_OUT_BYTE_5 (7Eh) For details, refer to Table 178.
TAG_CNT_[1:0]	2-bit counter which identifies sensor time slot

Table 178. FIFO tag

TAG_SENSOR_[4:0]	Sensor name
0x00	FIFO empty
0x01	Gyroscope NC(1)
0x02	Accelerometer NC(2)
0x03	Temperature
0x04	Timestamp
0x05	CFG_Change
0x06	Accelerometer NC_T_2(2)
0x07	Accelerometer NC_T_1(2)
0x08	Accelerometer 2xC(2)
0x09	Accelerometer 3xC(2)
0x0A	Gyroscope NC_T_2(1)
0x0B	Gyroscope NC_T_1(1)
0x0C	Gyroscope 2xC(1)
0x0D	Gyroscope 3xC(1)
0x12	Step counter
0x13	SFLP game rotation vector
0x16	SFLP gyroscope bias
0x17	SFLP gravity vector
0x1A	MLC result
0x1B	MLC filter
0x1C	MLC feature
0x1D	Accelerometer DualC(2)
0x1F	Qvar

1. *Gyroscope data are stored in FIFO in the order of the X, Y, Z axes.*
2. *Accelerometer data are stored in FIFO in the order of the Z, Y, X axes.*

9.68 FIFO_DATA_OUT_BYTE_0 (79h) and FIFO_DATA_OUT_BYTE_1 (7Ah)

FIFO data output (R)

FIFO provides 6 bytes output, starting from byte 0 up to byte 5.

Table 179. FIFO_DATA_OUT_BYTE_1 and FIFO_DATA_OUT_BYTE_0 registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 180. FIFO_DATA_OUT_BYTE_1 and FIFO_DATA_OUT_BYTE_0 register description

D[15:0]	FIFO output byte 1 and 0

9.69 FIFO_DATA_OUT_BYTE_2 (7Bh) and FIFO_DATA_OUT_BYTE_3 (7Ch)

FIFO data output (R)

FIFO provides 6 bytes output, starting from byte 0 up to byte 5.

Table 181. FIFO_DATA_OUT_BYTE_3 and FIFO_DATA_OUT_BYTE_2 registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 182. FIFO_DATA_OUT_BYTE_3 and FIFO_DATA_OUT_BYTE_2 register description

D[15:0]	FIFO output byte 3 and 2

9.70 FIFO_DATA_OUT_BYTE_4 (7Dh) and FIFO_DATA_OUT_BYTE_5 (7Eh)

FIFO data output (R)

FIFO provides 6 bytes output, starting from byte 0 up to byte 5.

Table 183. FIFO_DATA_OUT_BYTE_5 and FIFO_DATA_OUT_BYTE_4 registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 184. FIFO_DATA_OUT_BYTE_5 and FIFO_DATA_OUT_BYTE_4 register description

D[15:0]	FIFO output byte 5 and 4

10 Embedded functions register mapping

The table given below provides a list of the registers for the embedded functions available in the device and the corresponding addresses. Embedded functions registers are accessible when EMB_FUNC_REG_ACCESS is set to 1 in FUNC_CFG_ACCESS (01h).

Table 185. Register address map - embedded functions

Name	Type	Register address		Default	Comment
		Hex	Binary		
PAGE_SEL	R/W	02	00000010	00000001	
EMB_FUNC_EN_A	R/W	04	00000100	00000000	
EMB_FUNC_EN_B	R/W	05	00000101	00000000	
EMB_FUNC_EXEC_STATUS	R	07	00000111	output	
PAGE_ADDRESS	R/W	08	00001000	00000000	
PAGE_VALUE	R/W	09	00001001	00000000	
EMB_FUNC_INT1	R/W	0A	00001010	00000000	
FSM_INT1	R/W	0B	00001011	00000000	
RESERVED	-	0C	00001100		
MLC_INT1	R/W	0D	00001101	00000000	
EMB_FUNC_INT2	R/W	0E	00001110	00000000	
FSM_INT2	R/W	0F	00001111	00000000	
RESERVED	-	10	00010000		
MLC_INT2	R/W	11	00010001	00000000	
EMB_FUNC_STATUS	R	12	00010010	output	
FSM_STATUS	R	13	00010011	output	
RESERVED	-	14	00010100		
MLC_STATUS	R	15	00010101	output	
PAGE_RW	R/W	17	00010111	00000000	
RESERVED	-	18-43			
EMB_FUNC_FIFO_EN_A	R/W	44	01000100	00000000	
EMB_FUNC_FIFO_EN_B	R/W	45	01000101		
FSM_ENABLE	R/W	46	01000110	00000000	
RESERVED	-	47	01000111		
FSM_LONG_COUNTER_L	R/W	48	01001000	00000000	
FSM_LONG_COUNTER_H	R/W	49	01001001	00000000	
RESERVED	-	4A			
INT_ACK_MASK	R/W	4B	01001011	00000000	
FSM_OUTS1	R	4C	01001100	output	
FSM_OUTS2	R	4D	01001101	output	
FSM_OUTS3	R	4E	01001110	output	
FSM_OUTS4	R	4F	01001111	output	
FSM_OUTS5	R	50	01010000	output	
FSM_OUTS6	R	51	01010001	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
FSM_OUTS7	R	52	01010010	output	
FSM_OUTS8	R	53	01010011	output	
RESERVED	-	54- 5D			
SFLP_ODR	R/W	5E	01011110	01011011	
FSM_ODR	R/W	5F	01011111	01001011	
MLC_ODR	R/W	60	01100000	00010101	
STEP_COUNTER_L	R	62	01100010	output	
STEP_COUNTER_H	R	63	01100011	output	
EMB_FUNC_SRC	R/W	64	01100100	output	
EMB_FUNC_INIT_A	R/W	66	01100110	00000000	
EMB_FUNC_INIT_B	R/W	67	01100111	00000000	
MLC1_SRC	R	70	01110000	output	
MLC2_SRC	R	71	01110001	output	
MLC3_SRC	R	72	01110010	output	
MLC4_SRC	R	73	01110011	output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.
The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

11 Embedded functions register description

11.1 PAGE_SEL (02h)

Enable advanced features dedicated page (R/W)

Table 186. PAGE_SEL register

PAGE_SEL3	PAGE_SEL2	PAGE_SEL1	PAGE_SEL0	0(1)	0(1)	0(1)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 187. PAGE_SEL register description

PAGE_SEL[3:0]	Select the advanced features dedicated page Default value: 0000

11.2 EMB_FUNC_EN_A (04h)

Enable embedded functions register (R/W)

Table 188. EMB_FUNC_EN_A register

MLC_BEFORE_FSM_EN	0(1)	SIGN_MOTION_EN	TILT_EN	PEDO_EN	0(1)	SFLP_GAME_EN	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 189. EMB_FUNC_EN_A register description

MLC_BEFORE_FSM_EN(1)	Enables the machine learning core function. When the machine learning core is enabled by setting this bit to 1, the MLC algorithms are executed before the FSM programs. Default value: 0 (0: machine learning core function disabled; 1: machine learning core function enabled and executed before FSM programs)
SIGN_MOTION_EN	Enables significant motion detection function. Default value: 0 (0: significant motion detection function disabled; 1: significant motion detection function enabled)
TILT_EN	Enables tilt calculation. Default value: 0 (0: tilt algorithm disabled; 1: tilt algorithm enabled)
PEDO_EN	Enables pedometer algorithm. Default value: 0 (0: pedometer algorithm disabled; 1: pedometer algorithm enabled)
SFLP_GAME_EN	Enables sensor fusion low-power algorithm for 6-axis (accelerometer + gyroscope) game rotation vector. Default value: 0 (0: sensor fusion algorithm for 6-axis accelerometer + gyroscope disabled; 1: sensor fusion algorithm for 6-axis accelerometer + gyroscope enabled)

1. *MLC_EN bit in the EMB_FUNC_EN_B (05h) register must be set to 0 when using this bit.*

11.3 EMB_FUNC_EN_B (05h)

Enable embedded functions register (R/W)

Table 190. EMB_FUNC_EN_B register

0(1)	0(1)	0(1)	MLC_EN	FIFO_ COMPR_EN	0(1)	0(1)	FSM_EN

1. *This bit must be set to 0 for the correct operation of the device.*

Table 191. EMB_FUNC_EN_B register description

MLC_EN(1)	Enables machine learning core function. When the machine learning core is enabled by setting this bit to 1, the MLC algorithms are executed after the FSM programs. Default value: 0 (0: machine learning core function disabled; 1: machine learning core function enabled and executed after FSM programs)
FIFO_COMPR_EN(1)	Enables FIFO compression function. Default value: 0 (0: FIFO compression function disabled; 1: FIFO compression function enabled)
FSM_EN	Enables finite state machine (FSM) function. Default value: 0 (0: FSM function disabled; 1: FSM function enabled)

1. *MLC_BEFORE_FSM_EN bit in the EMB_FUNC_EN_A (04h) register must be set to 0 when using this bit.*
2. *This bit is active when the FIFO_COMPR_RT_EN bit of FIFO_CTRL2 (08h) is set to 1.*

11.4 EMB_FUNC_EXEC_STATUS (07h)

Embedded functions execution status register (R)

Table 192. EMB_FUNC_EXEC_STATUS register

0	0	0	0	0	0	EMB_FUNC_ EXEC_OVR	EMB_FUNC _ENDOP

Table 193. EMB_FUNC_EXEC_STATUS register description

EMB_FUNC_EXEC_OVR	This bit is set to 1 when the execution of the embedded functions program exceeds maximum time (new data are generated before the end of the algorithms). Default value: 0
EMB_FUNC_ENDOP	When this bit is set to 1, no embedded function is running. Default value: 0

11.5 PAGE_ADDRESS (08h)

Page address register (R/W)

Table 194. PAGE_ADDRESS register

PAGE_ ADDR7	PAGE_ ADDR6	PAGE_ ADDR5	PAGE_ ADDR4	PAGE_ ADDR3	PAGE_ ADDR2	PAGE_ ADDR1	PAGE_ ADDR0

Table 195. PAGE_ADDRESS register description

PAGE_ADDR[7:0]	After setting the bit PAGE_WRITE / PAGE_READ in register PAGE_RW (17h), this register is used to set the address of the register to be written/read in the advanced features page selected through the bits PAGE_SEL[3:0] in register PAGE_SEL (02h).

11.6 PAGE_VALUE (09h)

Page value register (R/W)

Table 196. PAGE_VALUE register

PAGE_ VALUE7	PAGE_ VALUE6	PAGE_ VALUE5	PAGE_ VALUE4	PAGE_ VALUE3	PAGE_ VALUE2	PAGE_ VALUE1	PAGE_ VALUE0

Table 197. PAGE_VALUE register description

PAGE_VALUE[7:0]	These bits are used to write (if the bit PAGE_WRITE = 1 in register PAGE_RW (17h)) or read (if the bit PAGE_READ = 1 in register PAGE_RW (17h)) the data at the address PAGE_ADDR[7:0] of the selected advanced features page.

11.7 EMB_FUNC_INT1 (0Ah)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

Table 198. EMB_FUNC_INT1 register

INT1_ FSM_LC	0(1)	INT1_ SIG_MOT	INT1_TILT	INT1_STEP _DETECTOR	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 199. EMB_FUNC_INT1 register description

INT1_FSM_LC(1)	Routing FSM long counter timeout interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_SIG_MOT(1)	Routing significant motion event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_TILT(1)	Routing tilt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_STEP_DETECTOR(1)	Routing pedometer step recognition event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)

1. *This bit is active when the INT1_EMB_FUNC bit of MD1_CFG (5Eh) is set to 1.*

11.8 FSM_INT1 (0Bh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

Table 200. FSM_INT1 register

INT1_FSM8	INT1_FSM7	INT1_FSM6	INT1_FSM5	INT1_FSM4	INT1_FSM3	INT1_FSM2	INT1_FSM1

Table 201. FSM_INT1 register description

INT1_FSM8[1]	Routing FSM8 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM7[1]	Routing FSM7 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM6[1]	Routing FSM6 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM5[1]	Routing FSM5 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM4[1]	Routing FSM4 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM3[1]	Routing FSM3 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM2[1]	Routing FSM2 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM1[1]	Routing FSM1 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)

1. *This bit is active when the INT1_EMB_FUNC bit of MD1_CFG (5Eh) is set to 1.*

11.9 MLC_INT1 (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

Table 202. MLC_INT1 register

0(1)	0(1)	0(1)	0(1)	INT1_MLC4	INT1_MLC3	INT1_MLC2	INT1_MLC1

1. *This bit must be set to 0 for the correct operation of the device.*

Table 203. MLC_INT1 register description

INT1_MLC4	Routing MLC4 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC3	Routing MLC3 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC2	Routing MLC2 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC1	Routing MLC1 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)

11.10 EMB_FUNC_INT2 (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

Table 204. EMB_FUNC_INT2 register

INT2_ FSM_LC	0(1)	INT2_ SIG_MOT	INT2_TILT	INT2_STEP _DETECTOR	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 205. EMB_FUNC_INT2 register description

INT2_FSM_LC(1)	Routing FSM long counter timeout interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_SIG_MOT(1)	Routing significant motion event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_TILT(1)	Routing tilt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_STEP_DETECTOR(1)	Routing pedometer step recognition event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)

1. *This bit is active when the INT2_EMB_FUNC bit of MD2_CFG (5Fh) is set to 1.*

11.11 FSM_INT2 (0Fh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

Table 206. FSM_INT2 register

INT2_FSM8	INT2_FSM7	INT2_FSM6	INT2_FSM5	INT2_FSM4	INT2_FSM3	INT2_FSM2	INT2_FSM1

Table 207. FSM_INT2 register description

INT2_FSM8(1)	Routing FSM8 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM7(1)	Routing FSM7 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM6(1)	Routing FSM6 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM5(1)	Routing FSM5 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM4(1)	Routing FSM4 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM3(1)	Routing FSM3 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM2(1)	Routing FSM2 interrupt event on INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM1(1)	Routing FSM1 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)

1. *This bit is active when the INT2_EMB_FUNC bit of MD2_CFG (5Fh) is set to 1.*

11.12 MLC_INT2 (11h)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

Table 208. MLC_INT2 register

0(1)	0(1)	0(1)	0(1)	INT2_MLC4	INT2_MLC3	INT2_MLC2	INT2_MLC1

1. *This bit must be set to 0 for the correct operation of the device.*

Table 209. MLC_INT2 register description

INT2_MLC4	Routing MLC4 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC3	Routing MLC3 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC2	Routing MLC2 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC1	Routing MLC1 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)

11.13 EMB_FUNC_STATUS (12h)

Embedded function status register (R)

Table 210. EMB_FUNC_STATUS register

IS_FSM_LC	0	IS_SIGMOT	IS_TILT	IS_STEP_DET	0	0	0

Table 211. EMB_FUNC_STATUS register description

IS_FSM_LC	Interrupt status bit for FSM long counter timeout interrupt event. (1: interrupt detected; 0: no interrupt)
IS_SIGMOT	Interrupt status bit for significant motion detection (1: interrupt detected; 0: no interrupt)
IS_TILT	Interrupt status bit for tilt detection (1: interrupt detected; 0: no interrupt)
IS_STEP_DET	Interrupt status bit for step detection (1: interrupt detected; 0: no interrupt)

11.14 FSM_STATUS (13h)

Finite state machine status register (R)

Table 212. FSM_STATUS register

IS_FSM8	IS_FSM7	IS_FSM6	IS_FSM5	IS_FSM4	IS_FSM3	IS_FSM2	IS_FSM1

Table 213. FSM_STATUS register description

IS_FSM8	Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM7	Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM6	Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM5	Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM4	Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM3	Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM2	Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM1	Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt)

11.15 MLC_STATUS (15h)

Machine learning core status register (R)

Table 214. MLC_STATUS register

0	0	0	0	IS_MLC4	IS_MLC3	IS_MLC	IS_MLC1

Table 215. MLC_STATUS register description

IS_MLC4	Interrupt status bit for MLC4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC3	Interrupt status bit for MLC3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC2	Interrupt status bit for MLC2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC1	Interrupt status bit for MLC1 interrupt event. (1: interrupt detected; 0: no interrupt)

11.16 PAGE_RW (17h)

Enable read and write mode of advanced features dedicated page (R/W)

Table 216. PAGE_RW register

EMB_ FUNC_LIR	PAGE_ WRITE	PAGE_ READ	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 217. PAGE_RW register description

EMB_FUNC_LIR	Latched interrupt mode for embedded functions. Default value: 0 (0: embedded functions interrupt request not latched; 1: embedded functions interrupt request latched)
PAGE_WRITE	Enables writes to the selected advanced features dedicated page.(1) Default value: 0 (1: enable; 0: disable)
PAGE_READ	Enables reads from the selected advanced features dedicated page.(1) Default value: 0 (1: enable; 0: disable)

1. *Page selected by PAGE_SEL[3:0] in PAGE_SEL (02h) register.*

11.17 EMB_FUNC_FIFO_EN_A (44h)

Embedded functions FIFO configuration register A (R/W)

Table 218. EMB_FUNC_FIFO_EN_A register

MLC_ FIFO_EN	STEP_COUNTER _FIFO_EN	SFLP_GBIAS _FIFO_EN	SFLP_GRAVITY _FIFO_EN	0(1)	0(1)	SFLP_GAME _FIFO_EN	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 219. EMB_FUNC_FIFO_EN_A register description

MLC_FIFO_EN	Enables batching the machine learning core results in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
STEP_COUNTER_FIFO_EN	Enables batching the step counter values in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
SFLP_GBIAS_FIFO_EN	Enables batching the gyroscope bias values computed by the SFLP algorithm in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
SFLP_GRAVITY_FIFO_EN	Enables batching the gravity values computed by the SFLP algorithm in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
SFLP_GAME_FIFO_EN	Enables batching the game rotation vector (quaternion) values computed by the SFLP algorithm in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)

11.18 EMB_FUNC_FIFO_EN_B (45h)

Embedded functions FIFO configuration register B (R/W)

Table 220. EMB_FUNC_FIFO_EN_B register

0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	MLC_FILTER_FEATURE_FIFO_EN	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 221. EMB_FUNC_FIFO_EN_B register description

MLC_FILTER_FEATURE_FIFO_EN	Enables batching the machine learning core filters and features in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)

11.19 FSM_ENABLE (46h)

Enable FSM register (R/W)

Table 222. FSM_ENABLE register

FSM8_EN	FSM7_EN	FSM6_EN	FSM5_EN	FSM4_EN	FSM3_EN	FSM2_EN	FSM1_EN

Table 223. FSM_ENABLE register description

FSM8_EN	Enables FSM8. Default value: 0 (0: FSM8 disabled; 1: FSM8 enabled)
FSM7_EN	Enables FSM7. Default value: 0 (0: FSM7 disabled; 1: FSM7 enabled)
FSM6_EN	Enables FSM6. Default value: 0 (0: FSM6 disabled; 1: FSM6 enabled)
FSM5_EN	Enables FSM5. Default value: 0 (0: FSM5 disabled; 1: FSM5 enabled)
FSM4_EN	Enables FSM4. Default value: 0 (0: FSM4 disabled; 1: FSM4 enabled)
FSM3_EN	Enables FSM3. Default value: 0 (0: FSM3 disabled; 1: FSM3 enabled)
FSM2_EN	Enables FSM2. Default value: 0 (0: FSM2 disabled; 1: FSM2 enabled)
FSM1_EN	Enables FSM1. Default value: 0 (0: FSM1 disabled; 1: FSM1 enabled)

11.20 FSM_LONG_COUNTER_L (48h) and FSM_LONG_COUNTER_H (49h)

FSM long counter status register (R/W)

Long counter value is an unsigned integer value (16-bit format).

Table 224. FSM_LONG_COUNTER_L register

FSM_LC_7	FSM_LC_6	FSM_LC_5	FSM_LC_4	FSM_LC_3	FSM_LC_2	FSM_LC_1	FSM_LC_0

Table 225. FSM_LONG_COUNTER_L register description

FSM_LC_[7:0]	Long counter current value (LSbyte). Default value: 00000000

Table 226. FSM_LONG_COUNTER_H register

FSM_LC_15	FSM_LC_14	FSM_LC_13	FSM_LC_12	FSM_LC_11	FSM_LC_10	FSM_LC_9	FSM_LC_8

Table 227. FSM_LONG_COUNTER_H register description

FSM_LC_[15:8]	Long counter current value (MSbyte). Default value: 00000000

11.21 INT_ACK_MASK (4Bh)

Reset status register (R/W)

Table 228. INT_ACK_MASK register

IACK_ MASK7	IACK_ MASK6	IACK_ MASK5	IACK_ MASK4	IACK_ MASK3	IACK_ MASK2	IACK_ MASK1	IACK_ MASK0

Table 229. INT_ACK_MASK register description

IACK_MASK7	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 7 of the status register is not reset. When this bit is set to 0, bit 7 of the status register is reset. Default value: 0
IACK_MASK6	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 6 of the status register is not reset. When this bit is set to 0, bit 6 of the status register is reset. Default value: 0
IACK_MASK5	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 5 of the status register is not reset. When this bit is set to 0, bit 5 of the status register is reset. Default value: 0
IACK_MASK4	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 4 of the status register is not reset. When this bit is set to 0, bit 4 of the status register is reset. Default value: 0
IACK_MASK3	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 3 of the status register is not reset. When this bit is set to 0, bit 3 of the status register is reset. Default value: 0
IACK_MASK2	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 2 of the status register is not reset. When this bit is set to 0, bit 2 of the status register is reset. Default value: 0
IACK_MASK1	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 1 of the status register is not reset. When this bit is set to 0, bit 1 of the status register is reset. Default value: 0
IACK_MASK0	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (4Bh) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 0 of the status register is not reset. When this bit is set to 0, bit 0 of the status register is reset. Default value: 0

11.22 FSM_OUTS1 (4Ch)

FSM1 output register (R)

Table 230. FSM_OUTS1 register

P_axis_1	N_axis_1	P_axis_2	N_axis_2	P_axis_3	N_axis_3	P_V	N_V

Table 231. FSM_OUTS1 register description

P_axis_1	FSM1 output: positive event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
N_axis_1	FSM1 output: negative event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
P_axis_2	FSM1 output: positive event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
N_axis_2	FSM1 output: negative event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
P_axis_3	FSM1 output: positive event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
N_axis_3	FSM1 output: negative event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
P_V	FSM1 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM1 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.23 FSM_OUTS2 (4Dh)

FSM2 output register (R)

Table 232. FSM_OUTS2 register

P_axis_1	N_axis_1	P_axis_2	N_axis_2	P_axis_3	N_axis_3	P_V	N_V

Table 233. FSM_OUTS2 register description

P_axis_1	FSM2 output: positive event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
N_axis_1	FSM2 output: negative event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
P_axis_2	FSM2 output: positive event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
N_axis_2	FSM2 output: negative event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
P_axis_3	FSM2 output: positive event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
N_axis_3	FSM2 output: negative event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
P_V	FSM2 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM2 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.24 FSM_OUTS3 (4Eh)

FSM3 output register (R)

Table 234. FSM_OUTS3 register

P_axis_1	N_axis_1	P_axis_2	N_axis_2	P_axis_3	N_axis_3	P_V	N_V

Table 235. FSM_OUTS3 register description

P_axis_1	FSM3 output: positive event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
N_axis_1	FSM3 output: negative event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
P_axis_2	FSM3 output: positive event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
N_axis_2	FSM3 output: negative event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
P_axis_3	FSM3 output: positive event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
N_axis_3	FSM3 output: negative event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
P_V	FSM3 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM3 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.25 FSM_OUTS4 (4Fh)

FSM4 output register (R)

Table 236. FSM_OUTS4 register

P_axis_1	N_axis_1	P_axis_2	N_axis_2	P_axis_3	N_axis_3	P_V	N_V

Table 237. FSM_OUTS4 register description

P_axis_1	FSM4 output: positive event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
N_axis_1	FSM4 output: negative event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
P_axis_2	FSM4 output: positive event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
N_axis_2	FSM4 output: negative event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
P_axis_3	FSM4 output: positive event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
N_axis_3	FSM4 output: negative event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
P_V	FSM4 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM4 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.26 FSM_OUTS5 (50h)

FSM5 output register (R)

Table 238. FSM_OUTS5 register

P_axis_1	N_axis_1	P_axis_2	N_axis_2	P_axis_3	N_axis_3	P_V	N_V

Table 239. FSM_OUTS5 register description

P_axis_1	FSM5 output: positive event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
N_axis_1	FSM5 output: negative event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
P_axis_2	FSM5 output: positive event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
N_axis_2	FSM5 output: negative event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
P_axis_3	FSM5 output: positive event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
N_axis_3	FSM5 output: negative event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
P_V	FSM5 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM5 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.27 FSM_OUTS6 (51h)

FSM6 output register (R)

Table 240. FSM_OUTS6 register

P_axis_1	N_axis_1	P_axis_2	N_axis_2	P_axis_3	N_axis_3	P_V	N_V

Table 241. FSM_OUTS6 register description

P_axis_1	FSM6 output: positive event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
N_axis_1	FSM6 output: negative event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
P_axis_2	FSM6 output: positive event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
N_axis_2	FSM6 output: negative event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
P_axis_3	FSM6 output: positive event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
N_axis_3	FSM6 output: negative event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
P_V	FSM6 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM6 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.28 FSM_OUTS7 (52h)

FSM7 output register (R)

Table 242. FSM_OUTS7 register

P_axis_1	N_axis_1	P_axis_2	N_axis_2	P_axis_3	N_axis_3	P_V	N_V

Table 243. FSM_OUTS7 register description

P_axis_1	FSM7 output: positive event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
N_axis_1	FSM7 output: negative event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
P_axis_2	FSM7 output: positive event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
N_axis_2	FSM7 output: negative event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
P_axis_3	FSM7 output: positive event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
N_axis_3	FSM7 output: negative event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
P_V	FSM7 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM7 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.29 FSM_OUTS8 (53h)

FSM8 output register (R)

Table 244. FSM_OUTS8 register

P_axis_1	N_axis_1	P_axis_2	N_axis_2	P_axis_3	N_axis_3	P_V	N_V

Table 245. FSM_OUTS8 register description

P_axis_1	FSM8 output: positive event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
N_axis_1	FSM8 output: negative event detected on axis 1. This axis corresponds to the X-axis if the gyrocope is used and to the Z-axis if the accelerometer is used. Results related to Qvar are reported on axis 1. (0: event not detected; 1: event detected)
P_axis_2	FSM8 output: positive event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
N_axis_2	FSM8 output: negative event detected on axis 2. This axis corresponds to the Y-axis for both the gyrocope and accelerometer. (0: event not detected; 1: event detected)
P_axis_3	FSM8 output: positive event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
N_axis_3	FSM8 output: negative event detected on axis 3. This axis corresponds to the Z-axis if the gyrocope is used and to the X-axis if the accelerometer is used. (0: event not detected; 1: event detected)
P_V	FSM8 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM8 output: negative event detected on the vector. (0: event not detected; 1: event detected)

11.30 SFLP_ODR (5Eh)

Sensor fusion low-power output data rate configuration register (R/W)

Table 246. SFLP_ODR register

0(1)	1(2)	SFLP_GAME_ODR_2	SFLP_GAME_ODR_1	SFLP_GAME_ODR_0	0(1)	1(2)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 247. SFLP_ODR register description

SFLP_GAME_ODR_[2:0]	ODR configuration of the SFLP game algorithm: (000: 15 Hz; 001: 30 Hz; 010: 60 Hz; 011: 120 Hz (default); 100: 240 Hz; 101: 480 Hz)

11.31 FSM_ODR (5Fh)

Finite state machine output data rate configuration register (R/W)

Table 248. FSM_ODR register

0(1)	1(2)	FSM_ODR_2	FSM_ODR_1	FSM_ODR_0	0(1)	1(2)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 249. FSM_ODR register description

FSM_ODR_[2:0]	Finite state machine ODR configuration: (000: 15 Hz; 001: 30 Hz (default); 010: 60 Hz; 011: 120 Hz; 100: 240 Hz; 101: 480 Hz; 110: 960 Hz)

11.32 MLC_ODR (60h)

Machine learning core output data rate configuration register (R/W)

Table 250. MLC_ODR register

0(1)	MLC_ODR_2	MLC_ODR_1	MLC_ODR_0	0(1)	1(2)	0(1)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 251. MLC_ODR register description

MLC_ODR_[2:0]	Machine learning core ODR configuration: (000: 15 Hz; 001: 30 Hz (default); 010: 60 Hz; 011: 120 Hz; 100: 240 Hz; 101: 480 Hz; 110: 960 Hz)

11.33 STEP_COUNTER_L (62h) and STEP_COUNTER_H (63h)

Step counter output register (R)

Table 252. STEP_COUNTER_L register

STEP_7	STEP_6	STEP_5	STEP_4	STEP_3	STEP_2	STEP_1	STEP_0

Table 253. STEP_COUNTER_L register description

STEP_[7:0]	Step counter output (LSbyte)

Table 254. STEP_COUNTER_H register

STEP_15	STEP_14	STEP_13	STEP_12	STEP_11	STEP_10	STEP_9	STEP_8

Table 255. STEP_COUNTER_H register description

STEP_[15:8]	Step counter output (MSbyte)

11.34 EMB_FUNC_SRC (64h)

Embedded function source register (R/W)

Table 256. EMB_FUNC_SRC register

PEDO_ RST_STEP	0(1)	STEP_ DETECTED	STEP_COUNT _DELTA_IA	STEP_ OVERFLOW	STEPCOUNTER _BIT_SET	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 257. EMB_FUNC_SRC register description

PEDO_RST_STEP	Reset pedometer step counter. Read/write bit. (0: disabled; 1: enabled)
STEP_DETECTED	Step detector event detection status. Read-only bit. (0: step detection event not detected; 1: step detection event detected)
STEP_COUNT_DELTA_IA	Pedometer step recognition on delta time status. Read-only bit. (0: no step recognized during delta time; 1: at least one step recognized during delta time)
STEP_OVERFLOW	Step counter overflow status. Read-only bit. (0: step counter value < 2^{16}; 1: step counter value reached 2^{16})
STEPCOUNTER_BIT_SET	This bit is equal to 1 when the step count is increased. If a timer period is programmed in PEDO_SC_DELTAT_L (D0h) and PEDO_SC_DELTAT_H (D1h) embedded advanced features (page 1) registers, this bit is kept at 0. Read-only bit.

11.35 EMB_FUNC_INIT_A (66h)

Embedded functions initialization register (R/W)

Table 258. EMB_FUNC_INIT_A register

MLC_BEFORE_FSM_INIT	0(1)	SIG_MOT_INIT	TILT_INIT	STEP_DET_INIT	0(1)	SFLP_GAME_INIT	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 259. EMB_FUNC_INIT_A register description

MLC_BEFORE_FSM_INIT	Machine learning core initialization request (MLC executed before FSM). Default value: 0
SIG_MOT_INIT	Significant motion detection algorithm initialization request. Default value: 0
TILT_INIT	Tilt algorithm initialization request. Default value: 0
STEP_DET_INIT	Pedometer step counter/detector algorithm initialization request. Default value: 0
SFLP_GAME_INIT	SFLP game algorithm initialization request. Default value: 0

11.36 EMB_FUNC_INIT_B (67h)

Embedded functions initialization register (R/W)

Table 260. EMB_FUNC_INIT_B register

0(1)	0(1)	0(1)	MLC_INIT	FIFO_COMPR_INIT	0(1)	0(1)	FSM_INIT

1. *This bit must be set to 0 for the correct operation of the device.*

Table 261. EMB_FUNC_INIT_B register description

MLC_INIT	Machine learning core initialization request (MLC executed after FSM). Default value: 0
FIFO_COMPR_INIT	FIFO compression function initialization request. Default value: 0
FSM_INIT	FSM initialization request. Default value: 0

11.37 MLC1_SRC (70h)

Machine learning core source register (R)

Table 262. MLC1_SRC register

MLC1_SRC_7	MLC1_SRC_6	MLC1_SRC_5	MLC1_SRC_4	MLC1_SRC_3	MLC1_SRC_2	MLC1_SRC_1	MLC1_SRC_0

Table 263. MLC1_SRC register description

MLC1_SRC_[7:0]	Output value of MLC1 decision tree

11.38 MLC2_SRC (71h)

Machine learning core source register (R)

Table 264. MLC2_SRC register

MLC2_SRC_7	MLC2_SRC_6	MLC2_SRC_5	MLC2_SRC_4	MLC2_SRC_3	MLCS2_SRC_2	MLC2_SRC_1	MLC2_SRC_0

Table 265. MLC2_SRC register description

MLC2_SRC_[7:0]	Output value of MLC2 decision tree

11.39 MLC3_SRC (72h)

Machine learning core source register (R)

Table 266. MLC3_SRC register

MLC3_SRC_7	MLC3_SRC_6	MLC3_SRC_5	MLC3_SRC_4	MLC3_SRC_3	MLC3_SRC_2	MLC3_SRC_1	MLC3_SRC_0

Table 267. MLC3_SRC register description

MLC3_SRC_[7:0]	Output value of MLC3 decision tree

11.40 MLC4_SRC (73h)

Machine learning core source register (R)

Table 268. MLC4_SRC register

MLC4_SRC_7	MLC4_SRC_6	MLC4_SRC_5	MLC4_SRC_4	MLC4_SRC_3	MLC4_SRC_2	MLC4_SRC_1	MLC4_SRC_0

Table 269. MLC4_SRC register description

MLC4_SRC_[7:0]	Output value of MLC4 decision tree

12 Embedded advanced features pages

The table given below provides a list of the registers for the embedded advanced features page 0. These registers are accessible when PAGE_SEL[3:0] are set to 0000 in PAGE_SEL (02h).

Table 270. Register address map - embedded advanced features page 0

Name	Type	Register address		Default	Comment
		Hex	Binary		
SFLP_GAME_GBIASX_L	R/W	6E	01101110	00000000	
SFLP_GAME_GBIASX_H	R/W	6F	01101111	00000000	
SFLP_GAME_GBIASY_L	R/W	70	01110000	00000000	
SFLP_GAME_GBIASY_H	R/W	71	01110001	00000000	
SFLP_GAME_GBIASZ_L	R/W	72	01110010	00000000	
SFLP_GAME_GBIASZ_H	R/W	73	01110011	00000000	
FSM_QVAR_SENSITIVITY_L	R/W	BA	10111010	00100100	
FSM_QVAR_SENSITIVITY_H	R/W	BB	10111011	00010110	

The following table provides a list of the registers for the embedded advanced features page 1. These registers are accessible when PAGE_SEL[3:0] are set to 0001 in PAGE_SEL (02h).

Table 271. Register address map - embedded advanced features page 1

Name	Type	Register address		Default	Comment
		Hex	Binary		
FSM_LC_TIMEOUT_L	R/W	7A	01111010	00000000	
FSM_LC_TIMEOUT_H	R/W	7B	01111011	00000000	
FSM_PROGRAMS	R/W	7C	01111100	00000000	
FSM_START_ADD_L	R/W	7E	01111110	00000000	
FSM_START_ADD_H	R/W	7F	01111111	00000000	
PEDO_CMD_REG	R/W	83	10000011	00000000	
PEDO_DEB_STEPS_CONF	R/W	84	10000100	00001010	
PEDO_SC_DELTAT_L	R/W	D0	11010000	00000000	
PEDO_SC_DELTAT_H	R/W	D1	11010001	00000000	
MLC_QVAR_SENSITIVITY_L	R/W	E8	11101000	0000000	
MLC_QVAR_SENSITIVITY_H	R/W	E9	11101001	00111100	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

Write procedure example: write value 06h in register at address 84h (PEDO_DEB_STEPS_CONF) in page 1

1. Write bit EMB_FUNC_REG_ACCESS = 1 in FUNC_CFG_ACCESS (01h) // Enable access to embedded functions registers
2. Write bit PAGE_WRITE = 1 in PAGE_RW (17h) register // Select write operation mode
3. Write 0001 in PAGE_SEL[3:0] field of register PAGE_SEL (02h) // Select page 1
4. Write 84h in PAGE_ADDR register (08h) // Set address
5. Write 06h in PAGE_DATA register (09h) // Set value to be written
6. Write bit PAGE_WRITE = 0 in PAGE_RW (17h) register // Write operation disabled
7. Write bit EMB_FUNC_REG_ACCESS = 0 in FUNC_CFG_ACCESS (01h) // Disable access to embedded functions registers

Read procedure example: read value of register at address 84h (PEDO_DEB_STEPS_CONF) in page 1

1. Write bit EMB_FUNC_REG_ACCESS = 1 in FUNC_CFG_ACCESS (01h) // Enable access to embedded functions registers
2. Write bit PAGE_READ = 1 in PAGE_RW (17h) register // Select read operation mode
3. Write 0001 in PAGE_SEL[3:0] field of register PAGE_SEL (02h) // Select page 1
4. Write 84h in PAGE_ADDR register (08h) // Set address
5. Read value of PAGE_DATA register (09h) // Get register value
6. Write bit PAGE_READ = 0 in PAGE_RW (17h) register // Read operation disabled
7. Write bit EMB_FUNC_REG_ACCESS = 0 in FUNC_CFG_ACCESS (01h) // Disable access to embedded functions registers

Note: Steps 1 and 2 of both procedures are intended to be performed at the beginning of the procedure. Steps 6 and 7 of both procedures are intended to be performed at the end of the procedure. If the procedure involves multiple operations, only steps 3, 4 and 5 must be repeated for each operation. If, in particular, the multiple operations involve consecutive registers, only step 5 can be performed.

13 Embedded advanced features register description

13.1 Page 0 - embedded advanced features registers

13.1.1 SFLP_GAME_GBIASX_L (6Eh) and SFLP_GAME_GBIASX_H (6Fh)

SFLP game algorithm X-axis gyroscope bias register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 272. SFLP_GAME_GBIASX_L register

GAME_GBIASX_7	GAME_GBIASX_6	GAME_GBIASX_5	GAME_GBIASX_4	GAME_GBIASX_3	GAME_GBIASX_2	GAME_GBIASX_1	GAME_GBIASX_0

Table 273. SFLP_GAME_GBIASX_L register description

GAME_GBIASX_[7:0]	SFLP game algorithm X-axis gbias: temporary register for gbias setting procedure (LSbyte). Default value: 00000000

Table 274. SFLP_GAME_GBIASX_H register

GAME_GBIASX_15	GAME_GBIASX_14	GAME_GBIASX_13	GAME_GBIASX_12	GAME_GBIASX_11	GAME_GBIASX_10	GAME_GBIASX_9	GAME_GBIASX_8

Table 275. SFLP_GAME_GBIASX_H register description

GAME_GBIASX_[15:8]	SFLP game algorithm X-axis gbias: temporary register for gbias setting procedure (MSbyte). Default value: 00000000

13.1.2 SFLP_GAME_GBIASY_L (70h) and SFLP_GAME_GBIASY_H (71h)

SFLP game algorithm Y-axis gyroscope bias register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 276. SFLP_GAME_GBIASY_L register

GAME_GBIASY_7	GAME_GBIASY_6	GAME_GBIASY_5	GAME_GBIASY_4	GAME_GBIASY_3	GAME_GBIASY_2	GAME_GBIASY_1	GAME_GBIASY_0

Table 277. SFLP_GAME_GBIASY_L register description

GAME_GBIASY_[7:0]	SFLP game algorithm Y-axis gbias: temporary register for gbias setting procedure (LSbyte). Default value: 00000000

Table 278. SFLP_GAME_GBIASY_H register

GAME_GBIASY_15	GAME_GBIASY_14	GAME_GBIASY_13	GAME_GBIASY_12	GAME_GBIASY_11	GAME_GBIASY_10	GAME_GBIASY_9	GAME_GBIASY_8

Table 279. SFLP_GAME_GBIASY_H register description

GAME_GBIASY_[15:8]	SFLP game algorithm Y-axis gbias: temporary register for gbias setting procedure (MSbyte). Default value: 00000000

13.1.3 SFLP_GAME_GBIASZ_L (72h) and SFLP_GAME_GBIASZ_H (73h)

SFLP game algorithm Z-axis gyroscope bias register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Table 280. SFLP_GAME_GBIASZ_L register

GAME_GBIASZ_7	GAME_GBIASZ_6	GAME_GBIASZ_5	GAME_GBIASZ_4	GAME_GBIASZ_3	GAME_GBIASZ_2	GAME_GBIASZ_1	GAME_GBIASZ_0

Table 281. SFLP_GAME_GBIASZ_L register description

GAME_GBIASZ_[7:0]	SFLP game algorithm Z-axis gbias: temporary register for gbias setting procedure (LSbyte). Default value: 00000000

Table 282. SFLP_GAME_GBIASZ_H register

GAME_GBIASZ_15	GAME_GBIASZ_14	GAME_GBIASZ_13	GAME_GBIASZ_12	GAME_GBIASZ_11	GAME_GBIASZ_10	GAME_GBIASZ_9	GAME_GBIASZ_8

Table 283. SFLP_GAME_GBIASZ_H register description

GAME_GBIASZ_[15:8]	SFLP game algorithm Z-axis gbias: temporary register for gbias setting procedure (MSbyte). Default value: 00000000

13.1.4 FSM_QVAR_SENSITIVITY_L (BAh) and FSM_QVAR_SENSITIVITY_L (BBh)

Qvar sensor sensitivity value register for the finite state machine (R/W)

This register corresponds to the conversion value of the Qvar sensor. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

The default value of FSM_QVAR_S_[15:0] bits is 0x1624.

Table 284. FSM_QVAR_SENSITIVITY_L register

FSM_QVAR_S_7	FSM_QVAR_S_6	FSM_QVAR_S_5	FSM_QVAR_S_4	FSM_QVAR_S_3	FSM_QVAR_S_2	FSM_QVAR_S_1	FSM_QVAR_S_0

Table 285. FSM_QVAR_SENSITIVITY_L register description

FSM_QVAR_S_[7:0]	Qvar sensor sensitivity (LSbyte). Default value: 00100100

Table 286. FSM_QVAR_SENSITIVITY_H register

FSM_QVAR_S_15	FSM_QVAR_S_14	FSM_QVAR_S_13	FSM_QVAR_S_12	FSM_QVAR_S_11	FSM_QVAR_S_10	FSM_QVAR_S_9	FSM_QVAR_S_8

Table 287. FSM_QVAR_SENSITIVITY_H register description

FSM_QVAR_S_[15:8]	Qvar sensor (MSbyte). Default value: 00010110

13.2 Page1 - embedded advanced features registers

13.2.1 FSM_LC_TIMEOUT_L (7Ah) and FSM_LC_TIMEOUT_H (7Bh)

FSM long counter timeout register (R/W)

The long counter timeout value is an unsigned integer value (16-bit format). When the long counter value reached this value, the FSM generates an interrupt.

Table 288. FSM_LC_TIMEOUT_L register

FSM_LC_TIMEOUT7	FSM_LC_TIMEOUT6	FSM_LC_TIMEOUT5	FSM_LC_TIMEOUT4	FSM_LC_TIMEOUT3	FSM_LC_TIMEOUT2	FSM_LC_TIMEOUT1	FSM_LC_TIMEOUT0

Table 289. FSM_LC_TIMEOUT_L register description

FSM_LC_TIMEOUT[7:0]	FSM long counter timeout value (LSbyte). Default value: 00000000

Table 290. FSM_LC_TIMEOUT_H register

FSM_LC_TIMEOUT15	FSM_LC_TIMEOUT14	FSM_LC_TIMEOUT13	FSM_LC_TIMEOUT12	FSM_LC_TIMEOUT11	FSM_LC_TIMEOUT10	FSM_LC_TIMEOUT9	FSM_LC_TIMEOUT8

Table 291. FSM_LC_TIMEOUT_H register description

FSM_LC_TIMEOUT[15:8]	FSM long counter timeout value (MSbyte). Default value: 00000000

13.2.2 FSM_PROGRAMS (7Ch)

FSM number of programs register (R/W)

Table 292. FSM_PROGRAMS register

FSM_N_PROG7	FSM_N_PROG6	FSM_N_PROG5	FSM_N_PROG4	FSM_N_PROG3	FSM_N_PROG2	FSM_N_PROG1	FSM_N_PROG0

Table 293. FSM_PROGRAMS register description

FSM_N_PROG[7:0]	Number of FSM programs; must be less than or equal to 8. Default value: 00000000

13.2.3 FSM_START_ADD_L (7Eh) and FSM_START_ADD_H (7Fh)

FSM start address register (R/W). First available address is 0x35C.

Table 294. FSM_START_ADD_L register

FSM_START7	FSM_START6	FSM_START5	FSM_START4	FSM_START3	FSM_START2	FSM_START1	FSM_START0

Table 295. FSM_START_ADD_L register description

FSM_START[7:0]	FSM start address value (LSbyte). Default value: 00000000

Table 296. FSM_START_ADD_H register

FSM_START15	FSM_START14	FSM_START13	FSM_START12	FSM_START11	FSM_START10	FSM_START9	FSM_START8

Table 297. FSM_START_ADD_H register description

FSM_START[15:8]	FSM start address value (MSbyte). Default value: 00000000

13.2.4 PEDO_CMD_REG (83h)

Pedometer configuration register (R/W)

Table 298. PEDO_CMD_REG register

0(1)	0(1)	0(1)	0(1)	CARRY_COUNT_EN	FP_REJECTION_EN	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 299. PEDO_CMD_REG register description

CARRY_COUNT_EN	Set when user wants to generate interrupt only on count overflow event
FP_REJECTION_EN(1)	Enables the false-positive rejection feature

1. *This bit is active when the MLC_EN bit of EMB_FUNC_EN_B (05h) or the MLC_BEFORE_FSM_EN bit in the EMB_FUNC_EN_A (04h) register is set to 1.*

13.2.5 PEDO_DEB_STEPS_CONF (84h)

Pedometer debounce configuration register (R/W)

Table 300. PEDO_DEB_STEPS_CONF register

DEB_ STEP7	DEB_ STEP6	DEB_ STEP5	DEB_ STEP4	DEB_ STEP3	DEB_ STEP2	DEB_ STEP1	DEB_ STEP0

Table 301. PEDO_DEB_STEPS_CONF register description

DEB_STEP[7:0]	Debounce threshold. Minimum number of steps to increment the step counter (debounce). Default value: 00001010

13.2.6 PEDO_SC_DELTAT_L (D0h) and PEDO_SC_DELTAT_H (D1h)

Time period register for step detection on delta time (R/W)

Table 302. PEDO_SC_DELTAT_L register

PD_SC_7	PD_SC_6	PD_SC_5	PD_SC_4	PD_SC_3	PD_SC_2	PD_SC_1	PD_SC_0

Table 303. PEDO_SC_DELTAT_H register

PD_SC_15	PD_SC_14	PD_SC_13	PD_SC_12	PD_SC_11	PD_SC_10	PD_SC_9	PD_SC_8

Table 304. PEDO_SC_DELTAT_H/L register description

PD_SC_[15:0]	Time period value (1LSB = 6.4 ms)

13.2.7 MLC_QVAR_SENSITIVITY_L (E8h) and MLC_QVAR_SENSITIVITY_H (E9h)

Qvar sensor sensitivity value register for the machine learning core (R/W)

This register corresponds to the conversion value of the Qvar sensor. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

The default value of MLC_QVAR_S_[15:0] is 0x3C00.

Table 305. MLC_QVAR_SENSITIVITY_L register

MLC_ QVAR_S_7	MLC_ QVAR_S_6	MLC_ QVAR_S_5	MLC_ QVAR_S_4	MLC_ QVAR_S_3	MLC_ QVAR_S_2	MLC_ QVAR_S_1	MLC_ QVAR_S_0

Table 306. MLC_QVAR_SENSITIVITY_L register description

MLC_QVAR_S_[7:0]	Qvar sensor sensitivity (LSbyte). Default value: 00000000

Table 307. MLC_QVAR_SENSITIVITY_H register

MLC_ QVAR_S_15	MLC_ QVAR_S_14	MLC_ QVAR_S_13	MLC_ QVAR_S_12	MLC_ QVAR_S_11	MLC_ QVAR_S_10	MLC_ QVAR_S_9	MLC_ QVAR_S_8

Table 308. MLC_QVAR_SENSITIVITY_H register description

MLC_QVAR_S_[15:8]	Qvar sensor sensitivity (MSbyte). Default value: 00111100

14 Soldering information

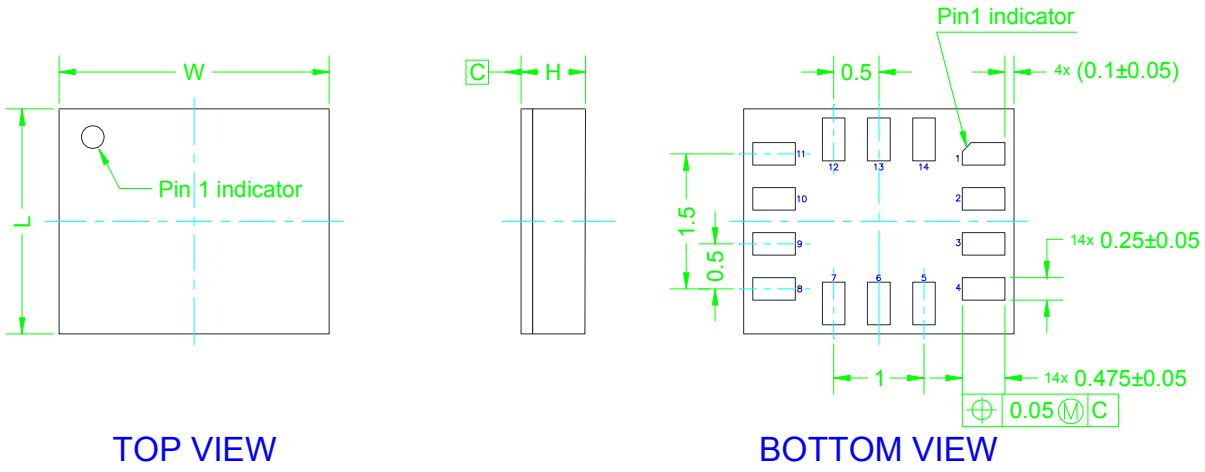
The LGA package is compliant with the ECOPACK and RoHS standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.
For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

15 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

15.1 LGA-14L package information

Figure 31. LGA-14L 2.5 x 3.0 x 0.74 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General tolerance is +/-0.1mm unless otherwise specified

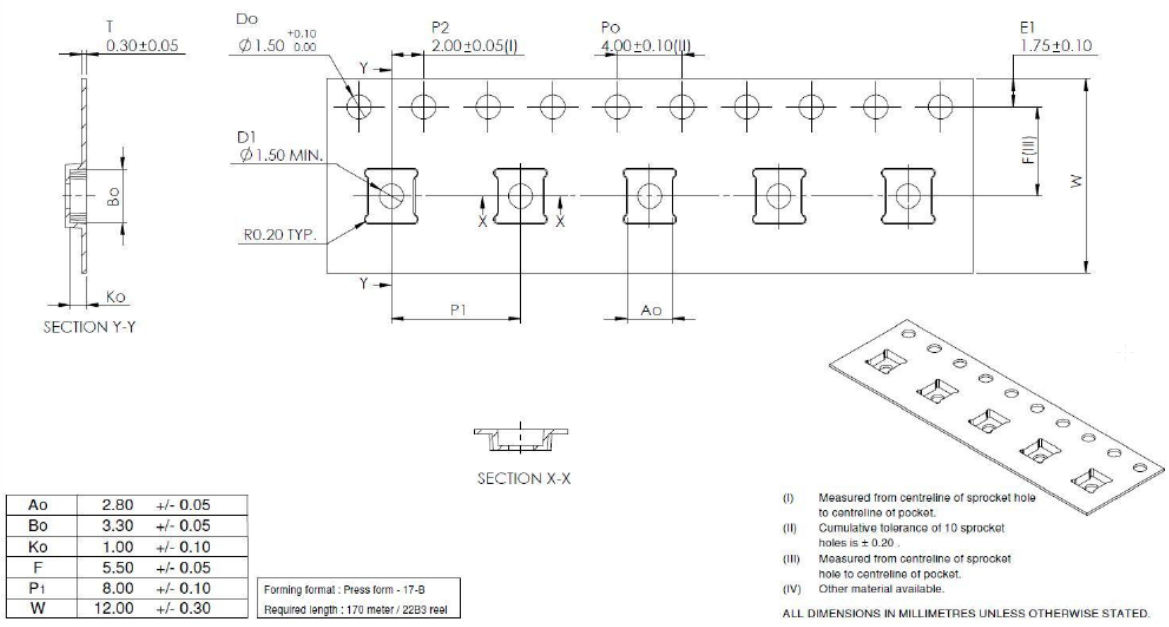
OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.50	±0.1
Width [W]	3.00	±0.1
Height [H]	0.74	MAX

DM00747677_3

15.2 LGA-14 packing information

Figure 32. **Carrier tape information for LGA-14 package**



Ao	2.80	+/- 0.05
Bo	3.30	+/- 0.05
Ko	1.00	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Forming format : Press form - 17-B
Required length : 170 meter / 22B3 reel

Figure 33. **LGA-14 package orientation in carrier tape**

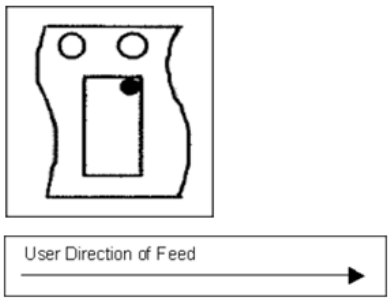


Figure 34. **Reel information for carrier tape of LGA-14 package**

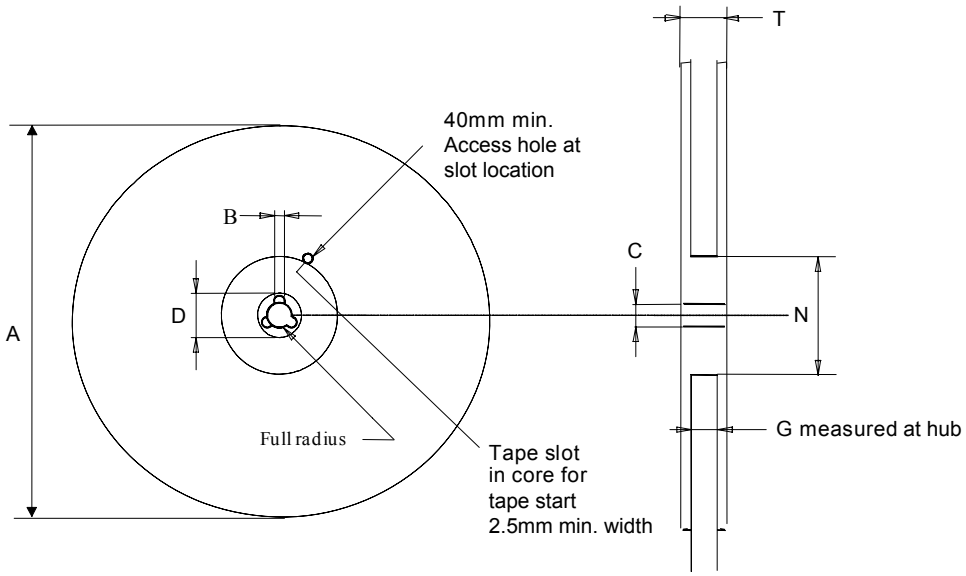


Table 309. **Reel dimensions for carrier tape of LGA-14 package**

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

Revision history

Table 310. **Document revision history**

Date	Revision	Changes
13-May-2022	1	Initial release
06-Jul-2022	2	First public release

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