# High Voltage Surge Stopper

## FEATURES

- **Rugged Floating Topology**
- **Wide Operating Voltage Range: 9V to >500V**
- Adjustable Output Clamp Voltage
- Controls N-Channel MOSFET
- Adjustable Protection Timer
- Internal 9-Second Cool-Down Timer
- Shutdown $I_Q$ < 14µA
- 8-Lead TSOT and 3mm × 2mm DFN Packages

## APPLICATIONS

- Industrial, Automotive and Avionic Surge Protection
- High Voltage DC Distribution
- 28V Vehicle Systems

## DESCRIPTION

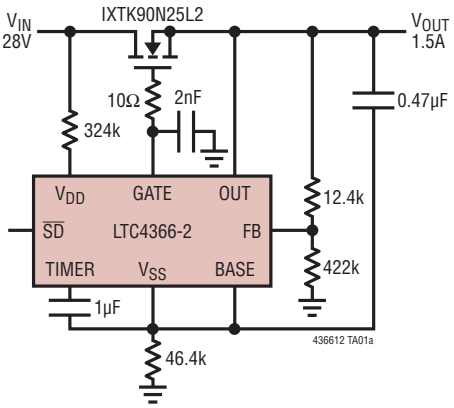
The LTC®4366 surge stopper protects loads from high voltage transients. By controlling the gate of an external N-channel MOSFET, the LTC4366 regulates the output during an overvoltage transient. The load may remain operational while the overvoltage is dropped across the MOSFET. Placing a resistor in the return line isolates the LTC4366 and allows it to float up with the supply; therefore, the upper limit on the output voltage depends only on the availability of high valued resistors and MOSFET ratings.

An adjustable overvoltage timer prevents MOSFET damage during the surge while an additional 9-second timer provides for MOSFET cool down. A shutdown pin reduces the quiescent current to less than 14µA during shutdown. After a fault the LTC4366-1 latches off while the LTC4366-2 will auto-retry.

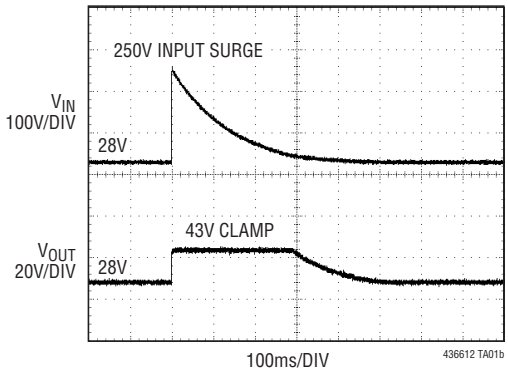
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## TYPICAL APPLICATION

**Overvoltage Protected 1.5A, 28V Supply**




**Overvoltage Protector Regulates Output at 43V During Transient**



## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2) All voltages relative to $V_{SS}$, unless otherwise noted.**

Supply Voltage ($V_{DD}$) ..... –0.3V to 10V
Supply Voltage (OUT) ..... –0.3V to 5V
Input Voltages
- FB ..... –0.3V to OUT + 0.3V
- TIMER ..... –0.3V to 3.5V
- $\overline{SD}$ ..... –0.3V to 10V

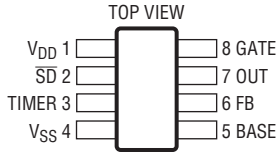
Output Voltages
- BASE ..... –1.5V to 4V
- OUT – BASE ..... –0.3V to 5.5V
- GATE (Note 3) ..... –0.3V to 15V
- GATE – OUT (Note 3) ..... –0.3V to 10V

Currents
- $I_{VDD}$ ..... 10mA
- $I_{OUT}$ ..... 10mA
- BASE ..... –300µA to 10µA
- $\overline{SD}$ ..... –10mA to 10µA

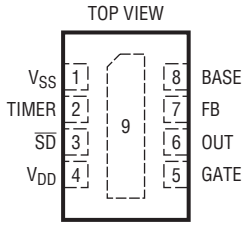
Operating Ambient Temperature Range (Note 4)
- LTC4366C ..... 0°C to 70°C
- LTC4366I ..... –40°C to 85°C
- LTC4366H ..... –40°C to 125°C
- LTC4366MP ..... –55°C to 125°C

Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
- TSOT-23 Package Only ..... 300°C

## PIN CONFIGURATION




TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 195°C/W




DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
$T_{JMAX}$ = 150°C,
$\theta_{JA}$ = 75°C/W IF $V_{SS}$ IS SOLDERED TO PCB, $\theta_{JA}$ = 135°C/W IF $V_{SS}$ IS NOT SOLDERED TO PCB
EXPOSED PAD (PIN 9), PCB $V_{SS}$ CONNECTION OPTIONAL

# ORDER INFORMATION

**Lead Free Finish**

| TAPE AND REEL (MINI) | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC4366CTS8-1#TRMPBF | LTC4366CTS8-1#TRPBF | LTFMC | 8-Lead Plastic TSOT-23 | 0°C to 70°C |
| LTC4366ITS8-1#TRMPBF | LTC4366ITS8-1#TRPBF | LTFMC | 8-Lead Plastic TSOT-23 | –40°C to 85°C |
| LTC4366HTS8-1#TRMPBF | LTC4366HTS8-1#TRPBF | LTFMC | 8-Lead Plastic TSOT-23 | –40°C to 125°C |
| LTC4366CDDB-1#TRMPBF | LTC4366CDDB-1#TRPBF | LFMD | 8-Lead (3mm × 2mm) Plastic DFN | 0°C to 70°C |
| LTC4366IDDB-1#TRMPBF | LTC4366IDDB-1#TRPBF | LFMD | 8-Lead (3mm × 2mm) Plastic DFN | –40°C to 85°C |
| LTC4366HDDB-1#TRMPBF | LTC4366HDDB-1#TRPBF | LFMD | 8-Lead (3mm × 2mm) Plastic DFN | –40°C to 125°C |
| LTC4366CTS8-2#TRMPBF | LTC4366CTS8-2#TRPBF | LTFMF | 8-Lead Plastic TSOT-23 | 0°C to 70°C |
| LTC4366ITS8-2#TRMPBF | LTC4366ITS8-2#TRPBF | LTFMF | 8-Lead Plastic TSOT-23 | –40°C to 85°C |
| LTC4366HTS8-2#TRMPBF | LTC4366HTS8-2#TRPBF | LTFMF | 8-Lead Plastic TSOT-23 | –40°C to 125°C |
| LTC4366CDDB-2#TRMPBF | LTC4366CDDB-2#TRPBF | LFMG | 8-Lead (3mm × 2mm) Plastic DFN | 0°C to 70°C |
| LTC4366IDDB-2#TRMPBF | LTC4366IDDB-2#TRPBF | LFMG | 8-Lead (3mm × 2mm) Plastic DFN | –40°C to 85°C |
| LTC4366HDDB-2#TRMPBF | LTC4366HDDB-2#TRPBF | LFMG | 8-Lead (3mm × 2mm) Plastic DFN | –40°C to 125°C |
| LTC4366MPTS8-1#TRMPBF | LTC4366MPTS8-1#TRPBF | LTFMC | 8-Lead Plastic TSOT-23 | –55°C to 125°C |
| LTC4366MPTS8-2#TRMPBF | LTC4366MPTS8-2#TRPBF | LTFMF | 8-Lead Plastic TSOT-23 | –55°C to 125°C |
| LTC4366MPDDB-1#TRMPBF | LTC4366MPDDB-1#TRPBF | LFMD | 8-Lead (3mm × 2mm) Plastic DFN | –55°C to 125°C |
| LTC4366MPDDB-2#TRMPBF | LTC4366MPDDB-2#TRPBF | LFMG | 8-Lead (3mm × 2mm) Plastic DFN | –55°C to 125°C |

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. All voltages relative to $V_{SS}$, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **$V_{DD}$ Regulator** | | | | | | | |
| $V_{Z(VDD)}$ | $V_{DD}$ Shunt Regulator Voltage | I = 1mA | ● | 11.5 | 12 | 12.5 | V |
| $\Delta V_{Z(VDD)}$ | $V_{DD}$ Shunt Regulator Load Regulation | I = 1mA to 5mA LTC4366C/I/H<br>LTC4366MP | ●<br>● | | 30<br>30 | 90<br>130 | mV<br>mV |
| $V_{DD}$ | $V_{DD}$ Supply Voltage (Note 3) | | ● | 4.5 | | $V_{Z(VDD)}$ | V |
| $I_{VDD(STLO)}$ | $V_{DD}$ Pin Current – Start-Up, Gate Low | GATE = 0V, $V_{DD}$ = 7V, OUT = 0V | ● | | 15 | 23 | µA |
| $I_{VDD(STHI)}$ | $V_{DD}$ Pin Current – Start-Up, Gate High | GATE Open, $V_{DD}$ = 7V, OUT = 0V | ● | | 9 | 13 | µA |
| $I_{VDD(SD)}$ | $V_{DD}$ Pin Current – Shutdown | $V_{DD}$ = 7V, OUT = 0V | ● | | 5 | 8 | µA |
| **OUT Regulator** | | | | | | | |
| $V_{Z(OUT)}$ | OUT Shunt Regulator Voltage | I = 1mA, BASE = 0V | ● | 5.0 | 5.7 | 6.0 | V |
| $\Delta V_{Z(OUT)}$ | OUT Shunt Regulator Load Regulation | I = 1mA to 5mA | ● | | 30 | 70 | mV |
| OUT | OUT Supply Voltage (Note 3) | | ● | 3.0 | | $V_{Z(OUT)}$ | V |
| $V_{UVLO1}$ | OUT Undervoltage Lockout 1 | Rising LTC4366C/I/H<br>LTC4366MP | ●<br>● | 2.42<br>2.42 | 2.55<br>2.55 | 2.75<br>2.80 | V<br>V |
| $\Delta V_{UVH1}$ | OUT Undervoltage Lockout 1 Hysteresis | | ● | 0.2 | 0.28 | 0.4 | V |
| $V_{UVLO2}$ | OUT Undervoltage Lockout 2 | Rising | ● | 4.5 | 4.75 | 4.9 | V |
| $\Delta V_{UVH2}$ | OUT Undervoltage Lockout 2 Hysteresis | | ● | 0.3 | 0.4 | 0.5 | V |
| $I_{OUT(AMP)}$ | OUT Pin Current – Regulation Amplifier On | | ● | | 37 | 54 | µA |
| $I_{OUT(CP)}$ | OUT Pin Current – Charge Pump On | | ● | | 150 | 220 | µA |
| $I_{OUT(SD)}$ | OUT Pin Current – Shutdown | | ● | | 3 | 6 | µA |
| **BASE, $V_{SS}$** | | | | | | | |
| $V_{Z(BASE)}$ | BASE Shunt Regulator Voltage (OUT – BASE) | I = –10µA, OUT = 4.5V | ● | 5.5 | 6.2 | 6.6 | V |
| $\Delta V_{Z(BASE)}$ | BASE Shunt Regulator Load Regulation | I = –10µA to –80µA, OUT = 4.5V | ● | | 125 | 200 | mV |
| $I_{BASE}$ | BASE Pin Leakage Current | OUT = 4.5V, BASE = –0.5V | ● | –0.1 | –0.8 | –5.5 | µA |
| $I_{VSS(AMP)}$ | $V_{SS}$ Pin Current – Regulation Amplifier On | | ● | –30 | –45 | –72 | µA |
| $I_{VSS(CP)}$ | $V_{SS}$ Pin Current – Charge Pump On | | ● | –108 | –160 | –230 | µA |
| $I_{VSS(SD)}$ | $V_{SS}$ Pin Current – Shutdown | | ● | | –7 | –12 | µA |
| **GATE Drive** | | | | | | | |
| $\Delta V_{GATE}$ | External N-Channel Gate Drive (GATE – OUT) | OUT = 4.9V, I = 0, –1µA | ● | 11.2 | 12 | 12.5 | V |
| $I_{GATE(ST)}$ | GATE Pin Current – Start-Up | GATE = OUT = 0V LTC4366C/I/H<br>LTC4366MP | ●<br>● | –4.5<br>–3.2 | –7.5<br>–7.5 | –11<br>–11 | µA<br>µA |
| $I_{GATE(CP)}$ | GATE Pin Current – Charge Pump On | GATE = 5V, OUT = 4.9V | ● | –14 | –20 | –28 | µA |
| $I_{GATE(FD)}$ | GATE Pin Current – Fast Discharge | GATE = 10V, OUT = 4.9V | ● | 122 | 200 | 300 | mA |
| $I_{GATE(FLT)}$ | GATE Pin Current – Fault | GATE = 10V, OUT = 4.9V | ● | 0.3 | 0.7 | 1.2 | mA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. All voltages relative to $V_{SS}$, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **FB, $\overline{SD}$, TIMER** | | | | | | | | |
| $V_{FB(REG)}$ | 3% FB pin Regulation Threshold (OUT – FB) | | | ● | 1.193 | 1.23 | 1.267 | V |
| $I_{FB}$ | FB Pin Leakage Current | OUT – FB = 1.2V | | ● | | 0 | ±1 | µA |
| $V_{\overline{SD}(TH)}$ | $\overline{SD}$ Pin Threshold Voltage ($V_{DD}$ – $\overline{SD}$) | Falling | | ● | 1.0 | 1.5 | 2.3 | V |
| $V_{\overline{SD}(HYST)}$ | $\overline{SD}$ Pin Hysteresis | | LTC4366C/I/H<br>LTC4366MP | ●<br>● | 147<br>129 | 280<br>280 | 530<br>530 | mV<br>mV |
| $I_{\overline{SD}}$ | $\overline{SD}$ Pin Input Pull-Up Current | $V_{DD}$ – $\overline{SD}$ = 0.7V | LTC4366C/I/H<br>LTC4366MP | ●<br>● | –0.7<br>–0.5 | –1.6<br>–1.6 | –3.5<br>–3.5 | µA<br>µA |
| $V_{TIMER(H)}$ | TIMER Pin Threshold | TIMER Rising, $V_{DD}$ = 7V, OUT = $V_{Z(OUT)}$ | | ● | 2.6 | 2.8 | 3.1 | V |
| $I_{TIMER(UP)}$ | TIMER Pin Pull-Up Current | TIMER = 1V | LTC4366C/I/H<br>LTC4366MP | ●<br>● | –5.1<br>–4 | –9<br>–9 | –13<br>–13 | µA<br>µA |
| $I_{TIMER(DN)}$ | TIMER Pin Pull-Down Current | TIMER = 1V | LTC4366C/I/H<br>LTC4366MP | ●<br>● | 0.9<br>0.7 | 1.8<br>1.8 | 2.8<br>2.8 | µA<br>µA |
| $I_{TIMER(RATIO)}$ | TIMER Pin Current Ratio $I_{TIMER(DN)}/I_{TIMER(UP)}$ | | | ● | 15 | 20 | 25 | % |
| **AC Characteristics** | | | | | | | | |
| $t_{DLY-\overline{SD}}$ | $\overline{SD}$ Low to Gate Low Filter Time | Step $V_{DD}$ – $\overline{SD}$ from 0V to 3V | | ● | 420 | 700 | 1200 | µs |
| $t_{DLY-FAST}$ | FB Low to Gate Low Delay Time | Step OUT – FB from 0V to 1.3V | | ● | 60 | 150 | 300 | ns |
| $t_{D(COOL)}$ | Cool-Down Timer (Internal) | $V_{DD}$ = $V_{Z(VDD)}$ | LTC4366C/I/H<br>LTC4366MP | ●<br>● | 5.9<br>5.9 | 9<br>9 | 16<br>19 | Seconds<br>Seconds |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into pins are positive.

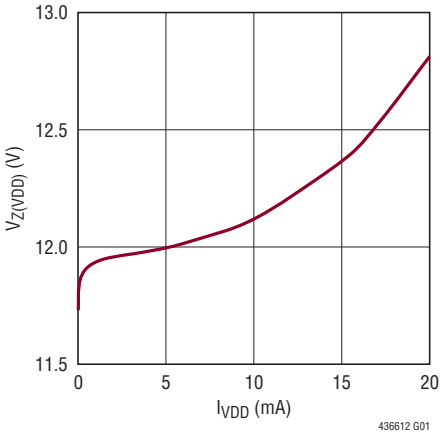
**Note 3:** Limits on the maximum rating is defined as whichever limit occurs first. An internal clamp limits the GATE pin to a maximum of 12V above source. Driving this pin to voltages beyond the clamp may damage the device.

**Note 4:** $T_J$ is calculated from the ambient temperature, $T_A$, and power dissipation, $P_D$, according to the formula:

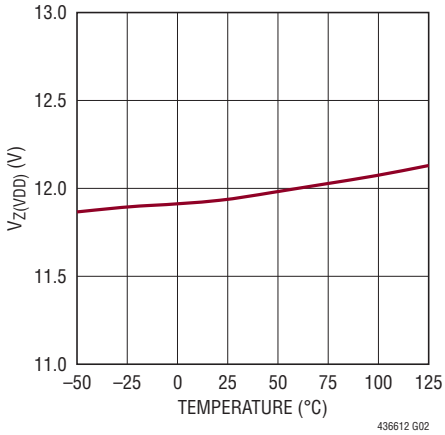
$$T_J = T_A + (P_D \bullet \theta_{JA})$$

## TYPICAL PERFORMANCE CHARACTERISTICS

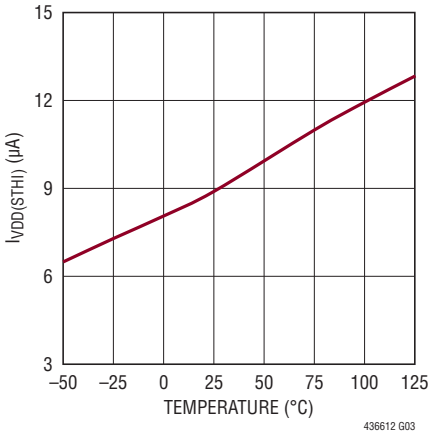
**$V_{DD}$ Shunt Regulator vs $V_{DD}$ Current**



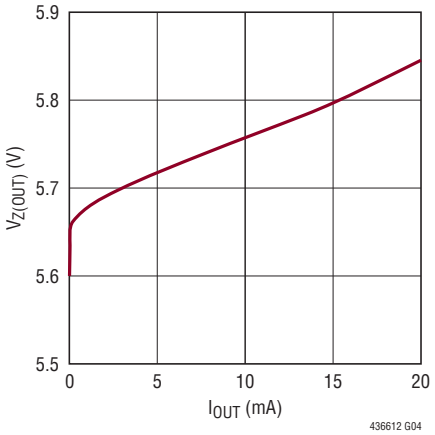

**$V_{DD}$ Shunt Regulator vs Temperature**



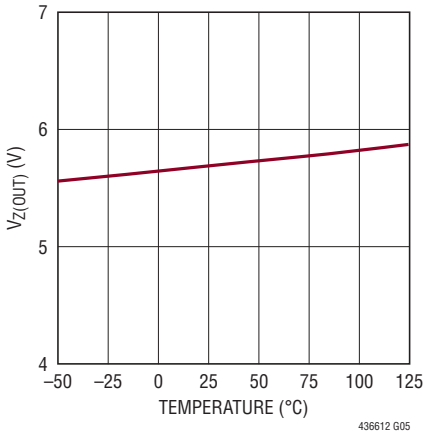

**$V_{DD}$ Start-Up Current vs Temperature (Gate High)**



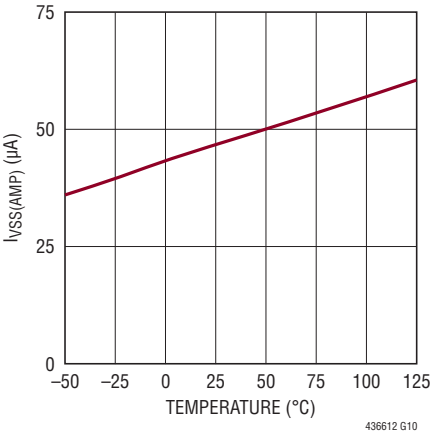

**OUT Shunt Regulator vs OUT Current**



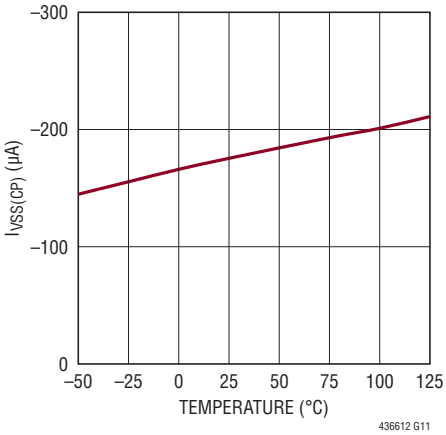

**OUT Shunt Regulator vs Temperature**



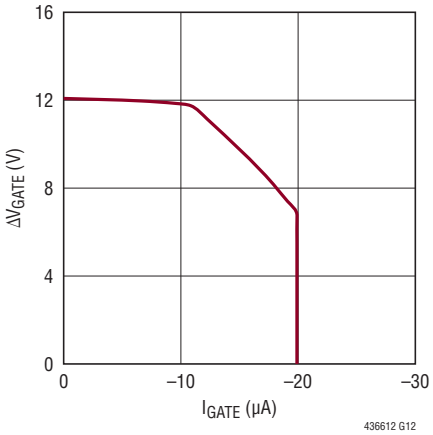

**$V_{SS}$ Current (Regulation AMP On) vs Temperature**



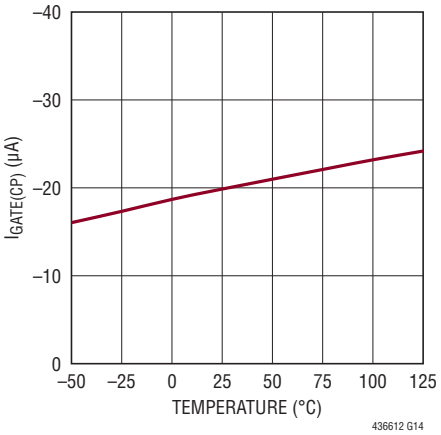

**$V_{SS}$ Current (Charge Pump On) vs Temperature**




**Gate Drive vs Gate Pull-Up Current**

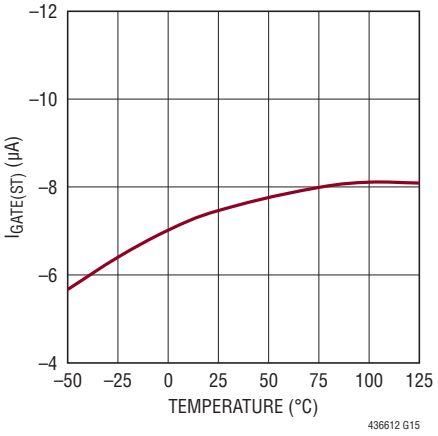



**Gate Current (Charge Pump On) vs Temperature**

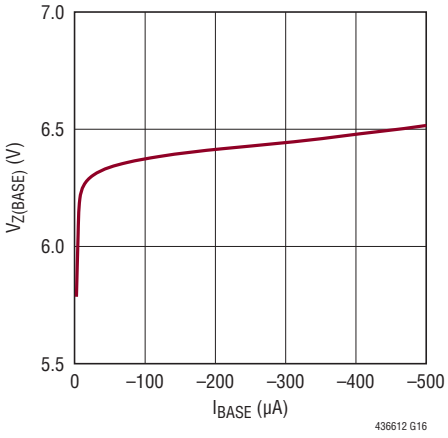


# TYPICAL PERFORMANCE CHARACTERISTICS

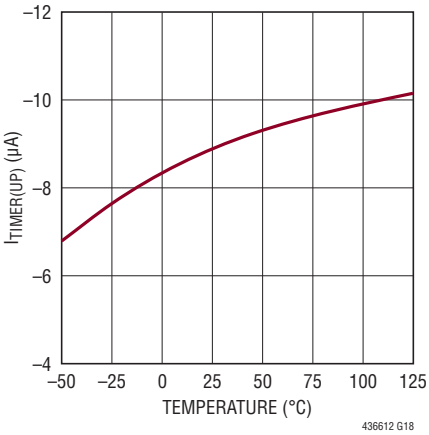
### Gate Start-Up Current vs Temperature



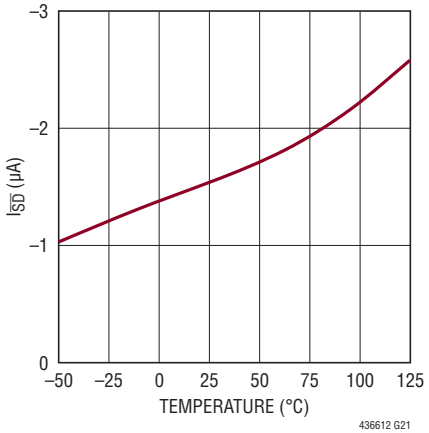

### Base Shunt Regulator vs Base Current



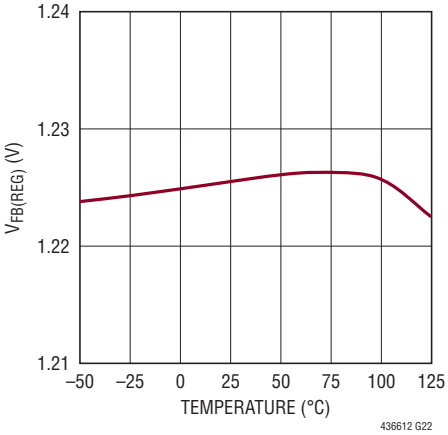

### Timer Pull-Up Current vs Temperature



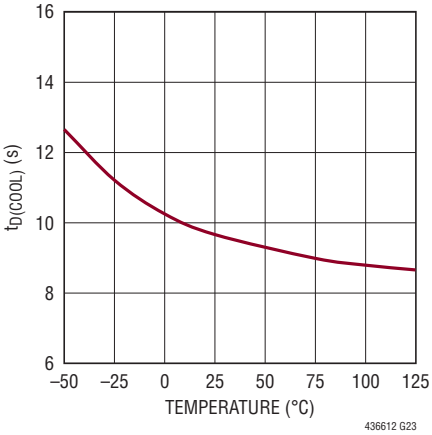

### $\overline{SD}$ Pull-Up Current vs Temperature




### FB Regulation Threshold vs Temperature




### Cool-Down Time vs Temperature



## PIN FUNCTIONS

**BASE:** Base Driver Output for External PNP Shunt Regulator. This pin is connected to the anode of an internal 6.2V Zener with the cathode tied to OUT. In cases where lower Zener (Z3) clamp current is desired but a large $V_{SS}$ resistor is prohibited, connect an external PNP base to this pin (PNP collector is grounded, emitter is tied to $V_{SS}$). Tie this pin to $V_{SS}$ if unused.

**Exposed Pad:** The exposed pad may be left open or connected to $V_{SS}$.

**FB:** Overvoltage Regulation Amplifier Feedback Input. Connect this pin to an external resistive divider from OUT to ground. The overvoltage regulation amplifier controls the gate of the external N-channel MOSFET to regulate the FB pin voltage at 1.23V below OUT. The overvoltage amplifier will activate a 200mA pull-down on the GATE pin during a fast overvoltage event.

**GATE:** Gate Drive for External N-Channel MOSFET. During start-up an internal 7.5µA current source charges the gate of the external N-channel MOSFET from the $V_{DD}$ pin. Once the OUT voltage is above $V_{SS}$ by 4.75V, the charge pump will finish charging the GATE to 12V above OUT. During a fast overvoltage event, a 200mA pull-down current source between GATE and OUT is activated, followed by regulation of the GATE pin voltage by the overvoltage regulation amplifier.

**OUT:** Charge Pump and Overvoltage Regulation Amplifier Supply Voltage. Supply input for floating circuitry powered from the MOSFET source. Once the OUT voltage is 4.75V (UVLO2) above $V_{SS}$, the charge pump will turn on and draw power from this pin. When OUT exceeds 2.55V (UVLO1) it is used as a power supply and reference input for overvoltage regulation amplifier. This pin is clamped at 5.7V and requires a 0.22µF or greater bypass to the $V_{SS}$ pin.

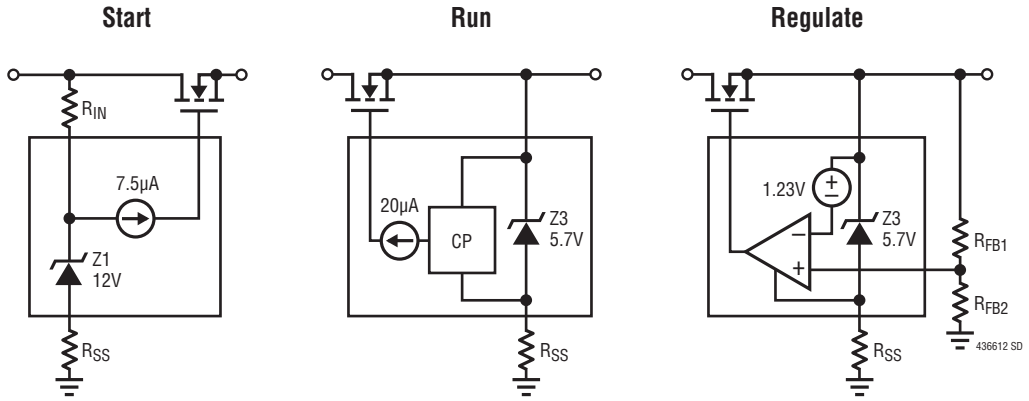
**$\overline{SD}$:** Shutdown Comparator Input. Tie to $V_{DD}$ if unused. Connect pin to a limited current pull down created by adding a resistor in series with an open-drain or open-collector pull-down transistor. Activating the external pull down overcomes the internal 1.6µA pull-up current source and allows the $\overline{SD}$ pin to cross the shutdown threshold. This threshold is defined as 1.5V below $V_{DD}$ with a 280mV hysteresis. To prevent false triggers this pin must stay below the threshold for 700µs to activate the shutdown state. The shutdown state lowers the total quiescent current ($I_{VDD}$ plus $I_{OUT}$) below 20µA. This quiescent current does not include shunt current in the $V_{DD}$, OUT and BASE regulators. After a fault on the LTC4366, putting the part in shutdown will clear the fault and allow operation to resume. Clearing the fault during the 9-second cool-down period will shorten the timeout for the LTC4366-2 (auto-retry) version.

**TIMER:** Timer Input. Leave this pin open for a 1µs overvoltage regulation period before fault off. Connect a capacitor between this pin and $V_{SS}$ to set a 311ms/µF duration for overvoltage regulation before the switch is turned off. The LTC4366-2 version will restart after a nine second cool-down period.

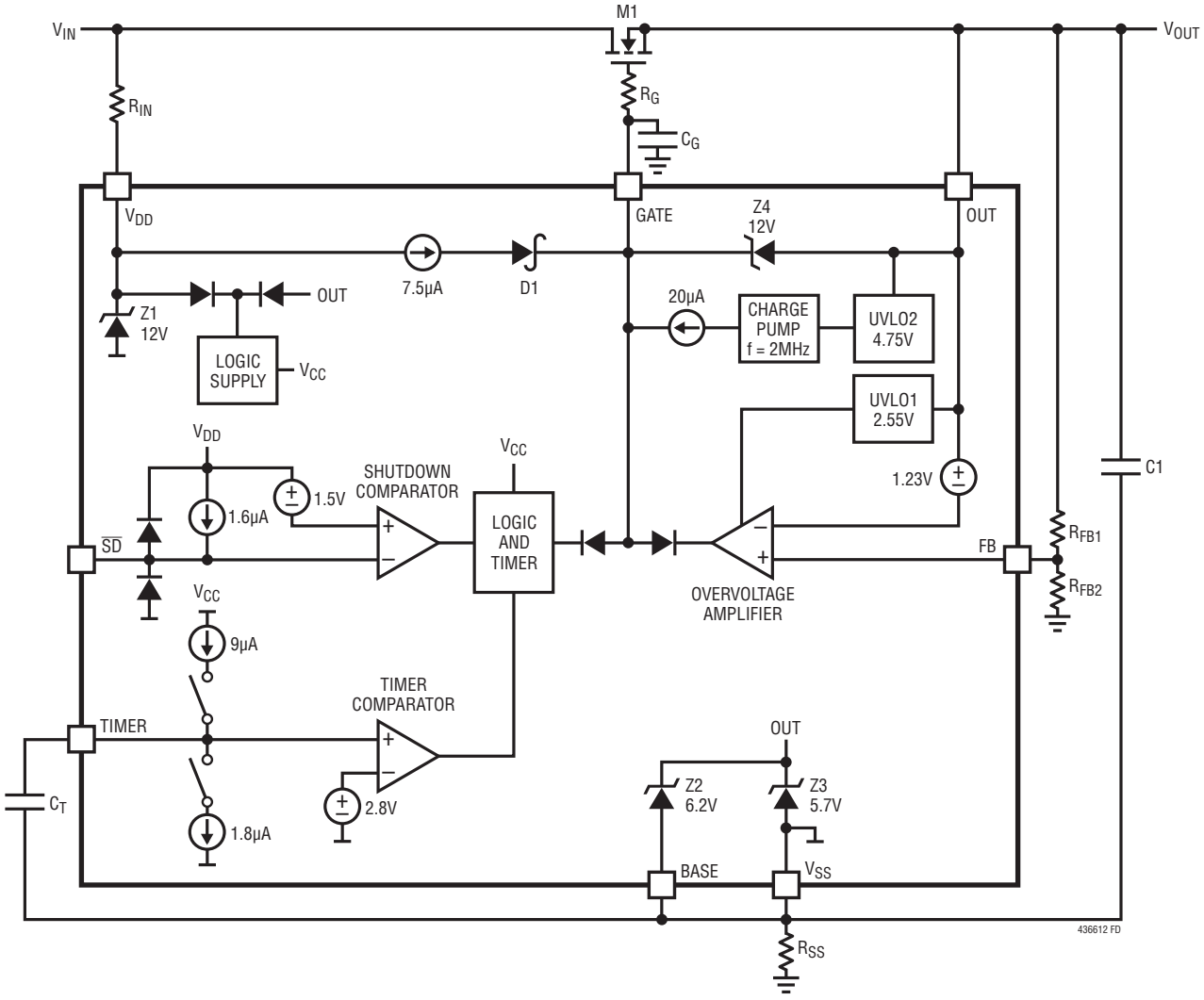
**$V_{DD}$:** Start-Up Supply. Supply input for 7.5µA start-up current source that charges the gate of the external N-channel MOSFET. Also provides supply for timer and logic circuits active when the external MOSFET is off. This pin is clamped at 12V above $V_{SS}$. Do not bypass this pin with a capacitor.

**$V_{SS}$:** Device Return and Substrate. The capacitors on the TIMER and OUT pins should be returned to this pin.

## SIMPLIFIED DIAGRAM




## FUNCTIONAL DIAGRAM



## OPERATION

The Simplified Diagram shows three states of operation: the start, run and regulate mode. Previous surge stopper parts are powered off the input supply, therefore the surge voltage is limited to the breakdown voltage of the input pins of the part. As demonstrated in run and regulate modes, the majority of this part is powered off the output, so the MOSFET isolates the surge from the power pins of the part. This allows surge voltages up to the breakdown of the external MOSFET.

In the start mode a 15µA trickle current flows through $R_{IN}$, half is used to charge the gate with the other half used as bias current. As the GATE pin charges, the external MOSFET brings up the OUT pin. This leads to the run mode where the output is high enough to become a supply voltage for the charge pump. The charge pump is then used to fully charge the gate 12V above the source.

With the output voltage equal to the input voltage, it is necessary to protect the load from an input supply overvoltage. In the regulate mode, the overvoltage regulation amplifier is referenced to the output through a 1.23V reference. If the voltage drop across the upper feedback resistor, $R_{FB1}$, exceeds 1.23V the regulation amplifier pulls the gate down to regulate the $R_{FB1}$ voltage back to 1.23V. Therefore, the output voltage is clamped by setting the proper ratio between $R_{FB1}$ and $R_{FB2}$.

For example, if the output voltage is regulated at 100V then the voltage drop across the $R_{FB2}$ is 98.77V. If the Zener Z3 is 5.7V then the voltage drop across $R_{SS}$ is 94.3V. Therefore, when the output is at a high voltage, the majority of the voltage is dropped across the two resistors $R_{FB2}$ and $R_{SS}$. This demonstrates how the LTC4366 floats up with the supply. The adjustable 3-terminal regulators, such as the LT®1085 and LM117, are also based on this idea.

The Functional Diagram shows the actual circuits. An external $R_{IN}$ resistor on the $V_{DD}$ pin powers up the 12V shunt regulator which then powers up logic supply, $V_{CC}$. After verifying that the shutdown input is not active, the GATE pin is charged with a 7.5µA current from $V_{DD}$. This is the start mode.

Once the OUT to $V_{SS}$ voltage exceeds the 2.55V UVLO1 threshold, the overvoltage amplifier is enabled. Next, the UVLO2 threshold of 4.75V is crossed and the charge pump turns on. The charge pump charges the GATE pin with 20µA to its final value 12V above OUT (clamped by Z4). This allows the capacitor between OUT and $V_{SS}$ to charge until clamped by Z3 to 5.7V. In this run mode the MOSFET is configured as a low resistance pass transistor with little voltage drop and power dissipation in the MOSFET.

The powered up LTC4366 is now ready to protect the load against an overvoltage transient. The overvoltage regulation amplifier monitors the load voltage between OUT and ground by sensing the voltage on the FB pin with respect to the OUT pin (drop across $R_{FB1}$). In an overvoltage condition the OUT rises until the amplifier drives the M1 gate to regulate and limit the output voltage. This is the regulate mode.

During regulation the excess voltage is dropped across the MOSFET. To prevent overheating the MOSFET, the LTC4366 limits the overvoltage regulation time using the TIMER pin. The TIMER pin is charged with 9µA until the pin exceeds 2.8V. At that point an overvoltage fault is set, the MOSFET is turned off, and the part enters a cool-down period of 9 seconds. The logic and timer block are active during cool down while the GATE pin is pulled to OUT.

The latched-off version, LTC4366-1, will remain in fault until the $\overline{SD}$ pin is toggled low and then high. Once the fault is cleared, the GATE is permitted to turn the MOSFET on again. The auto-retry version, LTC4366-2, waits 9 seconds then clears the fault and restarts.

## APPLICATIONS INFORMATION

The typical LTC4366 application is a protected system that distributes power to loads safe from overvoltage transients. External component selection is discussed in the following sections.

### Dual Shunt Regulators

The LTC4366 uses two shunt regulators coupled with the external voltage dropping resistors, $R_{SS}$ and $R_{IN}$, to generate internal supply rails at the $V_{DD}$ and OUT pins. These shunt-regulated rails allow overvoltage protection from unlimited high voltage transients irrespective of the voltage rating of the LTC4366's internal circuitry.

At the beginning of start-up, during shutdown, or after an overvoltage fault, the GATE pin is clamped to the OUT pin thereby shutting off the MOSFET. This allows the $V_{SS}$ and OUT pins to be pulled to ground by output load and $R_{SS}$. Under this condition the $V_{DD}$ pin is clamped with a 12V shunt regulator to $V_{SS}$. The full supply voltage minus 12V is then impressed on the $R_{IN}$ resistor which sets the shunt current. The shunt current can be as high as 10mA which is several orders of magnitude higher than the typical 9µA $V_{DD}$ pin quiescent current.

In normal operation the OUT voltage is equal to the input supply. With C1 fully charged $I_{C1}$ is zero at this point. Under this condition the voltage between the OUT and $V_{SS}$ pins are clamped with a 5.7V shunt regulator. The input supply voltage minus 5.7V is impressed on $R_{SS}$. The $R_{SS}$ current is divided into three areas: the 5.7V shunt current, bias current between OUT and $V_{SS}$ and finally the $R_{IN}$ current. The 5.7V shunt current can be as high as 10mA which greatly exceeds the typical OUT (160µA) bias current.

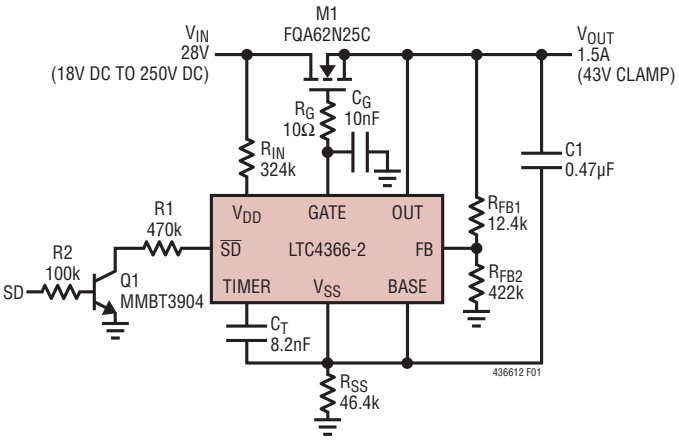



**Figure 1. Typical Application**

### Turn-On Sequence

The voltage between the $V_{DD}$ and $V_{SS}$ pins is shunt regulated to 12V after ramping up the input supply. Next, the internally generated supply, $V_{CC}$, produces a 30µs power-on-reset pulse which clears the fault latch and initializes internal latches. Next, the shutdown comparator determines if the $\overline{SD}$ pin is externally pulled low, thereby requesting a low bias current shutdown state. Otherwise the external MOSFET, M1, is allowed to turn on.

Turning on the 7.5µA GATE pull-up current source from the $V_{DD}$ pin begins what can be described as a "bootstrapped" method for powering up the MOSFET gate. Once the GATE reaches the $V_{DD}$ pin voltage (minus a Schottky diode), the 7.5µA source loses voltage headroom and stops charging the GATE (middle of waveforms in Figure 2.). The bootstrap method relies on charging C1 to a sufficient voltage after GATE stops increasing. The voltage on C1 is then used as a supply for a charge pump that charges the gate to its final value 12V above OUT. C1 will discharge if the charge pump current exceeds the C1 charging current. If the voltage drops below 4.35V, the charge pump will pause allowing C1 to recharge.

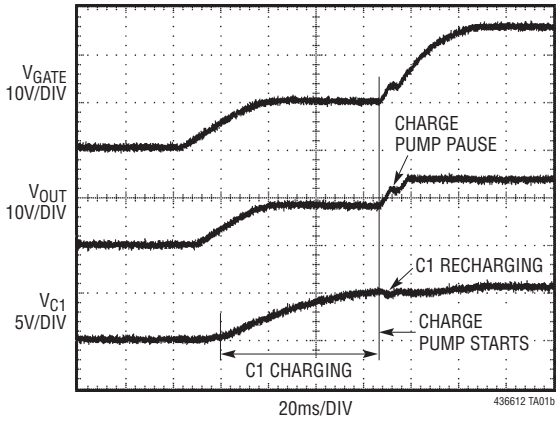



**Figure 2. Turn-On Waveforms**

## APPLICATIONS INFORMATION

Starting up with a supply voltage insufficient to charge C1 with large load current may result in overheating the MOSFET and subsequent damage. While the gate and output are ramping the drop across the MOSFET is the input supply minus the output. If the supply is lower than necessary to charge C1, then the output fails to ramp higher than the supply minus the threshold of the MOSFET. This 3V to 5V MOSFET drop with high load current will result in power dissipation without any protection or timeout limit.

### Overvoltage Fault

The LTC4366 prevents an overvoltage on the input supply from reaching the load. Normally, the pass transistor is fully on, powering the load with very little voltage drop. As the input voltage increases the OUT voltage increases until it reaches the regulation point ($V_{REG}$). From that point any further voltage increase is dropped across the MOSFET. Note the MOSFET is still on so the LTC4366 allows uninterrupted operation during a short overvoltage event.

The $V_{REG}$ point is configured with the two FB resistors, $R_{FB1}$ and $R_{FB2}$. The regulation amplifier compares the FB pin to a threshold 1.23V below the OUT pin. During regulation the drop across $R_{FB1}$ is 1.23V, while the remainder of the $V_{REG}$ voltage is dropped across $R_{FB2}$.

When the output is at the regulation point a timer is started to prevent excessive power dissipation in the MOSFET. Normally the TIMER pin is held low with a 1.8µA pull-down current. During regulation the TIMER pin charges with 9µA. If the regulation point is held long enough for the TIMER pin to reach 2.8V then an overvoltage fault is latched. The equation for setting the timer capacitor is:

$$C_T = 3.2 \bullet t[nF/ms]$$

Depending on which version, the part will cool down and self start (LTC4366-2), or remain latched off until the $\overline{SD}$ pin activates a shutdown followed by a start-up command (LTC4366-1). The cool-down time is typically nine seconds which provides a very low pulsed power duty cycle.

Starting up with an input supply overvoltage and full load current does increase the power dissipation in the MOSFET well beyond the case for an overvoltage surge. During the gate and output ramp up, the partial supply voltage (at full current) is dropped across the MOSFET. After start-up the normal overvoltage surge (with timeout) occurs before the shutting off the MOSFET. The Design Example section only considers the normal overvoltage surge for safe operating area (SOA) calculations for the MOSFET. Start-up into overvoltage will require additional SOA considerations.

### Shutdown

The LTC4366 has a low current (<20µA) shutdown state that turns off the pass FET by tying the GATE and OUT pins together with a switched resistor. In the normal operating condition, the $\overline{SD}$ pin is pulled up to the $V_{DD}$ pin voltage with a 1.6µA current source. Tie the $\overline{SD}$ pin to $V_{DD}$ when the shutdown state is not used.

Bringing the $\overline{SD}$ pin more than 1.5V below $V_{DD}$ pin voltage for greater than the 700µs filter time activates the shutdown state. This filter time prevents unwanted activation of shutdown during transients. The $\overline{SD}$ pin is diode clamped 0.7V below $V_{SS}$ which requires current limiting (maximum 10mA) on the pull-down device. One way to limit the current is to connect an external 470k resistor in series with the open-collector pull-down device. Activating the external pull-down overcomes the internal 1.6µA pull-up current source and allows the $\overline{SD}$ pin to cross the shutdown threshold.

## APPLICATIONS INFORMATION

Following an overvoltage fault, putting the part in shutdown will clear the fault, allowing operation to resume once the LTC4366 leaves shutdown.

### Output Short

A sudden short on the output can result in excessive current into the LTC4366 GATE pin supplied from the gate capacitor, $C_G$. The GATE pin is internally clamped to OUT with a 10V to 12V clamp. If the OUT pin is pulled low while the GATE pin is held up with $C_G$, then the clamp will be damaged trying to discharge $C_G$ when clamp voltage is exceeded. One solution is to add a 1k $R_S$ resistor in series with $C_G$ with a bypass diode as shown in Figure 3. The diode allows the capacitor to function as a bypass for energy coming from the MOSFET drain to gate capacitor during an supply overvoltage.

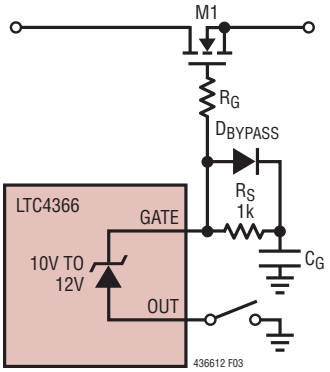



**Figure 3. Output Short Protection**

### Resistor Power Ratings

The proper rating for the $R_{SS}$ resistor in Figure 1 must be considered. During an overvoltage event the OUT pin is at regulation voltage ($V_{REG}$), so the voltage across $R_{SS}$ is $V_{REG}$ minus 5.7V. A small minimum supply voltage reduces the value of $R_{SS}$. Therefore, large differences between minimum supply voltage and the regulation voltage may require a large power resistor for $R_{SS}$.

The full supply voltage minus 12V can appear across $R_{IN}$ during the overvoltage cool-down period. Normally the value for $R_{IN}$ is several times larger than $R_{SS}$ which lowers the power and size requirements for this resistor.

### External PNP

In some cases the power resistor for $R_{SS}$ may be physically large. A large value $R_{SS}$ (with lower power and size) may be used in conjunction with a PNP as shown in Figure 4. In addition to the 0.8µA sourced from the BASE pin, the base current from the PNP must flow through $R_{SS}$ which will limit the maximum $R_{SS}$ value. In some cases the minimum PNP Beta is as low as 35. The base current becomes 10µA when the $V_{SS}$ current is 350µA. One can see this allows a 35 (Beta) times larger $R_{SS}$ than the application without the PNP.

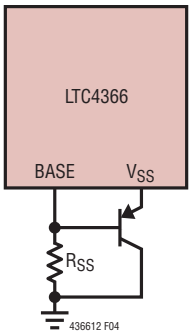



**Figure 4. External PNP Option**

### Minimum Supply Start-Up

When designing for the minimum supply condition, it is important that $R_{SS}$ and $R_{IN}$ are chosen to provide enough current to sufficiently charge C1 to 4.75V. The parameters that determine the minimum supply voltage include: C1 voltage, MOSFET threshold voltage, a series Schottky diode voltage drop, resistance of $R_{SS}$ and $R_{IN}$, current in the $V_{DD}$

## APPLICATIONS INFORMATION

pin, and finally the current from the $V_{SS}$ pin (see Figure 5).

$$V_{IN(MIN)} = (I_{VDD} \bullet R_{IN}) + V_D + V_{TH} + V_{C1} + (I_{VSS} \bullet R_{SS})$$

Using the Electrical Characteristics table for above parameters:

$V_{C1} = V_{UVLO2} = 4.75V$ (UVLO2 threshold)

$I_{VDD} = I_{VDD(STHI)} = 9\mu A$ ($I_{VDD}$ start-up, gate high)

$I_{VSS} = I_{VSS(AMP)} = 45\mu A$ ($I_{VSS}$ w/regulation amp)

$V_D = 0.58V$

$$V_{IN(MIN)} = (9\mu A \bullet R_{IN}) + 0.58V + V_{TH} + 4.75V + (45\mu A \bullet R_{SS})$$

When the MOSFET gate is fully enhanced, the OUT pin voltage is equal to the supply voltage. This places another constraint on the minimum supply voltage because the charge pump increases the $V_{SS}$ current to 160µA. The C1 voltage is assumed to be clamped at 5.7V. These values are specified as $V_{Z(OUT)}$ and $I_{VSS(CP)}$ (charge pump on) in the table of Electrical Characteristics:

$$V_{IN(MIN)} = V_{Z(OUT)} + (I_{VSS(CP)} \bullet R_{SS})$$

or

$$V_{IN(MIN)} = 5.7V + (160\mu A \bullet R_{SS})$$

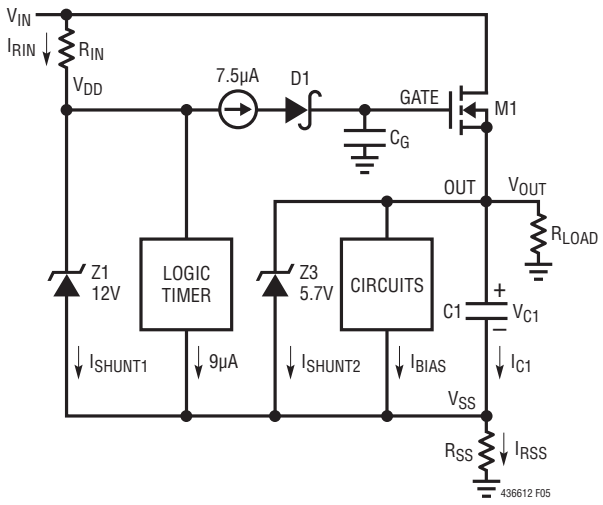



**Figure 5. Simplified Block Diagram**

The last $V_{IN(MIN)}$ equation sets the maximum value for $R_{SS}$. After choosing $R_{SS}$ the maximum value for $R_{IN}$ (for that particular $R_{SS}$) is calculated from the first $V_{IN(MIN)}$ equation:

$$R_{SS(MAX)} = \frac{V_{IN(MIN)} - 5.7V}{160\mu A}$$

$$R_{IN(MAX)} = \frac{V_{IN(MIN)} - 4.75V - 0.58V - V_{TH} - (45\mu A \bullet R_{SS})}{9\mu A}$$

These two equations maximize the values of $R_{SS}$ and $R_{IN}$ (reducing power dissipation) while still providing the necessary $V_{C1}$ voltage to turn the charge pump on. Increasing the supply voltage beyond the minimum supply voltage increases the current and power in $R_{SS}$ while reducing the time required to charge C1. Conditions that may require an even smaller $R_{SS(MAX)}$ will be discussed in the Maximum Supply Start-Up section.

### Maximum Supply Start-Up

The maximum overvoltage supply may also exist during start-up. The overvoltage protection circuitry has to wake up before high voltage is passed to the load. Dynamically the GATE is ramping up while C1 is charging. Capacitor C1 must charge to the 2.55V UVLO1 threshold to turn on the regulation amplifier and reference before the OUT pin voltage exceeds the overvoltage regulation point, $V_{REG}$. These conditions may reduce the value of $R_{SS}$ below the maximum value dictated by the minimum supply start-up discussed above.

When current in $R_{SS}$ exceeds the current sourced from the $V_{SS}$ pin (essentially $I_{RIN}$), the capacitor C1 begins to charge. The voltage at the $V_{SS}$ pin when $I_{RIN} = I_{RSS}$ is now labeled $V_{SS(MATCH)}$. The $V_{SS}$ pin voltage is the center of a voltage divider between $R_{IN}$ and $R_{SS}$ after the Zener clamp voltage from $V_{DD}$ to $V_{SS}$ is subtracted from the supply.

$$V_{SS(MATCH)} = \frac{R_{SS}}{R_{SS} + R_{IN}} \bullet \left(V_{IN(MAX)} - V_{Z(VDD)}\right)$$

As $V_{IN}$ increases the $V_{SS(MATCH)}$ voltage increases. If the match voltage exceeds the overvoltage regulation point ($V_{REG}$), then load is unprotected. This is true because C1 will still need to charge to 2.55V while $V_{SS}$ already

## APPLICATIONS INFORMATION

has exceeded $V_{REG}$. Since the OUT pin voltage is at least 2.55V larger than $V_{SS}$ it exceeds the specified maximum. Choosing the match point (with supply at the maximum) sufficiently below $V_{REG}$ (by at least 2.55V), allows C1 to charge up in time to protect the load from overvoltage. In reality having $V_{SS}$ pin voltage 7V below $V_{REG}$ provides required margin for charging C1.

$$V_{SS(MATCH)(MAX)} = V_{REG} - 7V$$

Increasing $R_{SS}$ increases the match point, so determining the maximum $R_{SS}$ value while still protecting from overvoltage is useful. Using $I_{RIN} = I_{RSS}$:

$$R_{SS} = R_{IN} \bullet \frac{V_{RSS}}{V_{RIN}}$$

Using:

$$V_{RSS} = V_{SS(MATCH)(MAX)} = V_{REG} - 7V$$

$$V_{RIN} = V_{IN} - V_{Z(VDD)} - V_{RSS}$$

Substituting:

$$R_{SS(MAX)} = \frac{R_{IN} \bullet (V_{REG} - 7V)}{V_{IN(MAX)} - 12V - (V_{REG} - 7V)}$$

$$R_{SS(MAX)} = \frac{R_{IN} \bullet (V_{REG} - 7V)}{V_{IN(MAX)} - 5V - V_{REG}}$$

If we guarantee that $R_{SS} < R_{SS(MAX)}$ then the following is true:

$$V_{SS(MATCH)} < V_{SS(MATCH)(MAX)}$$

C1 bypasses the charge pump, and requires at least a 0.22µF. The size of C1 needs limits also. The gate capacitor ($C_G$) dictates the maximum output capacitor $C1_{(MAX)}$ that will charge to the 2.55V UVLO1 threshold ($V_{UVLO1}$) before the OUT voltage exceeds the overvoltage threshold.

$$C1_{(MAX)} = \frac{-C_G \bullet (R_{SS} + R_{IN})(V_{REG} - V_{SS(MATCH)})}{I_G \bullet R_{SS} \bullet R_{IN} \bullet \ln\left[1 - \frac{2 \bullet V_{UVLO1}}{V_{REG} - V_{SS(MATCH)}}\right]}$$

In most cases:

$$C1_{(MAX)} = 10 \bullet C_G \text{ to } 100 \bullet C_G$$

### GATE Capacitor, $C_G$

The gate capacitor is used for three functions. First, $C_G$ absorbs charge from the gate-to-drain capacitance of the MOSFET during overvoltage transients. Second, the capacitor also acts as a compensation element for the overvoltage regulation amplifier. The minimum value for $C_G$ to guarantee stability is 2nF. Finally, $C_G$ sets the slew rate of the GATE and OUT pins. The voltage at the GATE pin rises at a slope equal to 20µA/$C_G$. This slope determines the charging current into the load capacitor.

$$I_{INRUSH} = \frac{C_{LOAD}}{C_G} \bullet I_G$$

The voltage rating for $C_G$ must be greater than the regulation voltage ($V_{REG}$).

### MOSFET Selection

The LTC4366 drives an N-channel MOSFET to conduct the load current. The important features of the MOSFET are on-resistance, $R_{DS(ON)}$, the maximum drain-source voltage, $V_{(BR)DSS}$, the threshold voltage, and the SOA.

The maximum allowable drain-source voltage must be higher than the supply voltage. If the output is shorted to ground or during an overvoltage event, the full supply voltage will appear across the MOSFET.

The threshold voltage of the MOSFET is used in the minimum supply start-up calculation. For applications with supplies less than 12V, a logic-level MOSFET is required. Above 12V a standard threshold N-channel MOSFET is sufficient.

The SOA of the MOSFET must encompass all fault conditions. In normal operation the pass transistor is fully on, dissipating very little power. But during overvoltage faults, the GATE pin is servoed to regulate the output voltage through the MOSFET. Large current and high voltage drop across the MOSFET can coexist in these cases. The SOA curves of the MOSFET must be considered carefully along with the selection of the fault timer capacitor.

# APPLICATIONS INFORMATION

## Layout Considerations

Due to the high impedances on the $\overline{SD}$, $V_{DD}$, and GATE pins, these pins are susceptible to leakages to ground. For example, a leakage to ground on $\overline{SD}$ will activate the shutdown state if greater than 1.6µA. Providing adequate spacing away from grounded traces and adding conformal coating on exposed pins lowers the risk that leakage current will interrupt system operation.

It is important to put the bypass capacitor, C1, as close as possible to the OUT and $V_{SS}$ pins. Place the 10Ω resistor as close as possible to the MOSFET gate pin. This will limit the parasitic trace capacitance that leads to MOSFET self-oscillation.

The FB pin is sensitive to parasitic capacitance when the regulation loop is closed. One result from this capacitive loading is output oscillations during overvoltage regulation. It is suggested that the resistors $R_{FB1}$ and $R_{FB2}$ be placed close to the pin and that the FB trace itself be minimized in size.

## DESIGN EXAMPLE

### Overview

The design process starts with minimum input voltage start-up equations to calculate values for $R_{SS}$ and $R_{IN}$. These values need further refinement to meet two other conditions: the maximum input voltage start-up conditions and proper current for the charging of C1. The the remaining element values are calculated based on the input parameters.

Following are the input parameters for this example:

$V_{SUPPLY(MIN)}$ = 18V, $V_{REG}$ = 43V, $V_{IN(MAX)}$ = 250V, $I_{LOAD}$ = 1.5A at start-up, $I_{LOAD}$ = 3A after start-up, $V_{TH}$ = 5V

Important Electrical Characteristics table parameters used in this example are summarized in Table 1.

### Step 1: Maximum $R_{SS}$

In this design example (Figure 6.) the component sizing first considers the start-up phase after the charge pump is active. The goal is to maximize the resistance of $R_{SS}$ which still allows operation when the input voltage is at the minimum value.

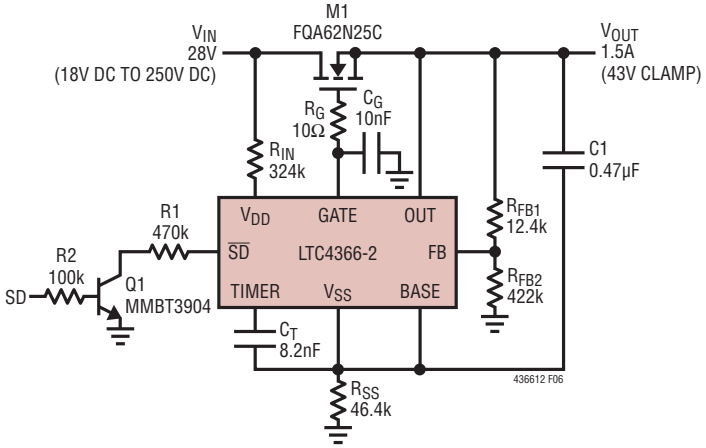



**Figure 6. Overvoltage Protected 28V, 1.5A Supply**

## APPLICATIONS INFORMATION

**Table 1. Electrical Parameters Used in Design Example**

| SYMBOL | PARAMETER | CONDITIONS | TYP | MAX |
|---|---|---|---|---|
| $V_{Z(OUT)}$ | OUT Shunt Reg. Voltage | I = 1mA, BASE = 0V | 5.7V | 6.0V |
| $V_{UVLO2}$ | OUT Undervoltage Lockout 2 | Rising | 4.75V | 4.9V |
| $I_{VSS(CP)}$ | $V_{SS}$ Pin Current – Charge Pump On | | –160µA | –230µA |
| $I_{VSS(AMP)}$ | $V_{SS}$ Pin Current – Regulation Amplifier On | | –45µA | –72µA |
| $I_{VDD(STHI)}$ | $V_{DD}$ Pin Current – Start-Up, Gate High | GATE Open, $V_{DD}$ = 7V, OUT = 0V | 9µA | 13µA |
| $I_{GATE(ST)}$ | GATE Pin Current – Start-Up | GATE = OUT = 0V | –7.5µA | –11µA |
| $V_{UVLO1}$ | OUT Undervoltage Lockout 1 | Rising | 2.55V | 2.75V |

After the charge pump is active the $V_{SS}$ current increases to 160µA (worst-case 230µA, see Table 1) current while the final value OUT voltage is equal to the minimum supply voltage. The C1 voltage is clamped at 5.7V (worst-case 6.0V):

$$R_{SS(MAX)} = \frac{V_{IN(MIN)} - V_{Z(OUT)}}{I_{VSS(CP)}}$$

$$R_{SS(MAX)} = \frac{18V - 6V}{230\mu A} = 52.3k$$

### Step 2: Determine $R_{IN}$

The value for resistor $R_{IN}$ is calculated using the calculated $R_{SS}$ value. $R_{IN}$ is chosen to provide enough headroom to sufficiently charge C1 to 4.9V the maximum undervoltage lockout 2 threshold ($V_{UVLO2}$) which starts the charge pump. The parameters that determine $R_{IN}$ include: minimum supply voltage, the final C1 voltage, MOSFET threshold voltage, $R_{SS}$, 72µA maximum $V_{SS}$ pin current (regulation amplifier on, $I_{VSS(AMP)}$), and finally the 13µA maximum start-up current in the $V_{DD}$ pin ($I_{VDD(STHI)}$):

$$R_{IN(MAX)} = \frac{V_{IN(MIN)} - V_{UVLO2} - V_D - V_{TH} - \left(I_{SS(AMP)} \bullet R_{SS}\right)}{I_{VDD(STHI)}}$$

$$R_{IN(MAX)} = \frac{18V - 4.9V - 0.58V - 5V - \left(72\mu A \bullet 52.3k\right)}{13\mu A}$$

$$R_{IN(MAX)} = 287k$$

### Step 3: Find $R_{SS(MAX)}$

In some cases this value for $R_{SS}$ is too large to charge C1 and power the overvoltage amplifier before the maximum input voltage passes to the output. The voltage at the $V_{SS}$ pin when $I_{RIN} = I_{RSS}$ is called the match point ($V_{SS(MATCH)}$). Choosing the match point (with supply at the maximum) sufficiently below $V_{REG}$ (by at least 7V), allows C1 to charge up in time to protect the load from overvoltage:

$$R_{SS(MAX)} = \frac{R_{IN} \bullet \left(V_{REG} - 7V\right)}{V_{IN(MAX)} - 5V - V_{REG}}$$

$$R_{SS(MAX)} = \frac{287k \bullet \left(43V - 7V\right)}{250V - 5V - 43V} = 51.1k$$

In this case the $R_{SS}$ value of 52.3k calculated in Step 1 is too large.

### Step 4: Iterate Smaller $R_{SS}$

Using 51.1k ($R_{SS(MAX)}$) as the next guess for $R_{SS}$, we can now calculate $R_{IN}$ and $R_{SS(MAX)}$:

$$R_{IN} = \frac{18V - 4.9V - 0.58V - 5V - \left(72\mu A \bullet 51.1k\right)}{13\mu A}$$

$$R_{IN} = 294k$$

$$R_{SS(MAX)} \frac{294k \bullet \left(43V - 7V\right)}{250V - 5V - 43V} = 52.3k$$

In this case the $R_{SS}$ value of 51.1k is less than $R_{SS(MAX)}$ and the solution is acceptable.

## APPLICATIONS INFORMATION

### Step 5: Determine $C_G$, $C1_{(MAX)}$, Check $R_{SS}$

The gate capacitor ($C_G$) determines the gate slew rate and therefore the slew rate of the OUT pin since the output voltage follows the GATE pin. The voltage at the GATE pin rises with a slope equal to 7.5µA/$C_G$ at startup and 20µA/$C_G$ when the charge pump is on. Limiting this slope will limit the inrush current charging the load capacitance where:

$$I_{INRUSH} = \frac{C_{LOAD}}{C_G} \bullet I_G$$

In this example we choose $C_G$ to be 10nF which limits the inrush current to be 660mA for a 330µF $C_{LOAD}$.

C1 is used as a bypass capacitor for the circuitry between the OUT and $V_{SS}$ pins. C1 also stabilizes the shunt regulator that clamps the voltage between these pins where the minimum value for regulator stability is 0.22µF. An even greater 0.47µF value is desired for C1 to protect the OUT to $V_{SS}$ circuitry from transients on the OUT pin.

The startup into an overvoltage creates an upper boundary on the value of C1. The value of $C_G$, $R_{SS}$ and $R_{VIN}$ determines a maximum C1 that will reach UVLO1 and power the regulation amplifier before the OUT pin voltage exceeds the overvoltage threshold. If our desired value for C1 (0.47µF) exceeds the maximum allowed C1 then a smaller $R_{SS}$ must be used to iterate a new solution for $C1_{(MAX)}$. We start with calculating $V_{SS(MATCH)}$:

$$V_{SS(MATCH)} = \frac{R_{SS}}{R_{SS} + R_{VIN}} \bullet \left(V_{IN} - V_{Z(VDD)}\right)$$

If we use the worst-case 1% maximum value for $R_{SS}$ (51.6k) and minimum value for $R_{VIN}$ (291k):

$$V_{SS(MATCH)} = 35.8V$$

$$C1_{(MAX)} = \frac{-C_G \bullet (R_{SS} + R_{IN})\left(V_{REG} - V_{SS(MATCH)}\right)}{I_G \bullet R_{SS} \bullet R_{IN} \bullet \ln\left[1 - \frac{2 \bullet V_{UVLO1}}{V_{REG} - V_{SS(MATCH)}}\right]}$$

Use the worst-case maximum gate current of 11µA instead of the typical 7.5µA and the worst-case minimum UVLO1 threshold, 2.75V:

$$C1_{(MAX)} = \frac{-10nF \bullet (51.6k + 291k)(43V - 35.8V)}{11\mu A \bullet 51.6k \bullet 291k \bullet \ln\left[1 - \frac{2 \bullet 2.75V}{43V - 35.8V}\right]}$$

or

$$C1_{(MAX)} = 0.1\mu F$$

This limit on C1 does not meet the shunt regulator stability requirements (C1 > 0.22µF).

If we desire a larger value of C1 then a lower size of $R_{SS}$ is required. A lower value for $R_{SS}$ is 48.7k, which calls out an $R_{IN}$ value of 309k and a max C1 value of 0.27µF. The next lower value of 46.4k with $R_{VIN}$ of 324k, results in the worst-case maximum C1 value of 0.49µF. A larger C1 increases circuit immunity to transients in exchange for slightly higher current. Therefore, a selection of components that allow a 0.47µF C1 is recommended.

The lowered $R_{SS}$ value of 46.4k now considers the tolerances of all the components that set the C1 ramp rate to guarantee it charges to the 2.55V UVLO1 threshold before the OUT voltage exceeds the overvoltage threshold.

### Step 6: Determine $R_{FB1}$, $R_{FB2}$

The feedback resistors, $R_{FB1}$ and $R_{FB2}$, are chosen to regulate the overvoltage at 43V. One way to quickly choose these resistors is to assign 100µA or 1.2V across a 12.4k $R_{FB1}$. $R_{FB2}$ would need to drop the remainder of the regulated voltage. Dividing this remainder by 100µA yields the value for $R_{FB2}$. In this example $R_{FB2}$ drops 41.8V. When divided by 100µA it results in a 422k value.

### Step 7: Determine $C_T$, R1

During an overvoltage the power dissipated in the MOSFET is dependent on the load current and the difference between the supply and regulated voltages. It is necessary to keep the device power in a safe range. In the power MOSFET data sheets there is a maximum safe operating curve displaying current versus drain to source voltage for a fixed pulsed time. Other pulsed time data from DC to 10µs are plotted on the one graph. The different lines of operation generally follow a constant power squared

## APPLICATIONS INFORMATION

times time or $P^2t$. Knowing the power we then adjust the time using the timer capacitor to limit the $P^2t$ during overvoltage. In this example the MOSFET data sheet has a $640W^2s$ $P^2t$ for a 10ms single pulse.

In this application 250V minus 43V is applied across the MOSFET at 3A. If the power is applied for less than 16.5ms then MOSFET $P^2t$ limit is not exceeded:

$$P = (250V - 43V) \bullet 3A = 621W$$

$$P^2t = (621W)^2 \bullet 16.5ms = 6363W^2s$$

Prior to the moment when the output is regulated at 43V, the output is ramping from 28V to 43V. This ramp time is based on the 20µA gate current charging the 10nF capacitor. Using the equation for ramp time:

$$\Delta t = \frac{C_G \bullet \Delta V}{I_G} = \frac{10nF \bullet 15V}{20\mu A} = 7.5ms$$

To be safe we set the overvoltage time to 10ms. We set the regulation time to be 2.5ms (the remainder of the 10ms overvoltage time minus the ramp time). In this example it is assumed the 250V overvoltage is a constant DC voltage for 10ms. This duration exceeds Mil-Std-1275 which specifies a 70µs surge to 250V that decays in 1.6ms. Using the following equation (based on charging with 9µA) to set the $C_T$:

$$C_T = I_T \bullet \frac{\Delta t}{\Delta V} = 9\mu A \bullet \frac{2.5ms}{2.8V} \approx 8.2nF$$

In order to limit the $\overline{SD}$ pin current (10mA max) a collector resistor, R1, in series with Q1 is required. The maximum value for this resistor is around 5M. This requirement occurs when the pull-down is required to sink 1.6µA from $\overline{SD}$ and $V_{DD}$ is clamped at 12V. High valued resistors are susceptible to leakage currents so we chose a 470k resistor for R1. Resistor R2 provides ESD protection for Q1's base.

The gate resistor $R_G$ limits the parasitic trace capacitance on M1's gate node that could lead to parasitic MOSFET self-oscillation. The recommended value for $R_G$ is 10Ω.

### High Voltage Application

In Figure 7 the circuit accepts 110V AC (rectified to 160V) and protects the load from accidental connection to 220V AC by limiting the output to less than 200V. The circuit has a 100V to 800V $V_{IN}$ operating range where the FET breakdown voltage limits the maximum input voltage. The C1 is set to 0.47µF to provide a bypass for the charge pump that is large enough to provide good noise immunity from outside voltage transients. The timer capacitor is sized to give a 1ms overvoltage regulation time that keeps the $P^2t$ below the $640W^2s$ specified for this MOSFET.

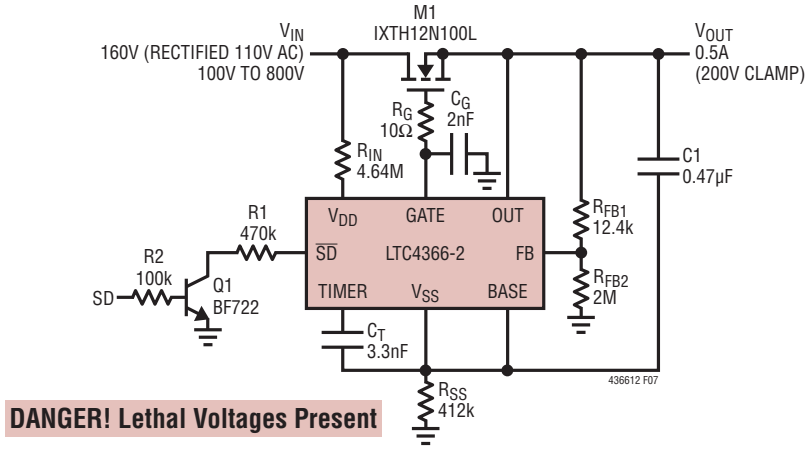



**Figure 7. Rectified 110V AC Supply Protected from 220V AC**

## APPLICATIONS INFORMATION

### 28V Vehicle Application

The circuit in Figure 8 adds reverse voltage protection to the standard 28V application shown in Figure 6. There are three modes to this circuit: pass FET On when the input is 18V to 41V, clamping the output to 43V when more than 43V appears at the input and finally reverse voltage protection when up to –250V DC is present at the input.

The reverse voltage protection consists of the circuitry inside the dotted box in Figure 8. When a positive voltage is first applied to the input, D3 and the forward biased base-collector junction of Q2 allow the gate of M2 to follow the input voltage minus a two diode drop. During this condition the body diode of M2 is used to transmit power to the LTC4366. Once the LTC4366 is powered up it fully enhances the gate of M1 and M2 (via D1). The M1 and M2 pass FETs then provide a low impedance path to the load. In an overvoltage condition, D1 blocks excessive positive voltage from the input supply passing to the GATE pin of the LTC4366. D4 eliminates current flow through R6 when the input is positive while D3 prevents emitter base breakdown of Q2 when the input is powering up.

During negative input voltages Q2 turns on when current from R6 (via D4) develops a forward diode drop on R5. Q2 then holds the gate of M2 at the input voltage which turns M2 off. This blocks negative input voltages from reaching M1 and the load. D2 prevents damage to the LTC4366's GATE pin by clamping it at ground when the M2's gate is negative.

### Low Voltage Application

The circuit on the last page (Surge Protected Automotive Supply) starts up with minimum input voltage of 9V. In order to successfully start up at 9V and clamp the output voltage at 18V for input voltages up to 100V the value of $R_{SS}$ has to be small (1.91k). The FET used in this case has a 3V threshold to ease the start-up requirements. The timer capacitor is sized to give a 2.5ms overvoltage regulation time that keeps the $P^2t$ below the $420W^2s$ specified for this MOSFET.

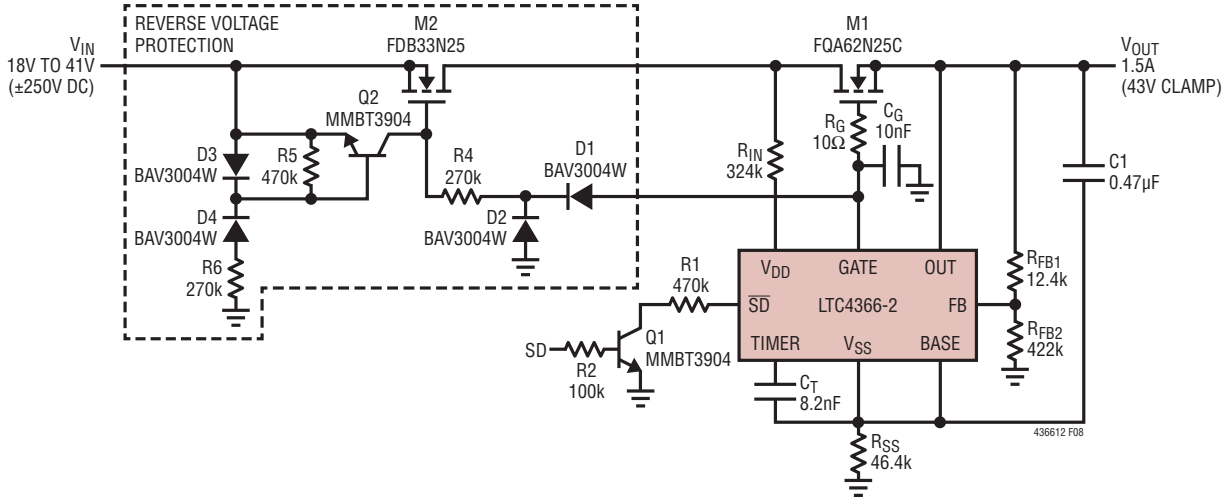
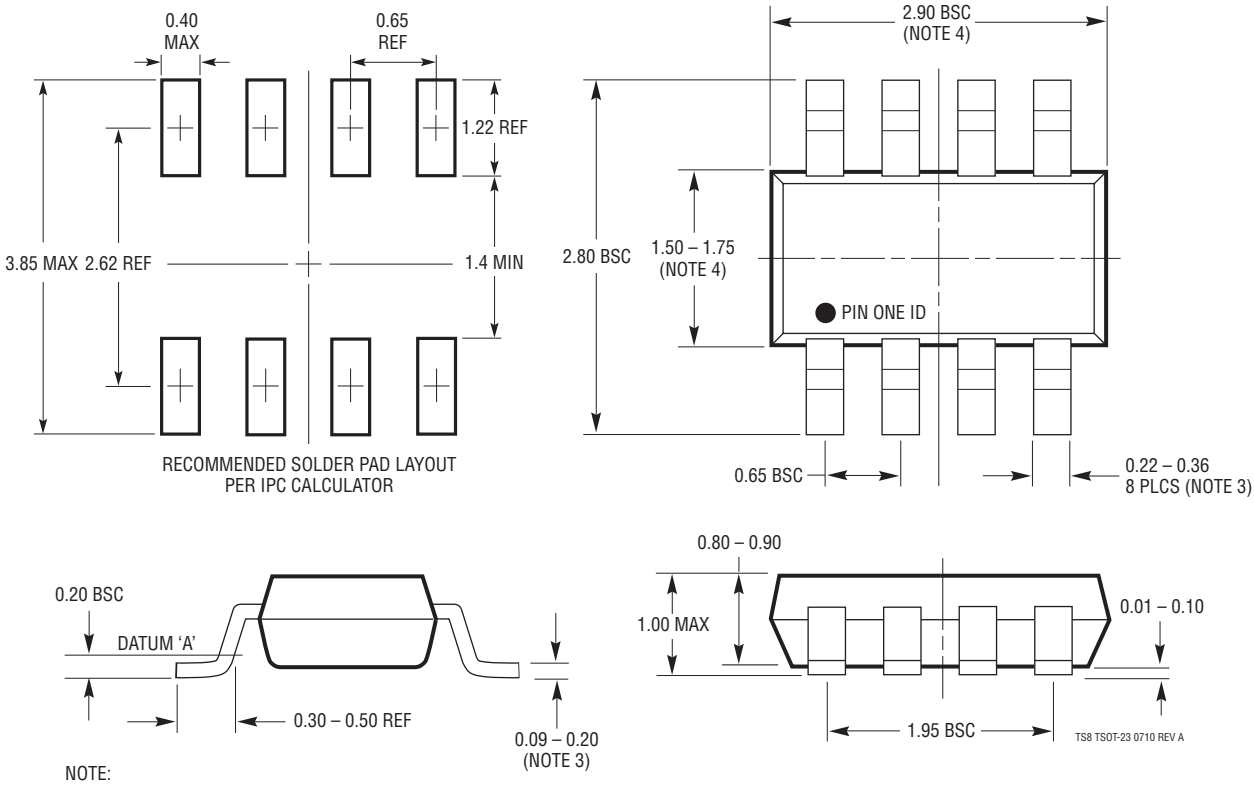



**Figure 8. 28V Vehicle Application with Reverse Voltage Protection**

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**TS8 Package**
**8-Lead Plastic TSOT-23**
(Reference LTC DWG # 05-08-1637 Rev A)

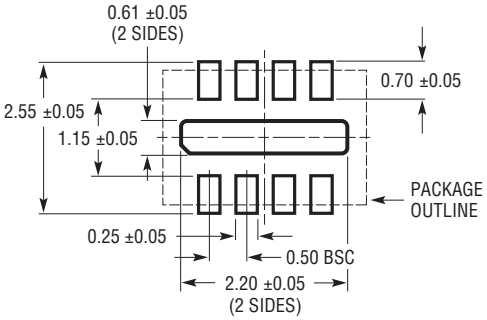



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

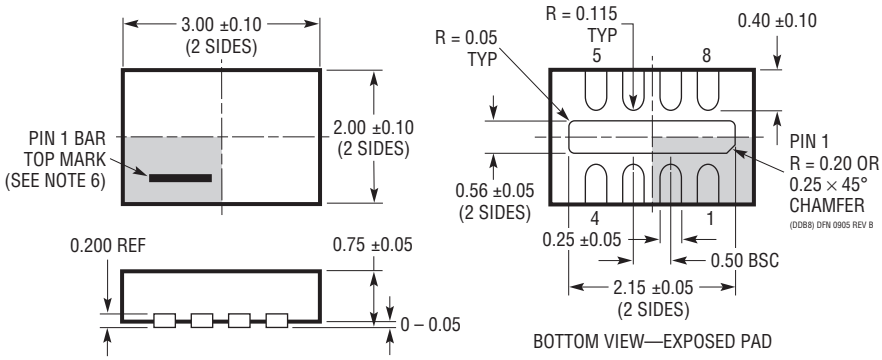
# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**DDB Package**
**8-Lead Plastic DFN (3mm × 2mm)**
(Reference LTC DWG # 05-08-1702 Rev B)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 1/12 | Added Patents Pending statement | 1 |
| | | Revised Figure 4 in Applications Information section | 11 |
| B | 2/12 | Removed reference to overcurrent faults under MOSFET Selection | 13 |
| | | Fixed orientation of M2 in Figure 8 | 18 |
| C | 8/12 | Updated Shutdown current from <20µA to <14µA | 1 |
| | | Changed MOSFET part number and Gate Capacitor value used in the Typical Application | 1 |
| | | Added MP-grade order information and specifications | 2, 3, 4, 5 |
| | | Added negative sign to graphs G12 x-axis and G18, G21 y-axis | 6, 7 |
| | | Changed MOSFET part number in Figure 1 and Figure 6 | 11, 16 |
| | | Added section GATE Capacitor, $C_G$ | 15 |
| | | Changed $I_{LOAD}$ current from 5A to 3A in Design Example | 16 |
| | | Updated $C1_{(MAX)}$ values in Step 5 calculations to 0.27µF and worst case 0.49µF | 18 |
| | | Updated calculated values in Step 7, added supporting text | 19 |
| | | Changed MOSFET part number and GATE capacitor used in Figure 7 | 19 |
| D | 8/13 | Simplified Diagram: Corrected amplifier's input polarity in Regulate Diagram | 9 |
| | | Functional Diagram: Added switch in series with TIMER pull-down current | 9 |
| E | 8/15 | Clarified "Ambient" on Operating Temperature Range; raised $T_{JMAX}$ to 150°C | 2 |
| | | TIMER Pin Function: Changed 278ms/µF to 311ms/µF | 8 |
| | | Figures 1, 6, 8: Changed $C_T$ to 8.2nF from 10nF | 11, 16, 20 |
| | | In $C_T$ equation, changed constant to 3.2 from 3.5; updated $C_T$ calculation | 12, 19 |

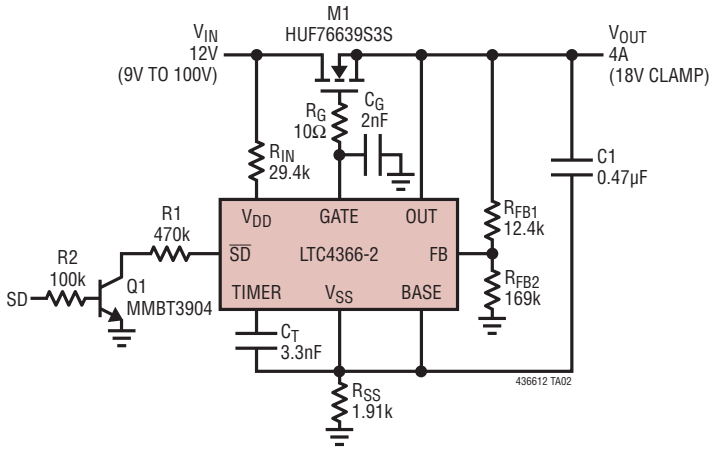


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## TYPICAL APPLICATION

**Surge Protected Automotive 12V Supply**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1696 | Overvoltage Protection Controller | ThinSOT™ Package, 2.7V to 28V |
| LTC2909 | Triple/Dual Inputs UV/OV Negative Monitor | Pin Selectable Input Polarity Allows Negative and OV Monitoring |
| LTC2912/LTC2913 | Single/Dual UV/OV Voltage Monitor | Ads UV and OV Trip Values, ±1.5% Threshold Accuracy |
| LTC2914 | Quad UV/OV Monitor | For Positive and Negative Supplies |
| LTC3827/LTC3827-1 | Low $I_Q$, Dual, Synchronous Controller | $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$, 80µA Quiescent Current |
| LTC3835/LTC3835-1 | Low $I_Q$, Synchronous Step-Down Controller | Single Channel LTC3827/LTC3827-1 |
| LT3845 | Low $I_Q$, Synchronous Step-Down Controller | $4V \le V_{IN} \le 60V$, $1.23V \le V_{OUT} \le 36V$, 120µA Quiescent Current |
| LTC3850 | Dual, 550kHz, 2-Phase Synchronous Step-Down Controller | Dual 180° Phased Controllers, $V_{IN}$ 4V to 24V, 97% Duty Cycle, 4mm × 4mm QFN-28, SSOP-28 Packages |
| LTC3890 | Low $I_Q$, Dual 2-Phase, Synchronous Step-Down Controller | $4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 24V$, 50µA Quiescent Current |
| LT4256 | Positive 48V Hot Swap Controller with Open-Circuit Detect | Foldback Current Limiting, Open-Circuit and Overcurrent Fault Output, Up to 80V Supply |
| LTC4260 | Positive High Voltage Hot Swap Controller with 8-Bit ADC and $I^2C$ | Wide Operating Range 8.5V to 80V |
| LTC4352 | Ideal MOSFET ORing Diode | External N-Channel MOSFETs Replace ORing Diodes, 0V to 18V |
| LTC4354 | Negative Voltage Diode-OR Controller | Controls Two N-Channel MOSFETs, 1.2µs Turn-Off, –80V Operation |
| LTC4355 | Positive Voltage Diode-OR Controller | Controls Two N-Channel MOSFETs, 0.4µs Turn-Off, 80V Operation |
| LT4363 | High Voltage Surge Stopper | 100V Overvoltage and Overcurrent Protection, Latch-Off and Auto-Retry Options |
| LTC4365 | Window Passer – OV, UV and Reverse Supply Protection Controller | 2.5V to 34V Operation, Protects 60V to –40V |


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