

PUMB11

PNP/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 10 kΩ

1 October 2022 Product data sheet

1. General description

PNP/PNP double Resistor-Equipped Transistor (RET) in a very SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PUMD3

NPN/NPN complement: PUMH11

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

3. Applications

- Low current peripheral drivers
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

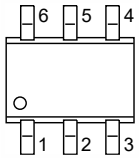
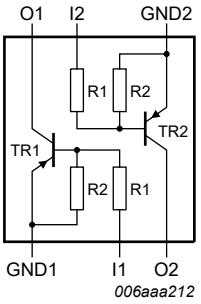
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	-50	V
I_O	output current			-	-	-100	mA
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 TSSOP6 (SOT363)	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMB11	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMB11	B%1

[1] % = placeholder for manufacturing site code

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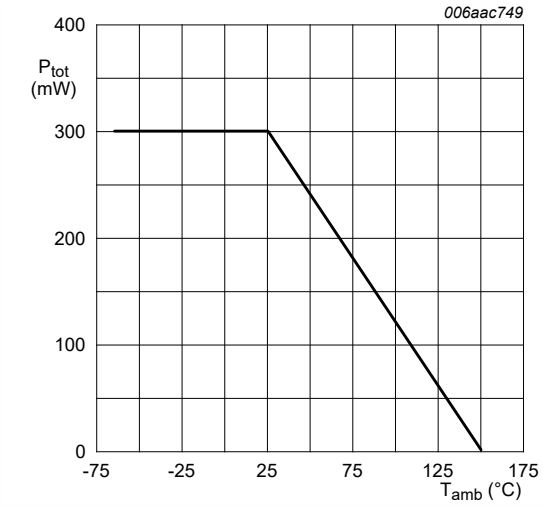
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{CBO}	collector-base voltage	open emitter		-	-50	V
V_{CEO}	collector-emitter voltage	open base		-	-50	V
V_{EBO}	emitter-base voltage	open collector		-	-10	V
V_I	input voltage	positive		-	10	V
		negative		-	-40	V
I_O	output current			-	-100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} = 25$ °C	[1]	-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

Fig. 1. Per device: Power derating curve

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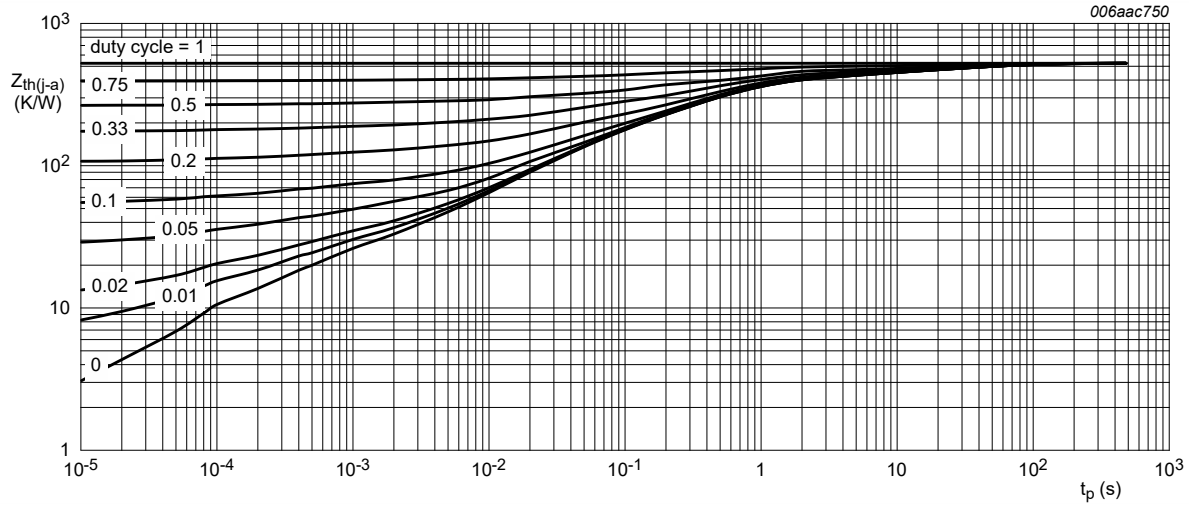
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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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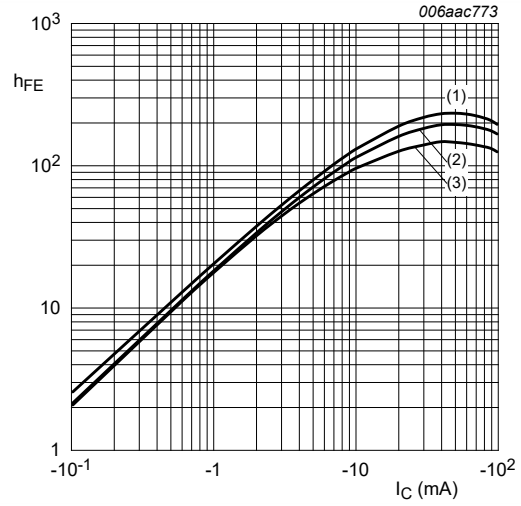
10. Characteristics

Table 7. Characteristics

T_{amb} = 25 °C unless otherwise specified.

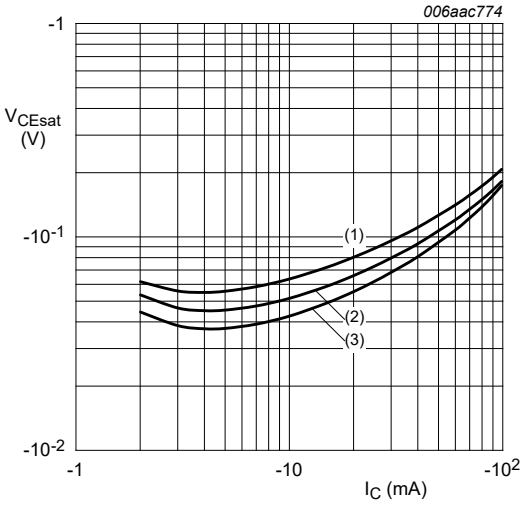
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = -100 µA; I_E = 0 A		-50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = -2 mA; I_B = 0 A		-50	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = -50 V; I_E = 0 A		-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = -30 V; I_B = 0 A		-	-	-1	µA
		V_{CE} = -30 V; I_B = 0 A; T_j = 150 °C		-	-	-5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = -5 V; I_C = 0 A		-	-	-400	µA
h_{FE}	DC current gain	V_{CE} = -5 V; I_C = -5 mA		-30	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = -10 mA; I_B = -0.5 mA		-	-	-100	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = -5 V; I_C = -100 µA		-	-1.1	-0.8	V
$V_{I(on)}$	on-state input voltage	V_{CE} = -0.3 V; I_C = -10 mA		-2.5	-1.8	-	V
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz		-	-	3	pF
f_T	transition frequency	V_{CE} = -5 V; I_C = -10 mA; f = 100 MHz	[2]	-	180	-	MHz

[1] See "Section 11: Test information" for resistor calculation and test conditions.
[2] Characteristics of built-in transistor



V_{CE} = -5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

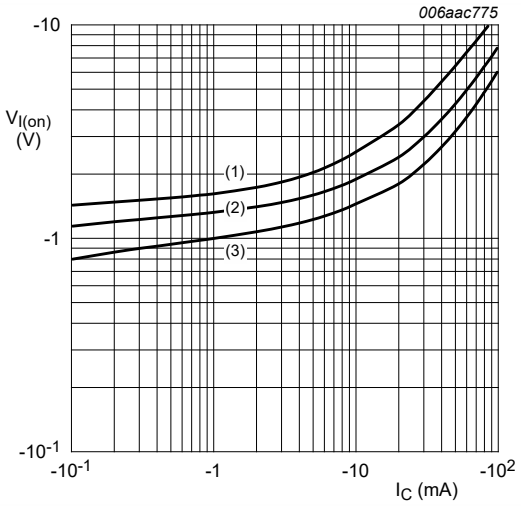
Fig. 3. DC current gain as a function of collector current; typical values



I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

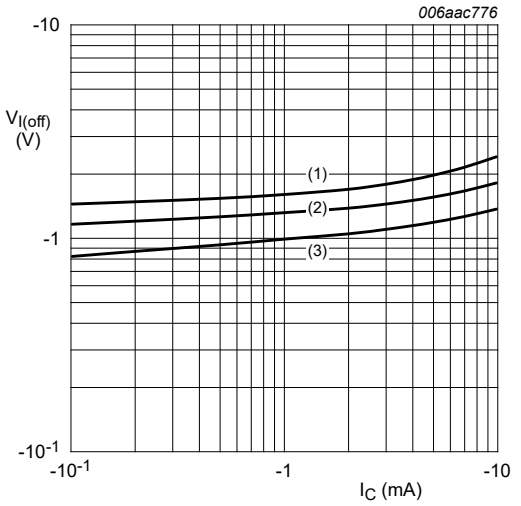
Fig. 4. Collector-emitter saturation voltage as a function of collector current; typical values

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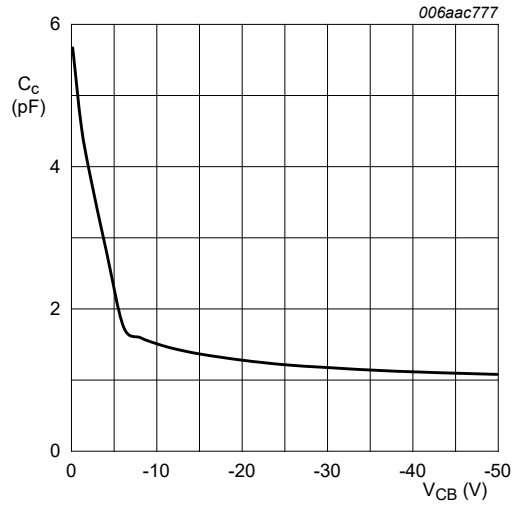
V_{CE} = -0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 5. On-state input voltage as a function of collector current; typical values



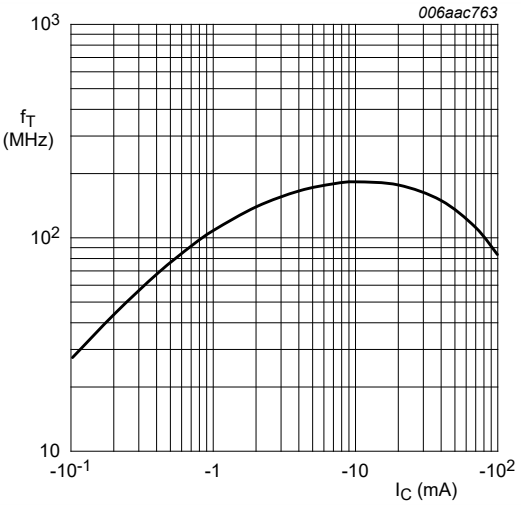
V_{CE} = -5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 6. Off-state input voltage as a function of collector current; typical values



f = 1 MHz
T_{amb} = 25 °C

Fig. 7. Collector capacitance as a function of collector-base voltage; typical values



f = 100 MHz
T_{amb} = 25 °C
V_{CE} = -5 V

Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

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11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_4) - V(I_3)}{R1 \cdot (I_4 - I_3)} - 1$$

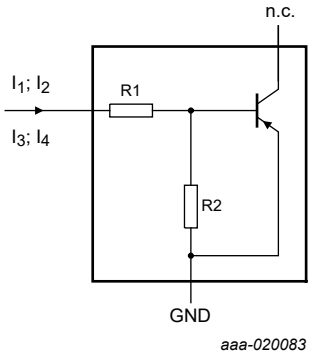


Fig. 9. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

PUMB11	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I_1	I_2	I_3	I_4
TR1 (PNP)	10	10	-350 µA	-450 µA	350 µA	450 µA
TR2 (PNP)	10	10	-350 µA	-450 µA	350 µA	450 µA

12. Package outline

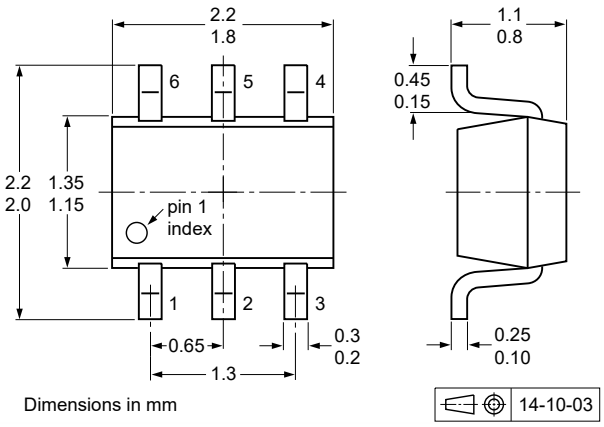


Fig. 10. Package outline TSSOP6 (SOT363)

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13. Soldering

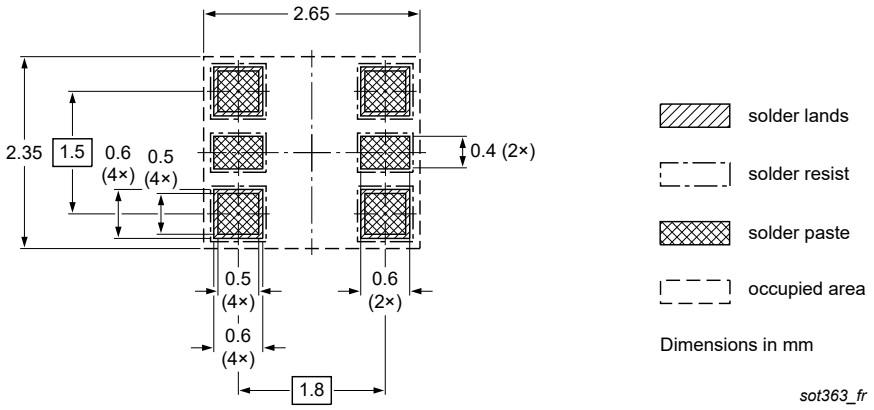


Fig. 11. Reflow soldering footprint for TSSOP6 (SOT363)

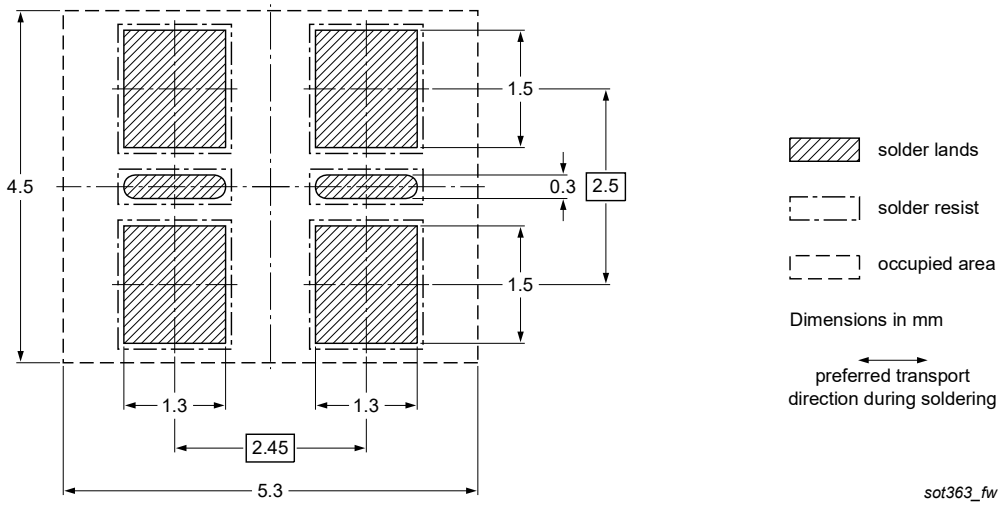


Fig. 12. Wave soldering footprint for TSSOP6 (SOT363)

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14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMB11 v.5	20221001	Product data sheet	-	PEMB11_PUMB11 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Family data sheet reduced to single type data sheet. • Product changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s). • Packing information is removed.			
PEMB11_PUMB11 v.4	20111130	Product data sheet	-	PEMB11_PUMB11 v.3
PEMB11_PUMB11 v.3	20031003	Product data sheet	-	PUMB11 v.2
PUMB11 v.2	20010913	Preliminary specification	-	PUMB11 v.1
PUMB11 v.1	20000808	Product specification	-	-

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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