WM8952

Mono ADC with Microphone Pre-amplifier

DESCRIPTION

The WM8952 is a low power, high quality mono ADC designed for portable applications such as wireless microphones or headsets.

The device integrates support for differential or single ended microphone connections. External component requirements are reduced as no separate microphone amplifier is required.

An advanced Sigma Delta Converter design is used to give high quality audio at sample rates from 8 to 48ks/s. A selectable high pass filter and four fully-programmable notch filters are also available in the signal path. An advanced mixed signal ALC function with noise gate is provided, supporting readback of PGA gain during ALC operation. The digital audio interface supports A-law and μ-law companding.

An on-chip PLL is provided to generate the required Master Clock from an external reference clock. The PLL clock can also be output if required elsewhere in the system.

The WM8952 operates at supply voltages from 2.5 to 3.6V, although the digital supplies can operate at voltages down to 1.71V to save power. Different sections of the chip can also be powered down under software control using the selectable two or three wire control interface. The device is supplied in a very small W-CSP package, offering high levels of functionality in minimum board area, with high thermal performance.

FEATURES

- **Mono ADC:**
- Audio sample rates:8, 11.025, 16, 22.05, 24, 32, 44.1, 48kHz
- ADC SNR 94dB, THD -80dB ('A'-weighted @ 8 – 48ks/s)
- **Mic Preamps :**
- Differential or single end Microphone Interface
  - Programmable preamp gain
  - Pseudo differential inputs with common mode rejection
  - Programmable ALC / Noise Gate in ADC path
- Low-noise bias supplied for electret microphones
- Multiple analog or 'Aux' inputs with analogue mixing

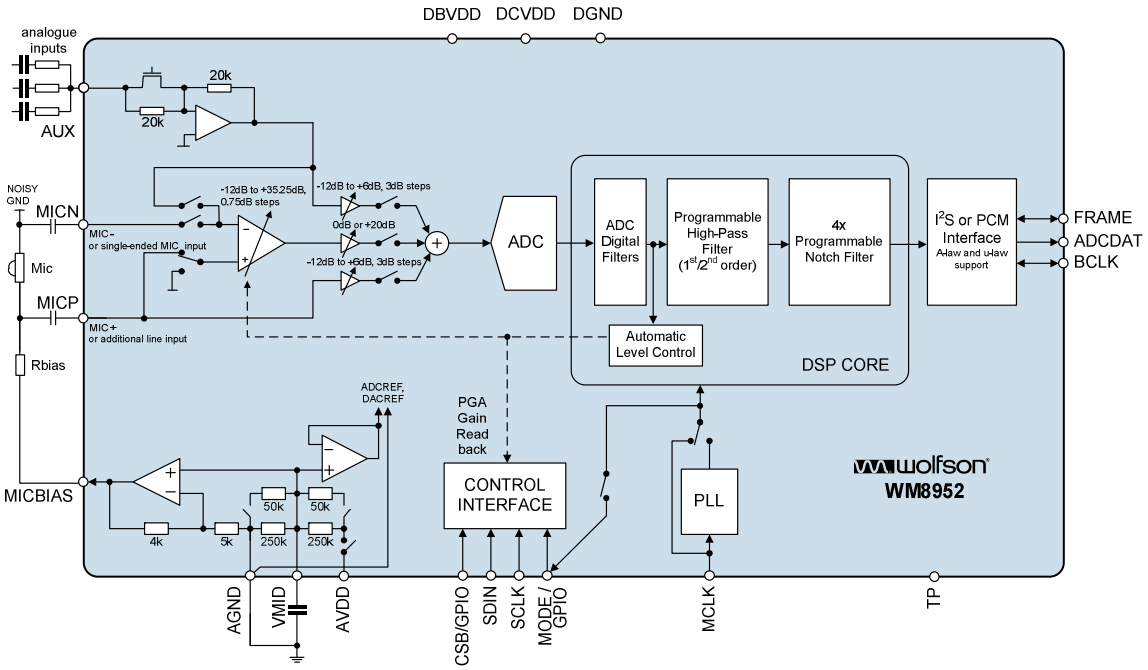
OTHER FEATURES

- Programmable high pass filter (wind noise reduction)
- 4 notch filters (narrowband noise suppression)
- On-chip PLL
- Low power, low voltage
  - 2.5V to 3.6V (digital: 1.71V to 3.6V)
- 28 ball W-CSP (2.59 × 2.5 × 0.7mm, 0.4mm pitch) Package

APPLICATIONS

- Headsets
- Wireless microphones
- General purpose mono audio ADC

BLOCK DIAGRAM



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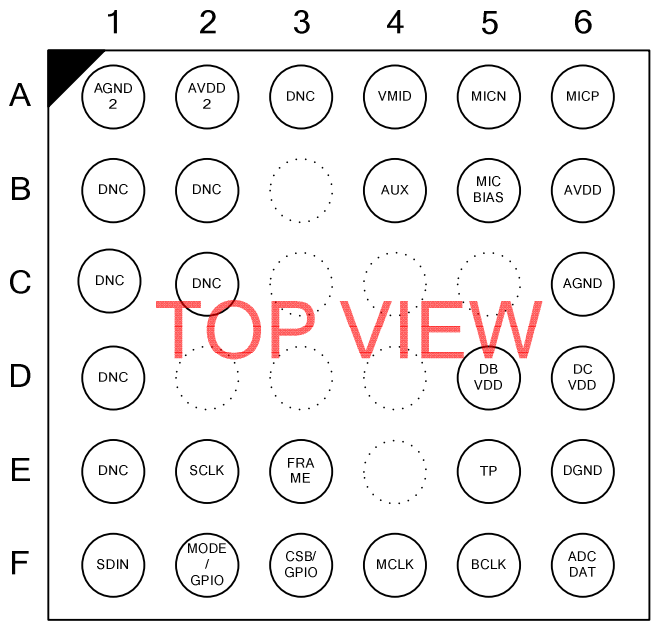
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PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PACKAGE BODY TEMPERATURE
WM8952ECS/RV	-25°C to +85°C	28-ball W-CSP (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity:

WM8952ECS/RV = 3,500

PIN DESCRIPTION

PIN (WLCSP)	NAME	TYPE	DESCRIPTION
B5	MICBIAS	Analogue Output	Microphone bias
B6	AVDD	Supply	Analogue supply
C6	AGND	Supply	Analogue ground
D6	DCVDD	Supply	Digital Supply (Core)
D5	DBVDD	Supply	Digital supply (Input/Output)
E6	DGND	Supply	Digital ground
F6	ADCDAT	Digital Output	ADC digital audio data output
E5	TP	Test pin	Connect to ground
E3	FRAME	Digital Input / Output	ADC sample rate clock or frame synch
F5	BCLK	Digital Input / Output	Digital audio port clock
F4	MCLK	Digital Input	Master clock input
F3	CSB/GPIO	Digital Input / Output	3-Wire control interface chip select or GPIO pin
E2	SCLK	Digital Input	Control interface clock input
F1	SDIN	Digital Input / Output	Control interface data input
F2	MODE/GPIO	Digital Input	Control interface mode selection or GPIO pin
A1	AGND2	Supply	Analogue ground
A2	AVDD2	Supply	Analogue supply
B4	AUX	Analogue Input	Auxiliary analogue input
A4	VMID	Reference	Decoupling for midrail reference voltage
A5	MICN	Analogue Input	Microphone negative input (common mode)
A6	MICP	Analogue Input	Microphone positive input
A3, B1, B2, C1, C2, D1, E1	DNC	Do Not Connect	Leave these pins floating

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DBVDD, DCVDD, AVDD supply voltages	-0.3V	+4.2
Voltage range digital inputs	DGND -0.3V[1]	DVDD +0.3V[1]
Voltage range analogue inputs	AGND -0.3V[1]	AVDD +0.3V[1]
Operating temperature range, T_A	-25°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.71		3.6	V
Digital supply voltage (Buffer)	DBVDD		1.71		3.6	V
Analogue supplies range	AVDD, AVDD2[1]		2.5		3.6	V
Ground	DGND, AGND, AGND2			0		V

Notes

1. Analogue supply voltage must not be less than the digital supply voltages.
2. DBVDD must be ≥ DCVDD

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD=1.8V, DBVDD=3.3V, AVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Input PGA Inputs (MICN, MICP) **INPPGAVOL and PGABOOST = 0dB**						
Full-scale Input Signal Level – Single-ended input via LIN/RIN [1]				AVDD/3.3		V_{rms}
Full-scale Input Signal Level – Pseudo-differential input [1,2]				AVDD*0.7/ 3.3		V_{rms}
Input PGA equivalent input noise		INPPGAVOL = +35.25dB No input signal 0 to 20kHz		76.5		dB
MICN input resistance		INPPGAVOL = +35.25dB		2		kΩ
MICN input resistance		INPPGAVOL = 0dB		58.5		kΩ
MICN input resistance		INPPGAVOL = -12dB		97.5		kΩ
MICP input resistance		All gain settings		124.5		kΩ
Input Capacitance		All analogue input pins		10		pF
Maximum Input PGA Programmable Gain		Gain adjusted by INPPGAVOL	+33.25	+35.25	+37.25	dB
Minimum Input PGA Programmable Gain		Gain adjusted by INPPGAVOL	-14.00	-12	-10.00	dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Input PGA Mute Attenuation		INPPGAMUTE		92		dB
Input Gain Boost		PGABOOST= 0		0		dB
Input Gain Boost		PGABOOST = 1		+20		dB
Auxiliary Analogue Input (AUX)						
Full-scale Input Signal Level [2]				AVDD/3.3		V_{rms}
Input Resistance		Input boost and mixer enabled, at 0dB gain		20		kΩ
Input Capacitance		All analogue Inputs		10		pF
Maximum Gain from AUX input PGA mixers		Gain adjusted by AUX2BOOSTVOL	+4.00	+6	+7.50	dB
Minimum Gain from AUX input PGA mixers		Gain adjusted by AUX2BOOSTVOL	-14.00	-12	-9.00	dB
AUX2BOOSTVOL step size		Guaranteed monotonic		3		dB
Analogue to Digital Converter (ADC) - Input from MICN and MICP in differential configuration to input PGA **INPPGAVO, PGABOOST and ADCVOL = 0dB**						
Signal to Noise Ratio [3]	SNR	A-weighted AVDD=3.3V	81	91		dB
Total Harmonic Distortion [4]	THD	-1dBV Input AVDD=3.3V		-83	-74	dB
Total Harmonic Distortion + Noise [5]	THD+N	-1dBV Input AVDD=3.3V		-77	-68	dB
Microphone Bias						
Bias Voltage		MBVSEL=0	0.85* AVDD	0.9*AVDD	0.95* AVDD	V
		MBVSEL=1		0.65*AVDD		V
Bias Current Source		for $V_{MICBIAS}$ within +/-3%			3	mA
Output Noise Voltage		1kHz to 20kHz		15		nV/√Hz

Test Conditions

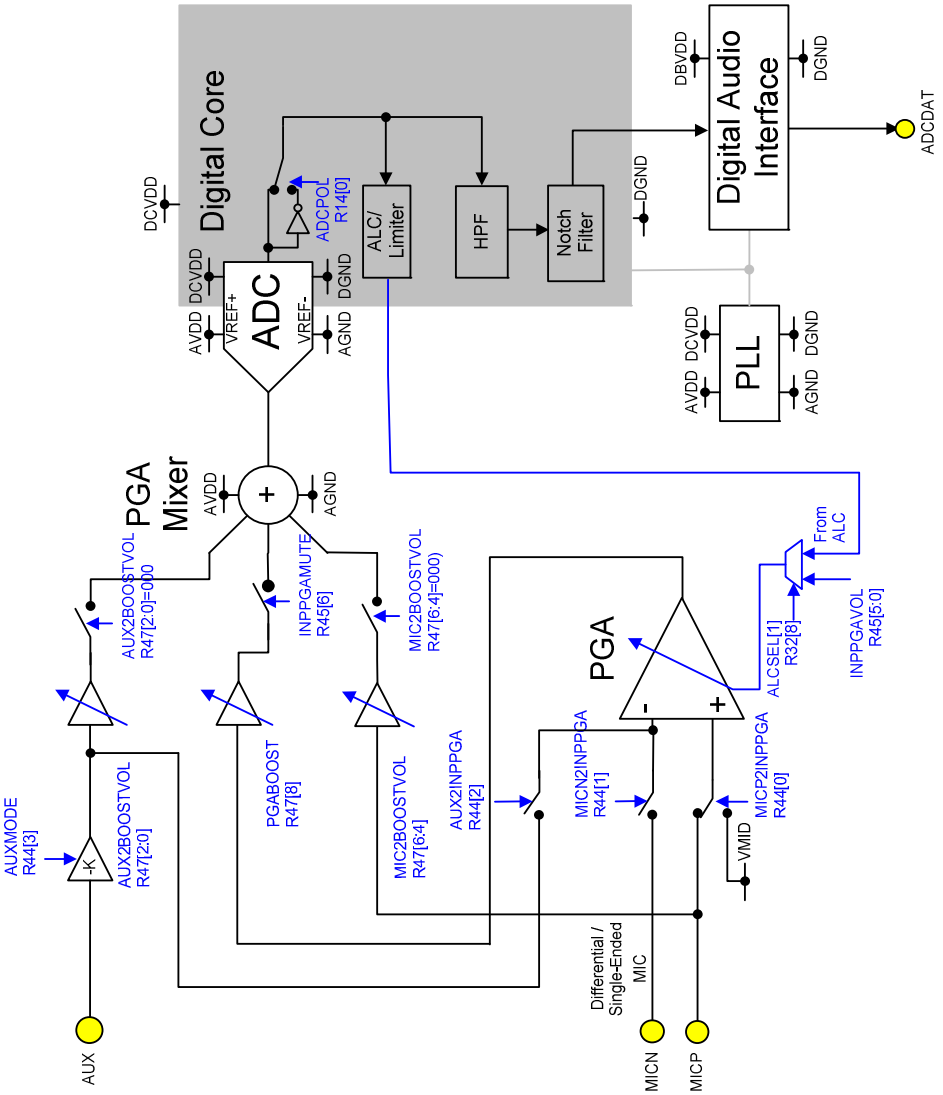
DCVDD=1.8V, DBVDD=3.3V, AVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7× DBVDD		DBVDD+0.7	V
Input LOW Level	V_{IL}		GND-0.7		0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9× DBVDD		DBVDD	V
Output LOW Level	V_{OL}	I_{OH}-1mA	GND		0.1xDBVDD	V
Input Capacitance		All digital pins		10		pF
Input leakage		All digital pins except MODE	-900		+900	nA
		MODE pin	-90		+90	µA

TERMINOLOGY

1. Full-scale input levels scale in relation to AVDD depending upon the input or output used. For example, when AVDD = 3.3V, 0dBFS = $1V_{rms}$ (0dBV). When AVDD < 3.3V the absolute level of 0dBFS will decrease with a linear relationship to AVDD.
2. Input level to RIP and LIP in differential configurations is limited to a maximum of -3dB or performance will be reduced.
3. Signal-to-noise ratio (dB) – SNR is the difference in level between a reference full scale output signal and the device output with no signal applied. This ratio is also called idle channel noise. (No Auto-zero or Automute function is employed in achieving these results).
4. THD is the difference in level between a reference output signal and the first seven harmonics of the output signal. To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the next seven harmonics is calculated.
5. Total Harmonic Distortion plus Noise (dB) – THD+N is the difference in level between a reference output signal and the sum of the harmonics, wide-band noise and interference on the output signal. To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the total harmonics, wide-band noise and interference is calculated.

AUDIO PATHS OVERVIEW



POWER CONSUMPTION

Typical current consumption for various scenarios is shown below.

MODE	AVDD (3V3) mA	DVDD (1.8V) mA	TOTAL POWER (mW)
Power OFF (No Clocks)	0.038	0	0.125
Sleep (VMID maintained, No Clocks)	0.190	0	0.627
Mono Record (MIC input, +20dB gain, 8kHz, quiescent) SLAVE	4.1	0.3	14.2
Mono Record (MIC input, +20dB gain, 44.1kHz, PLL, quiescent) MASTER	5.3	2.1	21.1

Table 1 Power Consumption

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

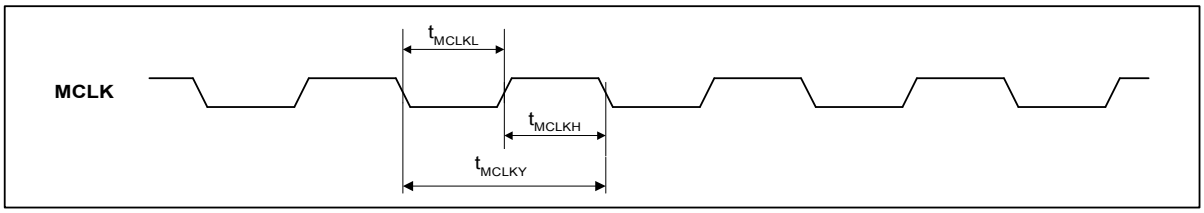


Figure 1 System Clock Timing Requirements

Test Conditions

DVDD=1.8V, AVDD=3.3V, DGND=AGND=0V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}	MCLK=SYSCLK (=256fs)	81.38			ns
		MCLK input to PLL Note 1	20			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

Note 1:

PLL pre-scaling and PLL N and K values should be set appropriately so that SYSCLK is no greater than 12.288MHz.

AUDIO INTERFACE TIMING – MASTER MODE

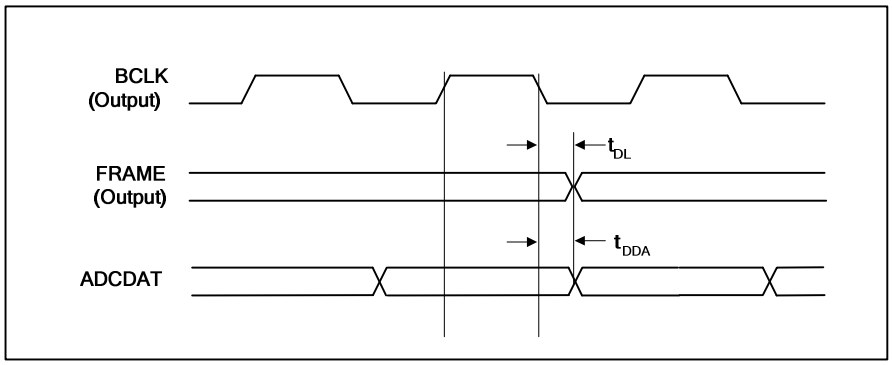


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DVDD=1.8V, AVDD= 3.3V, DGND=AGND =0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
FRAME propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			15	ns

AUDIO INTERFACE TIMING – SLAVE MODE

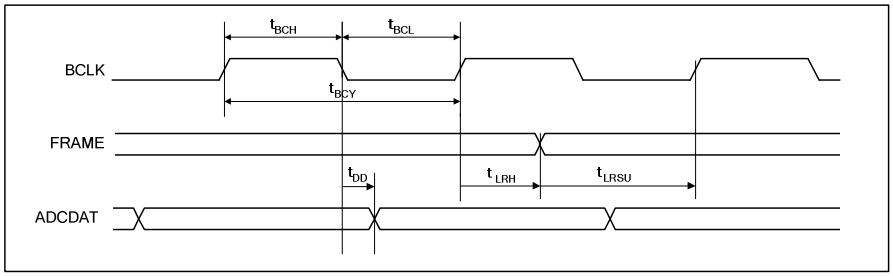


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DVDD=1.8V, AVDD=3.3V, DGND=AGND =0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	81.38			ns
BCLK pulse width high	t_{BCH}	32.55			ns
BCLK pulse width low	t_{BCL}	32.55			ns
FRAME set-up time to BCLK rising edge	t_{LRSU}	10			ns
FRAME hold time from BCLK rising edge	t_{LRH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			15	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

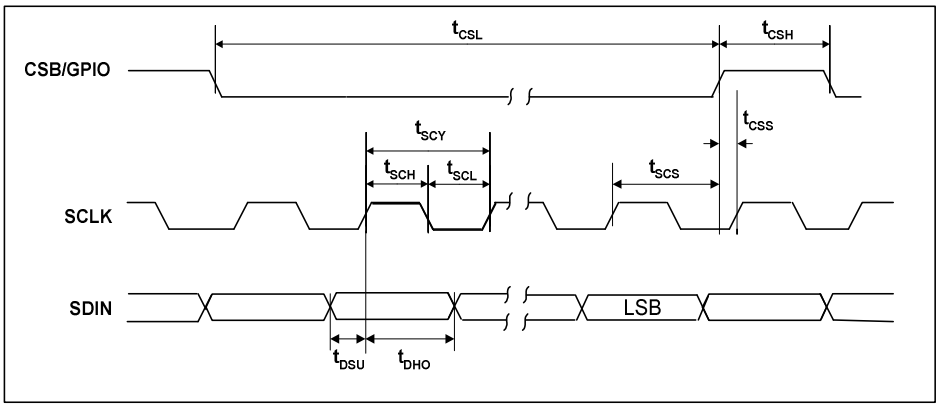


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DVDD = 1.8V, AVDD = 3.3V, DGND = AGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

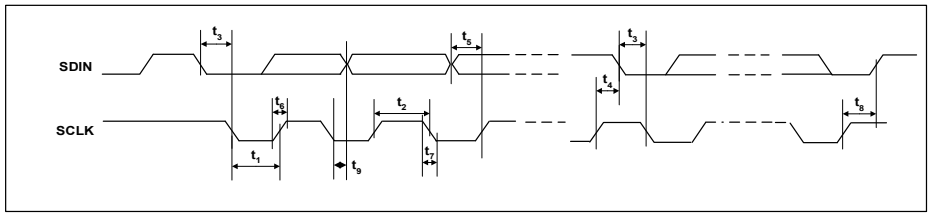


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DVDD=1.8V, AVDD=3.3V, DGND=AGND=0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

DEVICE DESCRIPTION

INTRODUCTION

FEATURES

The WM8952 is a low power audio ADC, with flexible line and microphone input. It offers great flexibility in use, and so can support many different modes of operation as follows:

MICROPHONE INPUTS

Two microphone inputs are provided, allowing for either a differential microphone input or a single ended microphone to be connected. These inputs have a user programmable gain range of -12dB to +35.25dB using internal resistors. After the input PGA stage comes a boost stage which can add a further 20dB of gain. A microphone bias is output from the chip which can be used to bias the microphones. The signal routing can be configured to allow manual adjustment of mic levels, or to allow the ALC loop to control the level of mic signal that is transmitted.

Total gain through the microphone paths of up to +55.25dB can be selected.

PGA AND ALC OPERATION

A programmable gain amplifier is provided in the input path to the ADC. This may be used manually or in conjunction with a mixed analogue/digital automatic level control (ALC) which keeps the recording volume constant.

AUX INPUT

The device includes a mono input, AUX, which can also be mixed into the signal path in a flexible fashion, either to the input PGA as a second microphone input or as a line input. The configuration of this circuit, with integrated on-chip resistors allows several analogue signals to be summed into the single AUX input if required.

ADC

The mono ADC uses a multi-bit high-order oversampling architecture to deliver optimum performance with low power consumption. Various sample rates are supported, from the 8ks/s rate typically used in voice dictation, up to the 48ks/s rate used in high quality audio applications.

DIGITAL FILTERING

Advanced Sigma Delta Converters are used along with digital decimation and interpolation filters to give high quality audio at sample rates from 8ks/s to 48ks/s.

Application specific digital filters are also available which help to reduce the effect of specific noise sources such as wind noise or narrowband noise from other parts of the system. The filters include a programmable ADC high pass filter and four fully programmable ADC notch filters.

AUDIO INTERFACES

The WM8952 has a standard audio interface, to support the transmission of audio data to and from the chip. This interface is a 4 wire standard audio interface which supports a number of audio data formats including I^2S, DSP Mode, MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes.

CONTROL INTERFACES

To allow full software control over all its features, the WM8952 supports 2 or 3 wire control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. The selection between 2-wire mode and 3-wire mode is determined by the state of the MODE / GPIO pin. If MODE / GPIO is high then 3-wire control mode is selected, if MODE is low then 2-wire control mode is selected.

In 2 wire mode, only slave operation is supported, and the address of the device is fixed as 0011010.

CLOCKING SCHEMES

WM8952 supports the normal audio clocking scheme operation, where 256fs MCLK is provided to the ADC.

However, a PLL is also included which may be used to generate the internal master clock frequency in the event that this is not available from the system controller. This PLL uses an input clock, typically the 12MHz USB or ilink clock, to generate high quality audio clocks. If this PLL is not required for generation of these clocks, it can be reconfigured to generate alternative clocks which

may then be output on the GPIO pin and used elsewhere in the system.

POWER CONTROL

The design of the WM8952 has given much attention to power consumption without compromising performance. It operates at low supply voltages, and includes the facility to power off any unused parts of the circuitry under software control.

As a power saving measure, ADC logic in the DSP core is held in its last enabled state when the ADC is disabled. In order to prevent pops and clicks on restart due to residual data in the filters, the master clock must remain for at least 64 input samples after the ADC has been disabled.

INPUT SIGNAL PATH

The WM8952 has 3 flexible analogue inputs: two microphone inputs, and an auxiliary input. These inputs can be used in a variety of ways. The input signal path before the ADC has a flexible PGA block which then feeds into a gain boost/mixer stage.

MICROPHONE INPUTS

The WM8952 can accommodate a variety of microphone configurations including single ended and differential inputs. The inputs through the MICN, MICP and optionally AUX pins are amplified through the input PGA as shown in Figure 6 .

A pseudo differential input is the preferential configuration where the positive terminal of the input PGA is connected to the MICP input pin by setting MICP2INPPGA=1. The microphone ground should then be connected to MICN (when MICN2INPPGA=1) or optionally to AUX (when AUX2INPPGA=1) input pins.

Alternatively a single ended microphone can be connected to the MICN input with MICN2INPPGA set to 1. The non-inverting terminal of the input PGA should be connected internally to VMID by setting MICP2INPPGA to 0.

In pseudo-differential mode the larger signal should be input to MICP and the smaller (e.g. noisy ground connections) should be input to MICN.

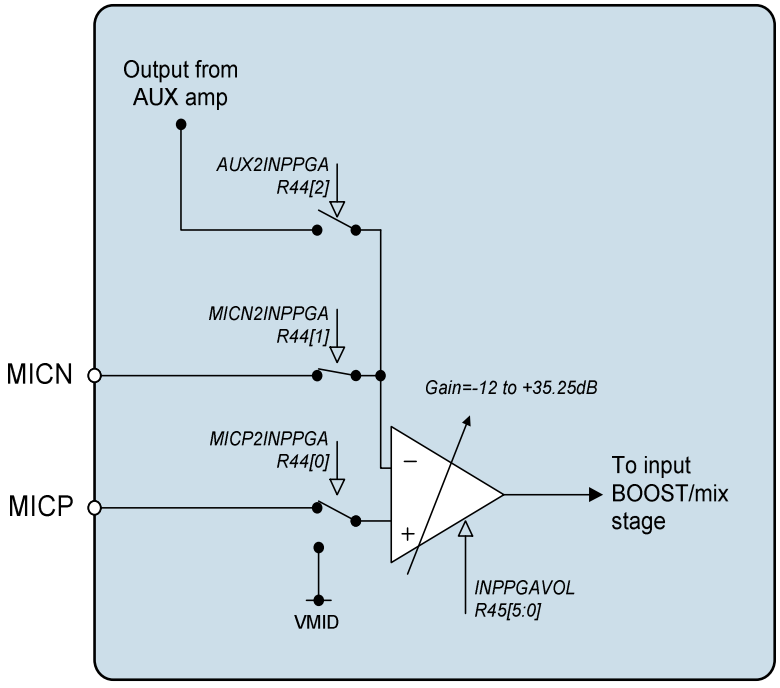


Figure 6 Microphone Input PGA Circuit (switch positions shown are for differential mic input)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 Input Control	2	AUX2INPPGA	0	Select AUX amplifier output as input PGA signal source. 0=AUX not connected to input PGA 1=AUX connected to input PGA amplifier negative terminal.
	1	MICN2INPPGA	1	Connect MICN to input PGA negative terminal. 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.
	0	MICP2INPPGA	0	Connect input PGA amplifier positive terminal to MICP or VMID. 0 = input PGA amplifier positive terminal connected to VMID 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string

Table 2 Input Control

The input PGA is enabled by the IPPGAEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power Management 2	2	INPPGAEN	0	Input microphone PGA enable 0 = disabled 1 = enabled

Table 3 Input PGA Enable Control

INPUT PGA VOLUME CONTROL

The input microphone PGA has a gain range from -12dB to +35.25dB in 0.75dB steps. The gain from the MICN input to the PGA output and from the AUX amplifier to the PGA output are always common and controlled by the register bits INPPGAVOL[5:0]. These register bits also affect the MICP pin when MICP2INPPGA=1.

When the Automatic Level Control (ALC) is enabled the input PGA gain is then controlled automatically and the INPPGAVOL bits should not be used.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 Input PGA volume control	7	INPPGAZC	0	Input PGA zero cross enable: 0=Update gain when gain register changes 1=Update gain on 1st zero cross after gain register write.
	6	INPPGAMUTE	1	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).
	5:0	INPPGAVOL	010000	Input PGA volume 000000 = -12dB 000001 = -11.25db . 010000 = 0dB . 111111 = 35.25dB
R32 ALC control 1	8	ALCSEL	0	ALC function select: 0=ALC off (PGA gain set by INPPGAVOL register bits) 1=ALC on (ALC controls PGA gain)

Table 4 Input PGA Volume Control

AUXILIARY INPUT

An auxiliary input circuit (Figure 7) is provided which consists of an amplifier which can be configured either as an inverting buffer for a single input signal or as a mixer/summer for multiple inputs with the use of external resistors. The circuit is enabled by the register bit AUXEN.

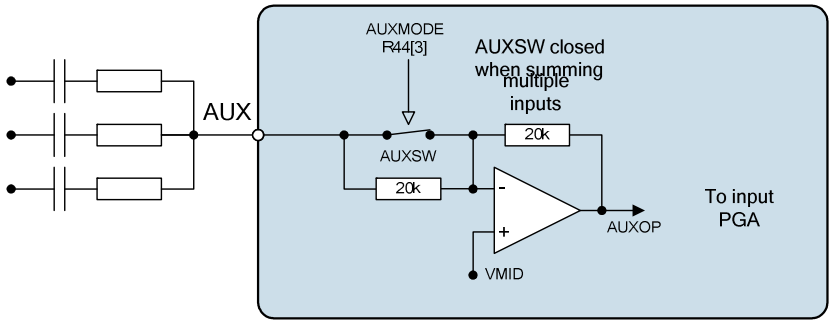


Figure 7 Auxiliary Input Circuit

The AUXMODE register bit controls the auxiliary input mode of operation:

In buffer mode (AUXMODE=0) the switch labelled AUXSW in Figure 7 is open and the signal at the AUX pin will be buffered and inverted through the aux circuit using only the internal components.

In mixer mode (AUXMODE=1) the on-chip input resistor is bypassed, this allows the user to sum in multiple inputs with the use of external resistors. When used in this mode there will be gain variations through this path from part to part due to the variation of the internal 20kΩ resistors relative to the higher tolerance external resistors.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	6	AUXEN	0	Auxiliary input buffer enable 0 = OFF 1 = ON
R44 Input control	3	AUXMODE	0	0 = inverting buffer 1 = mixer (on-chip input resistor bypassed)

Table 5 Auxiliary Input Buffer Control

INPUT BOOST

The input BOOST circuit has 3 selectable inputs: the input microphone PGA output, the AUX amplifier output and the MICP input pin (when not using a differential microphone configuration). These three inputs can be mixed together and have individual gain boost/adjust as shown in Figure 8.

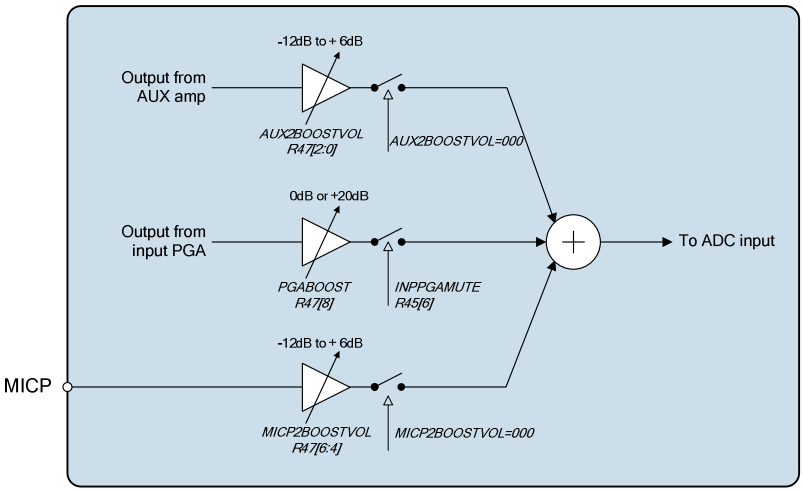


Figure 8 Input Boost Stage

The input PGA path can have a +20dB boost (PGABOOST=1) a 0dB pass through (PGABOOST=0) or be completely isolated from the input boost circuit (INPPGAMUTE=1).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 Input PGA gain control	6	INPPGAMUTE	1	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).
R47 Input BOOST control	8	PGABOOST	0	0 = PGA output has +0dB gain through input BOOST stage. 1 = PGA output has +20dB gain through input BOOST stage.

Table 6 Input BOOST Stage Control

The Auxiliary amplifier path to the BOOST stage is controlled by the AUX2BOOSTVOL[2:0] register bits. When AUX2BOOSTVOL=000 this path is completely disconnected from the BOOST stage. Settings 001 through to 111 control the gain in 3dB steps from -12dB to +6dB.

The MICP path to the BOOST stage is controlled by the MICP2BOOSTVOL[2:0] register bits. When MICP2BOOSTVOL=000 this input pin is completely disconnected from the BOOST stage. Settings 001 through to 111 control the gain in 3dB steps from -12dB to +6dB.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 Input BOOST control	6:4	MICP2BOOSTVOL	000	Controls the MICP pin to the input boost stage (NB, when using this path set MICP2INPPGA=0): 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage … 111=+6dB gain through boost stage
	2:0	AUX2BOOSTVOL	000	Controls the auxiliary amplifier to the input boost stage: 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage … 111=+6dB gain through boost stage

Table 7 Input BOOST Stage Control

The BOOST stage is enabled under control of the BOOSTEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power management 2	4	BOOSTEN	0	Input BOOST enable 0 = Boost stage OFF 1 = Boost stage ON

Table 8 Input BOOST Enable Control

MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via the MBVSEL register bit. When MBVSEL=0, MICBIAS=0.9*AVDD and when MBVSEL=1, MICBIAS=0.65*AVDD. The output can be enabled or disabled using the MICBEN control bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	4	MICBEN	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON

Table 9 Microphone Bias Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 Input Control	8	MBVSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD

Table 10 Microphone Bias Voltage Control

The internal MICBIAS circuitry is shown in Figure 9. Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

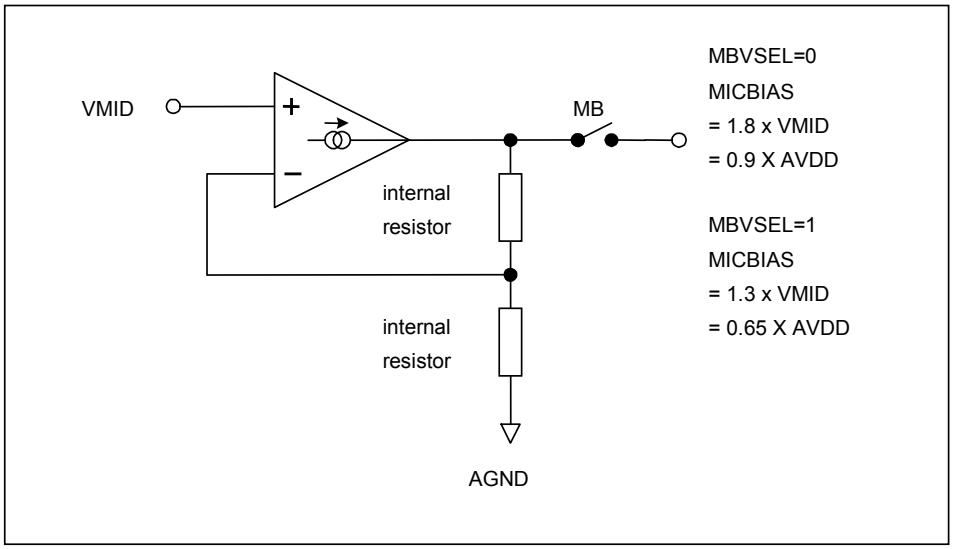


Figure 9 Microphone Bias Schematic

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8952 uses a multi-bit, oversampled sigma-delta ADC channel. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is $1.0V_{rms}$. Any voltage greater than full scale may overload the ADC and cause distortion.

ADC DIGITAL FILTERS

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path is illustrated in Figure 10.

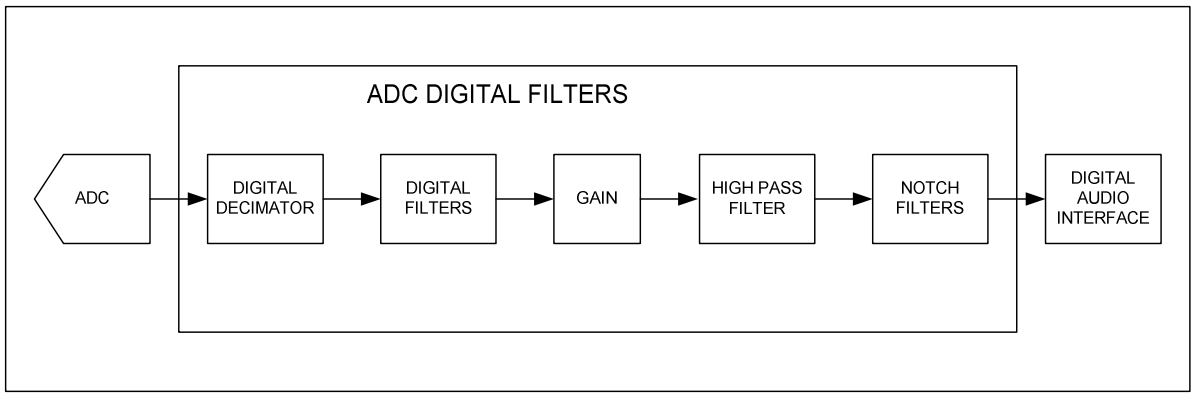


Figure 10 ADC Digital Filter Path

The ADC is enabled by the ADCEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power management 2	0	ADCEN	0	0 = ADC disabled 1 = ADC enabled

Table 11 ADC Enable

The polarity of the output signal can also be changed under software control using the ADCPOL register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 ADC Control	0	ADCPOL	0	0=normal 1=inverted

Table 12 ADC Polarity

SELECTABLE HIGH PASS FILTER

A selectable high pass filter is provided. To disable this filter set HPFEN=0. The filter has two modes controlled by HPFAPP. In Audio Mode (HPFAPP=0) the filter is first order, with a cut-off frequency of 3.7Hz. In Application Mode (HPFAPP=1) the filter is second order, with a cut-off frequency selectable via the HPFCUT register. The cut-off frequencies when HPFAPP=1 are shown in Table 14.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 ADC Control	8	HPFEN	1	High Pass Filter Enable 0=disabled 1=enabled
	7	HPFAPP	0	Select audio mode or application mode 0=Audio mode (1st order, fc = ~3.7Hz) 1=Application mode (2nd order, fc = HPFCUT)
	6:4	HPFCUT	000	Application mode cut-off frequency See Table 14 for details.

Table 13 ADC Filter Select

HPFCUT	FS (KHZ)								
	SR=101/100			SR=011/010			SR=001/000		
	8	11.025	12	16	22.05	24	32	44.1	48
000	82	113	122	82	113	122	82	113	122
001	102	141	153	102	141	153	102	141	153
010	131	180	196	131	180	196	131	180	196
011	163	225	245	163	225	245	163	225	245
100	204	281	306	204	281	306	204	281	306
101	261	360	392	261	360	392	261	360	392
110	327	450	490	327	450	490	327	450	490
111	408	563	612	408	563	612	408	563	612

Table 14 High Pass Filter Cut-off Frequencies (HPFAPP=1)

Note that the High Pass filter values (when HPFAPP=1) work on the basis that the SR register bits are set correctly for the actual sample rate as shown in Table 14.

PROGRAMMABLE NOTCH FILTERS

Four programmable notch filters are provided. These filters have a programmable centre frequency and bandwidth, programmable via two coefficients, a0 and a1. a0 and a1 are represented by the register bits NFx_A0[13:0] and NFx_A1[13:0]. The notch filter coefficients should be converted to sign / magnitude notation to enter into the registers. Notch Filter 3 can also be programmed as a 1st order low pass filter.

Because these coefficient values require two register writes to set up there is an NFx_UP (Notch Filter Update) flag for each filter which should be set only when both A0 and A1 for the filter have been set.

The notch filters can be individually enabled, using the corresponding NFx_EN register bit, as can be seen in Figure 11:

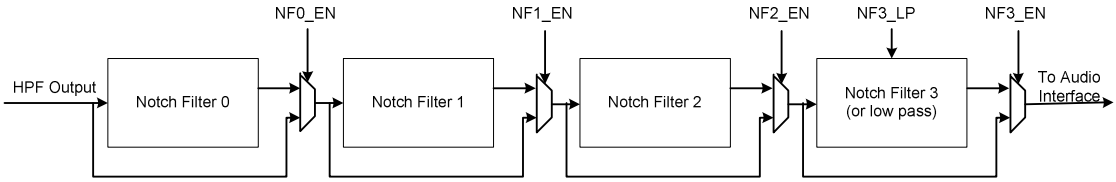


Figure 11 Labelling of Notch Filters and Arrangement of Notch Filter Enables

The notch filter coefficients must be entered using a sign / magnitude notation.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 Notch Filter 0A	15	NF0_UP	0	Notch filter 0 update. The notch filter 0 values used internally only update when one of the NF0_UP bits is set high.
	14	NF0_EN	0	Notch filter 0 enable: 0=Disabled 1=Enabled
	13:0	NF0_A0	0	Notch Filter 0 a0 coefficient
R17 Notch Filter 0B	15	NF0_UP	0	Notch filter 0 update. The notch filter 0 values used internally only update when one of the NF0_UP bits is set high.
	13:0	NF0_A1	0	Notch Filter 0 a1 coefficient

Table 15 Notch Filter 0 Function

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 Notch Filter 1A	15	NF1_UP	0	Notch filter 1 update. The notch filter 1 values used internally only update when one of the NFU bits is set high.
	14	NF1_EN	0	Notch Filter 1 enable. 0=Disabled 1=Enabled
	13:0	NF1_A0	0	Notch Filter 1 a0 coefficient
R19 Notch Filter 1B	15	NF1_UP	0	Notch filter 1 update. The notch filter 1 values used internally only update when one of the NFU bits is set high.
	13:0	NF1_A1	0	Notch Filter 1 a1 coefficient

Table 16 Notch Filter 1 Function

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 Notch Filter 2A	15	NF2_UP	0	Notch filter 2 update. The notch filter 2 values used internally only update when one of the NFU bits is set high.
	14	NF2_EN	0	Notch Filter 2 enable. 0=Disabled 1=Enabled
	13:0	NF2_A0	0	Notch Filter 2 a0 coefficient
R21 Notch Filter 2B	15	NF2_UP	0	Notch filter 2 update. The notch filter 2 values used internally only update when one of the NFU bits is set high.
	13:0	NF2_A1	0	Notch Filter 2 a1 coefficient

Table 17 Notch Filter 2 Function

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 Notch Filter 3A	15	NF3_UP	0	Notch filter 3 update. The notch filter 3 values used internally only update when one of the NFU bits is set high.
	14	NF3_EN	0	Notch Filter 3 enable. 0=Disabled 1=Enabled
	13:0	NF3_A0	0	Notch Filter 3 a0 coefficient
R23 Notch Filter 3B	15	NF3_UP	0	Notch filter 3 update. The notch filter 3 values used internally only update when one of the NFU bits is set high.
	14	NF3_LP	0	Notch Filter 3 mode select 0 = Notch Filter mode 1 = Low Pass Filter mode
	13:0	NF3_A1	0	Notch Filter 3 a1 coefficient

Table 18 Notch Filter 3 Function

The notch filter coefficients must be entered using a sign / magnitude notation. The MSB of the 14-bit register word (NFx_Ax[13]) is reserved for the sign part, leaving the 13 remaining bits for the magnitude part.

The notch filter coefficients are calculated as follows:

$$a_0 = \frac{1-\tan(w_b/2)}{1+\tan(w_b/2)}$$

Where:

$$w_0 = 2\pi f_c / f_s$$

$$w_b = 2\pi f_b / f_s$$

f_c = centre frequency in Hz, f_b = -3dB bandwidth in Hz, f_s = sample frequency in Hz

The actual register values can be determined from the coefficients as follows:

NFn_A0 = -a0 x 2^{13}

NFn_A1 = -a1 x 2^{12}

These values are then converted to a 14-bit sign / magnitude notation.

To configure Notch Filter 3 as a 1st order low pass filter, set the NF3_LP bit to 1 and calculate the coefficients as follows:

$$a_0 = 0$$

$$a_1 = \frac{\tan(w_c/2)-1}{\tan(w_c/2)+1}$$

Where:

$$w_c = 2\pi f_c / f_s$$

f_c = cut-off frequency in Hz, f_s = sample frequency in Hz

The actual register values can be determined from the coefficients as follows:

NF3_A0 = 0

NF3_A1 = -a_1 x2^{12}

These values are then converted to a 14-bit sign / magnitude notation.

DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally attenuated over a range from –127dB to 0dB in 0.5dB steps. The gain for a given eight-bit code X is given by:

Gain = 0.5 x (x–255) dB for $1 \leq x \leq 255$, MUTE for x = 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 ADC Digital Volume	7:0	ADCVOL [7:0]	11111111 (0dB)	ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB

Table 19 ADC Volume

INPUT LIMITER / AUTOMATIC LEVEL CONTROL (ALC)

The WM8952 has an automatic PGA gain control circuit, which can function as an input peak limiter or as an automatic level control (ALC).

The Automatic Level Control (ALC) provides continuous adjustment of the input PGA in response to the amplitude of the input signal. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level (ALCLVL).

If the signal is below the threshold, the ALC will increase the gain of the PGA at a rate set by ALCDCY. If the signal is above the threshold, the ALC will reduce the gain of the PGA at a rate set by ALCATK.

The ALC has two modes selected by the ALCMODE register: normal mode and peak limiter mode. The ALC/limiter function is enabled by setting the register bit R32[8] ALCSEL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ALC Control 1	2:0	ALCMIN [2:0]	000 (-12dB)	Set minimum gain of PGA 000 = -12dB 001 = -6dB 010 = 0dB 011 = +6dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +30dB
	5:3	ALCMAX [2:0]	111 (+35.25dB)	Set Maximum Gain of PGA 111 = +35.25dB 110 = +29.25dB 101 = +23.25dB 100 = +17.25dB 011 = +11.25dB 010 = +5.25dB 001 = -0.75dB 000 = -6.75dB
	8	ALCSEL	00	ALC function select 0 = ALC disabled 1 = ALC Enabled
R33 (21h) ALC Control 2	3:0	ALCLVL [3:0]	1011 (-6dB)	ALC target – sets signal level at ADC input 1111 = -1.5dBFS 1110 = -1.5dBFS 1101 = -3dBFS 1100 = -4.5dBFS 1011 = -6dBFS 1010 = -7.5dBFS 1001 = -9dBFS 1000 = -10.5dBFS 0111 = -12dBFS 0110 = -13.5dBFS 0101 = -15dBFS 0100 = -16.5dBFS 0011 = -18dBFS 0010 = -19.5dBFS 0001 = -21dBFS 0000 = -22.5dBFS

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td></td><td>7:4</td><td>ALCHLD
[3:0]</td><td>0000
(0ms)</td><td>ALC hold time before gain is increased.
0000 = 0ms
0001 = 2.67ms
0010 = 5.33ms
0011 = 10.66ms
0100 = 21.32ms
0101 = 42.64ms
0110 = 85.28ms
0111 = 0.17s
1000 = 0.34s
1001 = 0.68s
1010 or higher = 1.36s</td></tr>
<tr><td>R34 (22h)
ALC Control 3</td><td>8</td><td>ALCMODE</td><td>0</td><td>Determines the ALC mode of operation:
0 = ALC mode (Normal Operation)
1 = Limiter mode.</td></tr>
<tr><td></td><td>7:4</td><td>ALCDCY
[3:0]</td><td>0011
(26ms/6dB)</td><td>Decay (gain ramp-up) time
(ALCMODE ==0)
<table><tr><td></td><td>Per step</td><td>Per 6dB</td><td>90% of range</td></tr><tr><td>0000</td><td>410us</td><td>3.38ms</td><td>23.6ms</td></tr><tr><td>0001</td><td>820us</td><td>6.56ms</td><td>47.2ms</td></tr><tr><td>0010</td><td>1.64ms</td><td>13.1ms</td><td>94.5ms</td></tr><tr><td colspan="4">… (time doubles with every step)</td></tr><tr><td>1010 or higher</td><td>420ms</td><td>3.36s</td><td>24.2s</td></tr></table></td></tr>
<tr><td></td><td></td><td></td><td>0011
(5.8ms/6dB)</td><td>Decay (gain ramp-up) time
(ALCMODE ==1)
<table><tr><td></td><td>Per step</td><td>Per 6dB</td><td>90% of range</td></tr><tr><td>0000</td><td>90.8us</td><td>726us</td><td>5.23ms</td></tr><tr><td>0001</td><td>182us</td><td>1.45ms</td><td>10.5ms</td></tr><tr><td>0010</td><td>363us</td><td>2.91ms</td><td>20.9ms</td></tr><tr><td colspan="4">… (time doubles with every step)</td></tr><tr><td>1010</td><td>93ms</td><td>744ms</td><td>5.36s</td></tr></table></td></tr>
<tr><td></td><td>3:0</td><td>ALCATK
[3:0]</td><td>0010
(3.3ms/6dB)</td><td>ALC attack (gain ramp-down) time
(ALCMODE == 0)
<table><tr><td></td><td>Per step</td><td>Per 6dB</td><td>90% of range</td></tr><tr><td>0000</td><td>104us</td><td>832us</td><td>6ms</td></tr><tr><td>0001</td><td>208us</td><td>1.66ms</td><td>12ms</td></tr><tr><td>0010</td><td>416us</td><td>3.33ms</td><td>24ms</td></tr><tr><td colspan="4">… (time doubles with every step)</td></tr><tr><td>1010 or higher</td><td>106ms</td><td>852ms</td><td>6.13s</td></tr></table></td></tr>
<tr><td></td><td></td><td></td><td>0010
(726us/6dB)</td><td>ALC attack (gain ramp-down) time
(ALCMODE == 1)
<table><tr><td></td><td>Per step</td><td>Per 6dB</td><td>90% of range</td></tr><tr><td>0000</td><td>22.7us</td><td>182.4us</td><td>1.31ms</td></tr><tr><td>0001</td><td>45.4us</td><td>363us</td><td>2.62ms</td></tr><tr><td>0010</td><td>90.8us</td><td>726us</td><td>5.23ms</td></tr><tr><td colspan="4">… (time doubles with every step)</td></tr><tr><td>1010 or higher</td><td>23.2ms</td><td>186ms</td><td>1.34s</td></tr></table></td></tr>
</table>

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2Ah) ALC Control 4	1	ALCZC	0 (zero cross off)	ALC uses zero cross detection circuit. 0 = Disabled (recommended) 1 = Enabled

Table 20 ALC Control Registers

When the ALC is disabled, the input PGA remains at the last controlled value of the ALC. An input gain update must be made by writing to the INPPGAVOLL/R register bits.

If there is no analogue input signal present when the ALC is enabled, the ALC may not function correctly. To ensure correct operation of the ALC with no analogue input signal, the Input PGA Volume control register (R45) should be written with the INPPGAMUTE and ALCZC bits set to 0 before setting the ALCSEL bit to 1 in register R32 (bit 8).

NORMAL MODE

In normal mode, the ALC will attempt to maintain a constant signal level by increasing or decreasing the gain of the PGA. The following diagram shows an example of this.

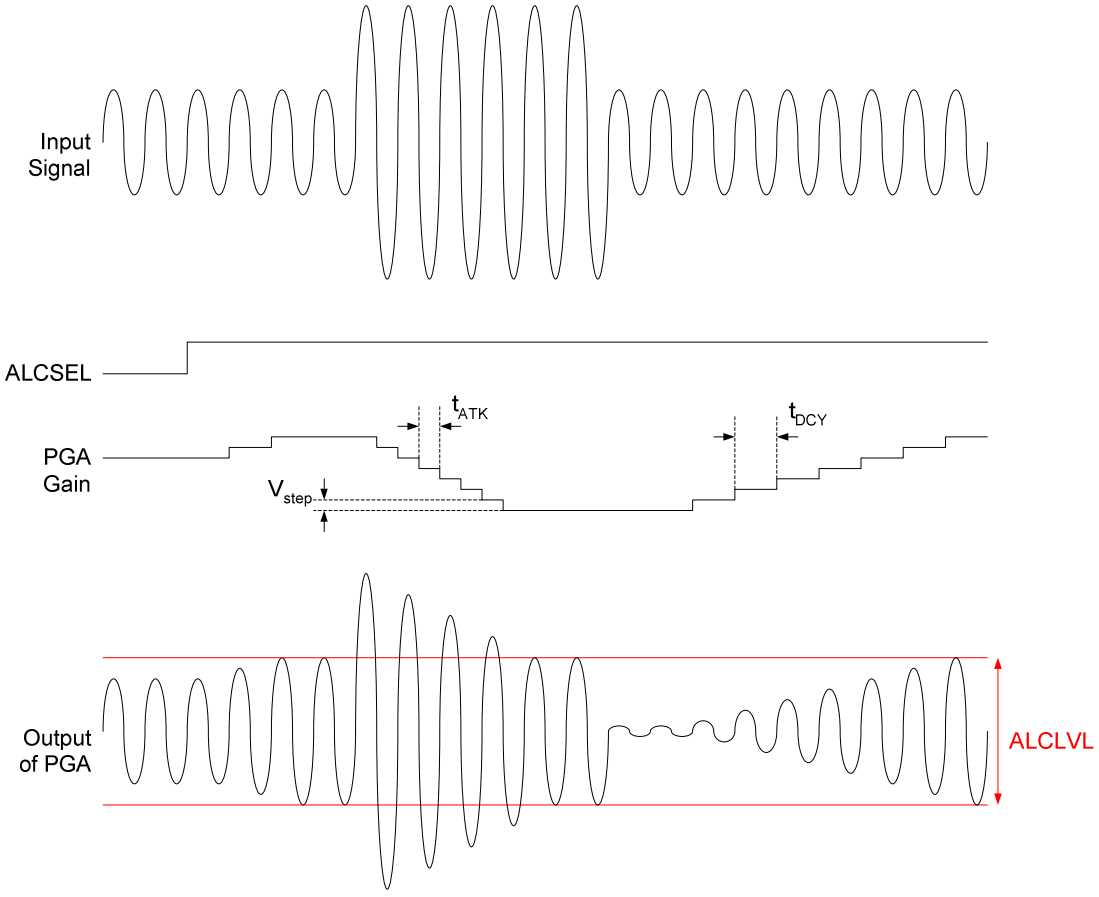


Figure 12 ALC Normal Mode Operation

LIMITER MODE

In limiter mode, the ALC will reduce peaks that go above the threshold level, but will not increase the PGA gain beyond the starting level. The starting level is the PGA gain setting when the ALC is enabled in limiter mode. If the ALC is started in limiter mode, this is the gain setting of the PGA at start-up. If the ALC is switched into limiter mode after running in ALC mode, the starting gain will be the gain at switchover. The diagram below shows an example of limiter mode.

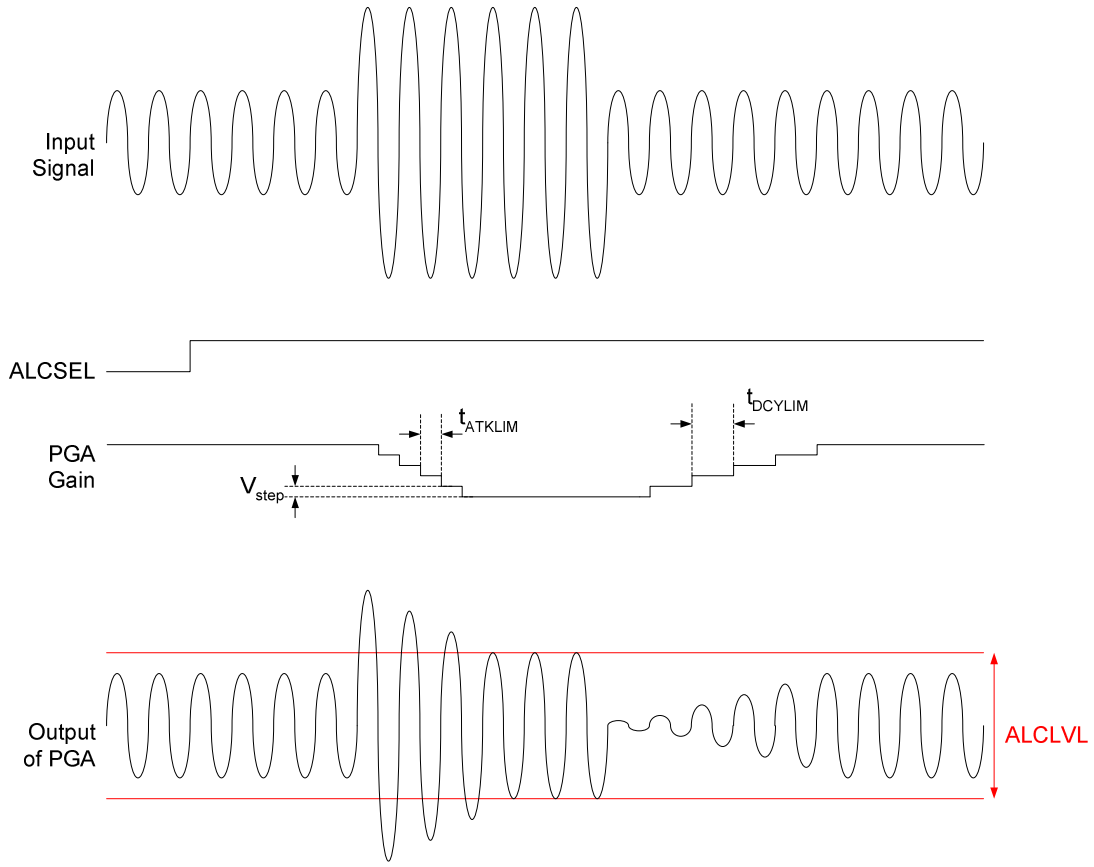


Figure 13 ALC Limiter Mode Operation

ATTACK AND DECAY TIMES

The attack and decay times set the update times for the PGA gain. The attack time is the time constant used when the gain is reducing. The decay time is the time constant used when the gain is increasing. In limiter mode, the time constants are faster than in ALC mode. The time constants are shown below in terms of a single gain step, a change of 6dB and a change of 90% of the PGAs gain range.

Note that, these times will vary slightly depending on the sample rate used (specified by the SR register).

NORMAL MODE

ALCMODE = 0 (Normal Mode)			
	Attack Time (s)		
ALCATK	t_{ATK}	t_{ATK6dB}	$t_{ATK90\%}$
0000	104µs	832µs	6ms
0001	208µs	1.66ms	12ms
0010	416µs	3.33ms	24ms
0011	832µs	6.66ms	48ms
0100	1.66ms	13.3ms	96ms
0101	3.33ms	26.6ms	192ms
0110	6.66ms	53.2ms	384ms
0111	13.3ms	106ms	767ms
1000	26.6ms	213.2ms	1.53s
1001	53.2ms	426ms	3.07s
1010	106ms	852ms	6.13s

ALCMODE = 0 (Normal Mode)			
	Decay Time (s)		
ALCDCY	t_{DCY}	t_{DCY6dB}	$t_{DCY90\%}$
0000	410µs	3.28ms	23.6ms
0001	820µs	6.56ms	47.2ms
0010	1.64ms	13.1ms	94.5ms
0011	3.28ms	26.2ms	189ms
0100	6.56ms	52.5ms	378ms
0101	13.1ms	105ms	756ms
0110	26.2ms	210ms	1.51s
0111	52.5ms	420ms	3.02s
1000	105ms	840ms	6.05s
1001	210ms	1.68s	12.1s
1010	420ms	3.36s	24.2s

Table 21 ALC Normal Mode (Attack and Decay times)

LIMITER MODE

ALCMODE = 1 (Limiter Mode)			
	Attack Time (s)		
ALCATK	t_{ATKLIM}	$t_{ATKLIM6dB}$	$t_{ATKLIM90\%}$
0000	22.7µs	182µs	1.31ms
0001	45.4µS	363µs	2.62ms
0010	90.8µS	726µs	5.23ms
0011	182µS	1.45ms	10.5ms
0100	363µS	2.91ms	20.9ms
0101	726µS	5.81ms	41.8ms
0110	1.45ms	11.6ms	83.7ms
0111	2.9ms	23.2ms	167ms
1000	5.81ms	46.5ms	335ms
1001	11.6ms	93ms	669ms
1010	23.2ms	186ms	1.34s

ALCMODE = 1 (Limiter Mode)			
	Attack Time (s)		
ALCDCY	t_{DCYLIM}	$t_{DCYLIM6dB}$	$t_{DCYLIM90\%}$
0000	90.8µs	726µs	5.23ms
0001	182µS	1.45ms	10.5ms
0010	363µS	2.91ms	20.9ms
0011	726µS	5.81ms	41.8ms
0100	1.45ms	11.6ms	83.7ms
0101	2.91ms	23.2ms	167ms
0110	5.81ms	46.5ms	335ms
0111	11.6ms	93ms	669ms
1000	23.2ms	186ms	1.34s
1001	46.5ms	372ms	2.68s
1010	93ms	744ms	5.36s

Table 22 ALC Limiter Mode (Attack and Decay times)

MINIMUM AND MAXIMUM GAIN

The ALCMIN and ALCMAX register bits set the minimum/maximum gain value that the PGA can be set to whilst under the control of the ALC. This has no effect on the PGA when ALC is not enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32	5:3	ALCMAX	111	Set Maximum Gain of PGA
ALC Control 1	2:0	ALCMIN	000	Set minimum gain of PGA

Table 23 ALC Max/Min Gain

In normal mode, ALCMAX sets the maximum boost which can be applied to the signal. In limiter mode, ALCMAX will normally have no effect (assuming the starting gain value is less than the maximum gain specified by ALCMAX) because the maximum gain is set at the starting gain level.

ALCMIN sets the minimum gain value which can be applied to the signal.

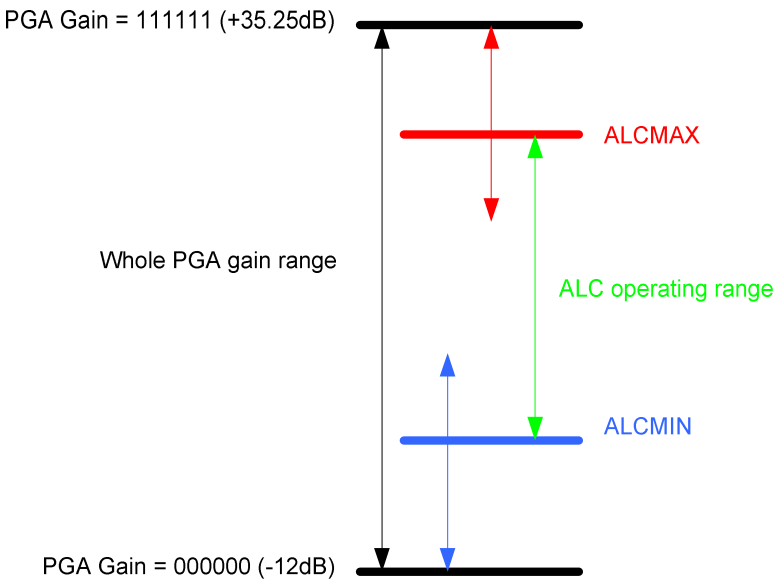


Figure 14 ALC Min/Max Gain

ALCMAX	Maximum Gain (dB)
111	35.25
110	29.25
101	23.25
100	17.25
011	11.25
010	5.25
001	-0.75
000	-6.75

Table 24 ALC Max Gain Values

ALCMIN	Minimum Gain (dB)
000	-12
001	-6
010	0
011	6
100	12
101	18
110	24
111	30

Table 25 ALC Min Gain Values

Note that if the ALC gain setting strays outside the ALC operating range, either by starting the ALC outside of the range or changing the ALCMAX or ALCMIN settings during operation, the ALC will immediately adjust the gain to return to the ALC operating range. It is recommended that the ALC starting gain is set between the ALCMAX and ALCMIN limits.

ALC HOLD TIME (NORMAL MODE ONLY)

In Normal mode, the ALC has an adjustable hold time which sets a time delay before the ALC begins its decay phase (gain increasing). The hold time is set by the ALCHLD register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R33 ALC Control 2	7:4	ALCHLD	0000	ALC hold time before gain is increased.

Table 26 ALC Hold Time

If the hold time is exceeded this indicates that the signal has reached a new average level and the ALC will increase the gain to adjust for that new average level. If the signal goes above the threshold during the hold period, the hold phase is abandoned and the ALC returns to normal operation.

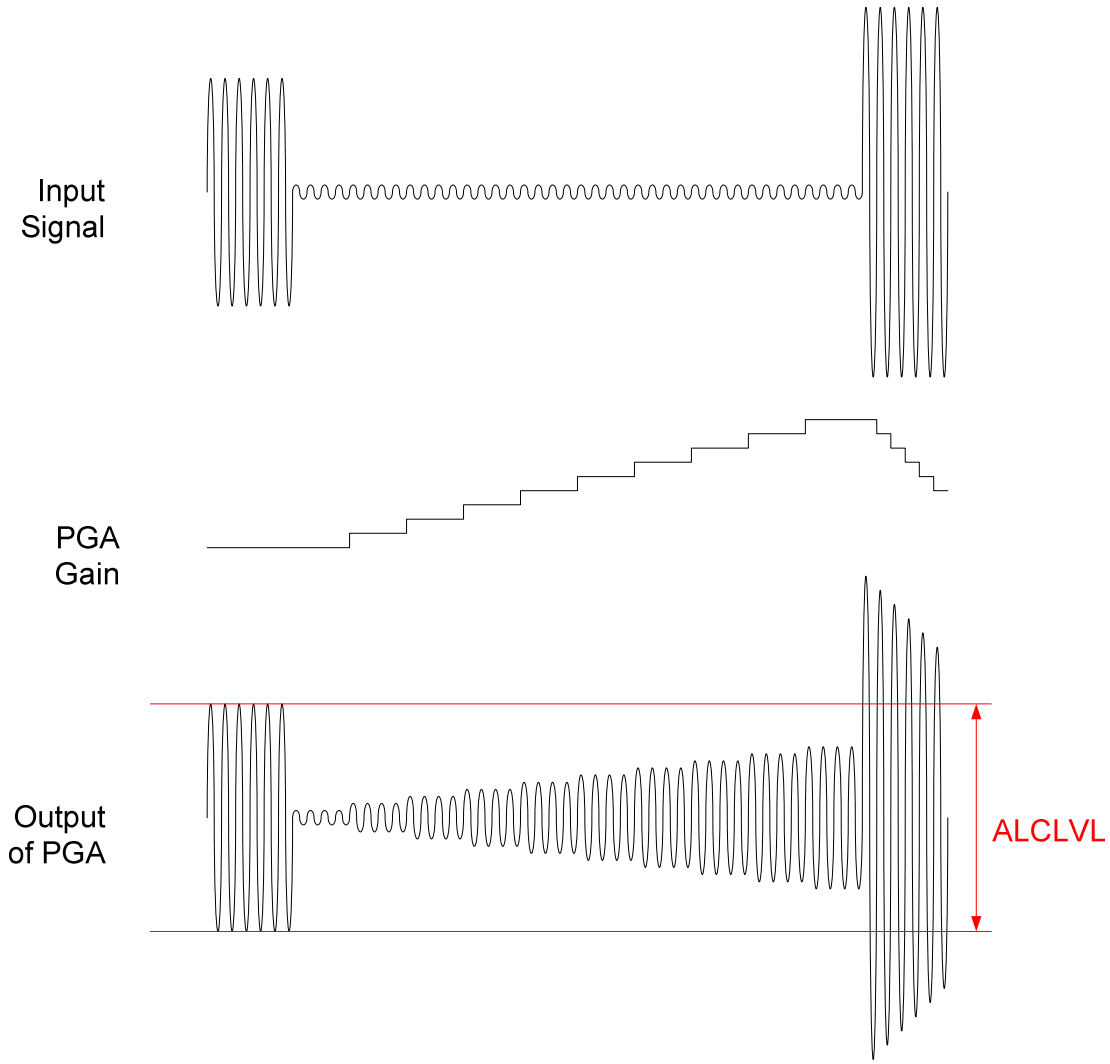


Figure 15 ALCLVL

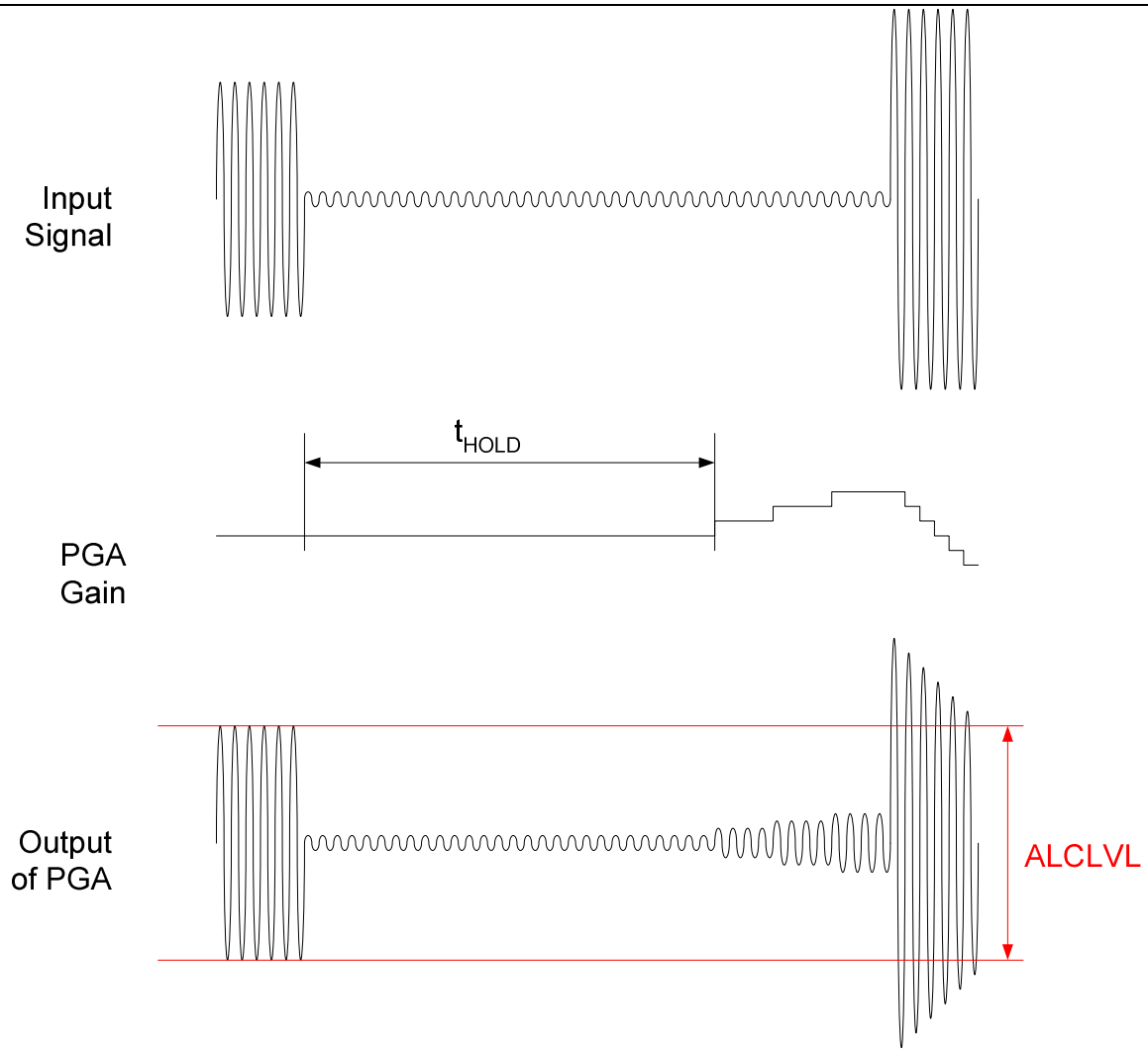


Figure 16 ALC Hold Time

ALCHLD	t_{HOLD} (s)
0000	0
0001	2.67ms
0010	5.34ms
0011	10.7ms
0100	21.4ms
0101	42.7ms
0110	85.4ms
0111	171ms
1000	342ms
1001	684ms
1010	1.37s

Table 27 ALC Hold Time Values

PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (–1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ALCATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

Note: If ALCATK = 0000, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

NOISE GATE (NORMAL MODE ONLY)

When the signal is very quiet and consists mainly of noise, the ALC function may cause “noise pumping”, i.e. loud hissing noise during silence periods. The WM8952 has a noise gate function that prevents noise pumping by comparing the signal level at the input pins against a noise gate threshold, NGTH. The noise gate cuts in when:

Signal level at ADC [dBFS] < NGTH [dBFS] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

Signal level at input pin [dBFS] < NGTH [dBFS]

The PGA gain is then held constant (preventing it from ramping up as it normally would when the signal is quiet).

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 6dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set–up of the function. The noise gate only operates in conjunction with the ALC and cannot be used in limiter mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 (23h) ALC Noise Gate Control	2:0	NGTH	000	Noise gate threshold: 000 = -39dB 001 = -45dB 010 = -51db 011 = -57dB 100 = -63dB 101 = -69dB 110 = -75dB 111 = -81dB
	3	NGATEN	0	Noise gate function enable 1 = enable 0 = disable

Table 28 ALC Noise Gate Control

The diagrams below show the response of the system to the same signal with and without noise gate.

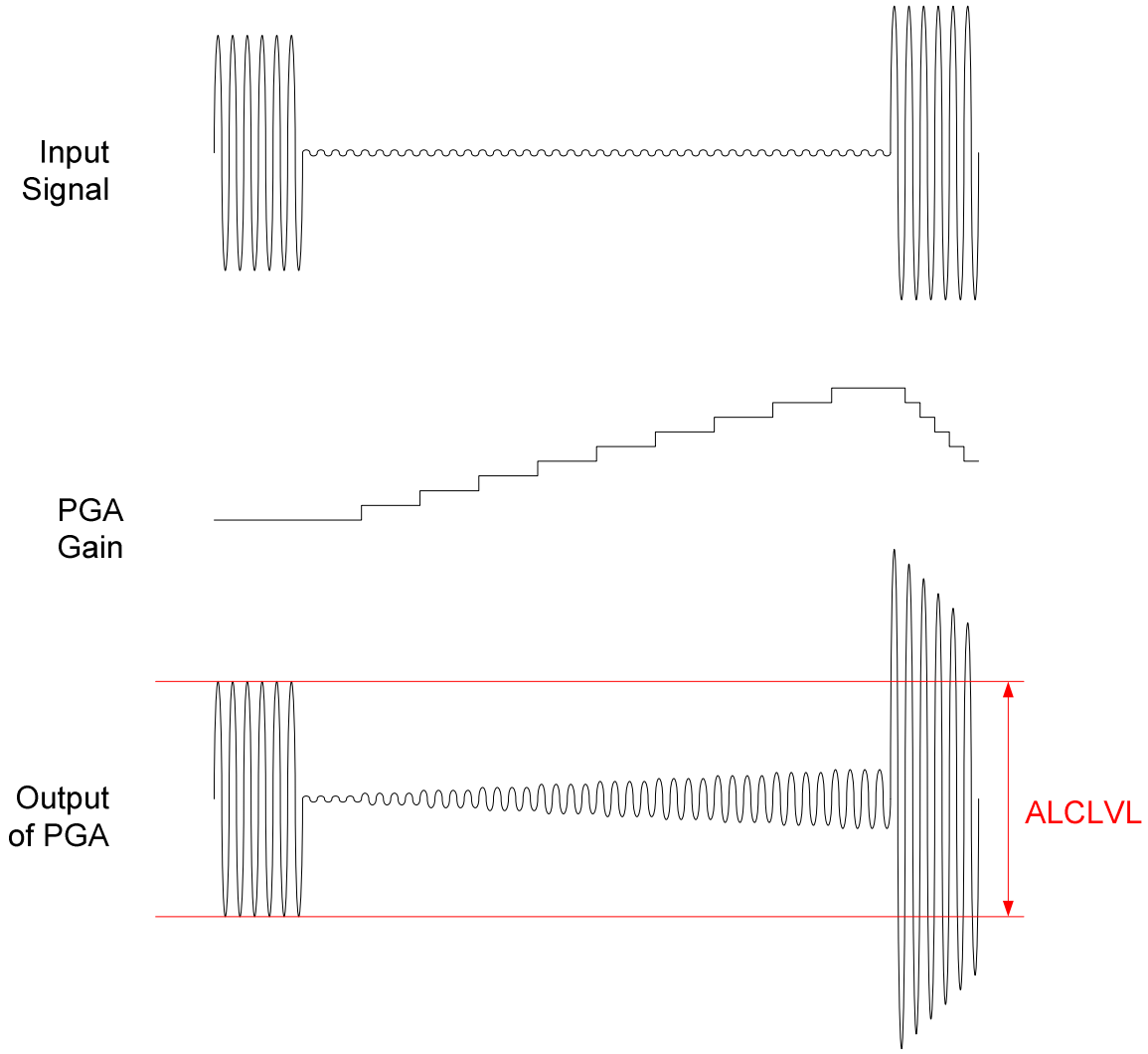


Figure 17 ALC Operation Above Noise Gate Threshold

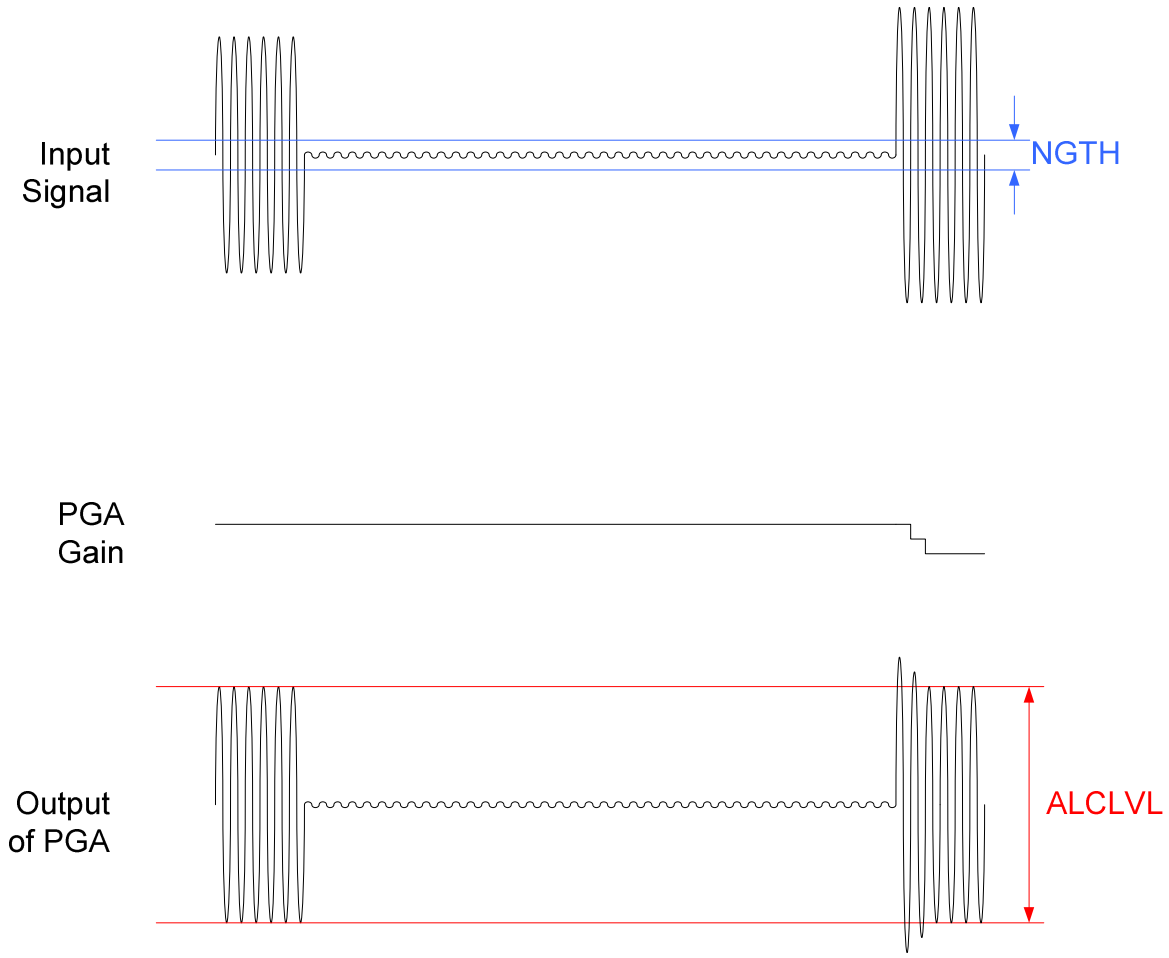


Figure 18 Noise Gate Operation

DIGITAL AUDIO INTERFACES

The audio interface has 3 pins:

- ADCDAT: ADC data output
- FRAME: Data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK and FRAME can be outputs when the WM8952 operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- I^2S
- DSP mode A / B

All of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

MASTER AND SLAVE MODE OPERATION

The WM8952 audio interface may be configured as either master or slave. As a master interface device the WM8952 generates BCLK and FRAME and thus controls sequencing of the data transfer on ADCDAT. To set the device to master mode register bit MS should be set high. In slave mode (MS=0), the WM8952 responds with data to clocks it receives over the digital audio interfaces.

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an FRAME transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each FRAME transition.

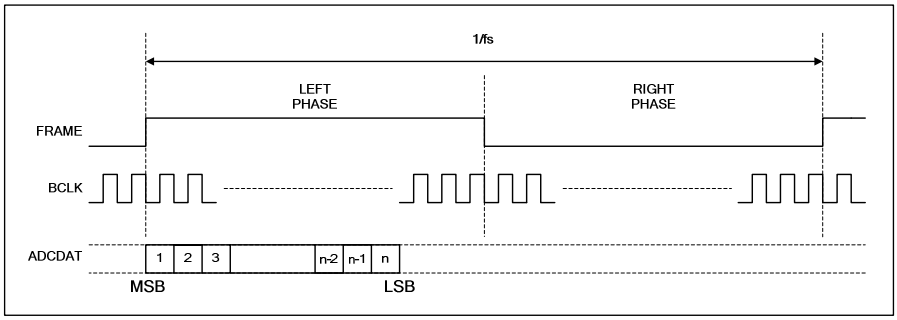


Figure 19 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a FRAME transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each FRAME transition.

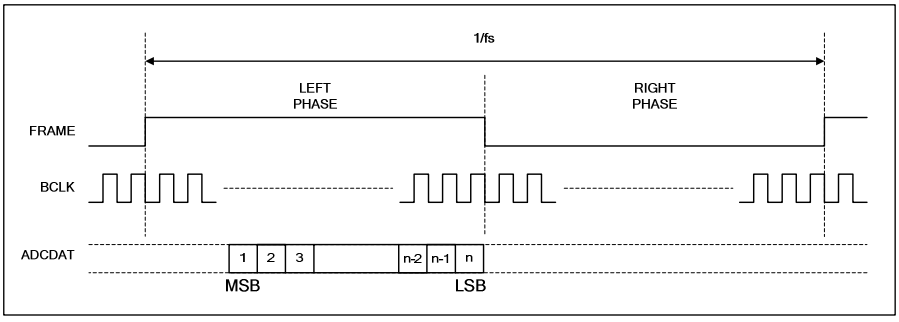


Figure 20 Right Justified Audio Interface (assuming n-bit word length)

In I²S mode, the MSB is available on the second rising edge of BCLK following a FRAME transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

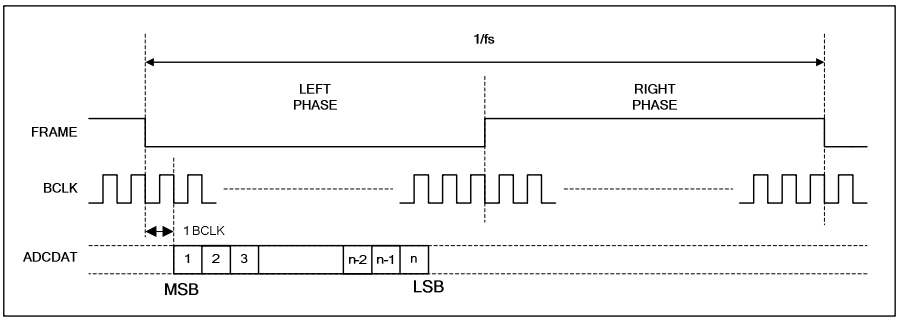


Figure 21 I²S Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1st (Mode B) the 2nd (Mode A) rising edge of BCLK (selectable by FRAMEP) following a rising edge of FRAME. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample. FRAMEP should be set to 0 in this mode.

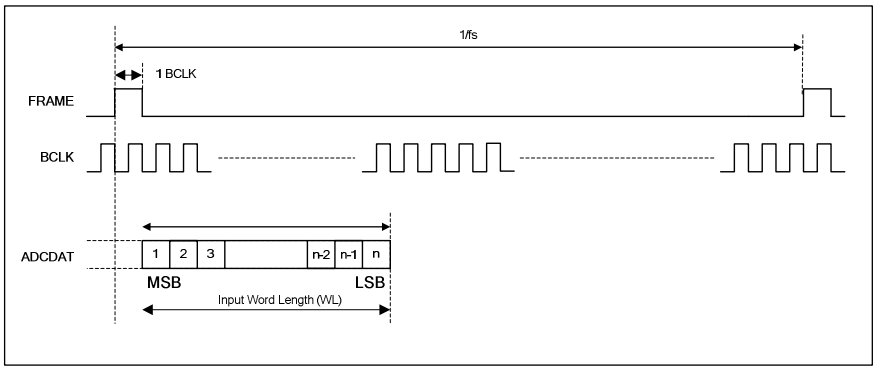


Figure 22 DSP/PCM Mode Audio Interface (Mode A, FRAMEP=0)

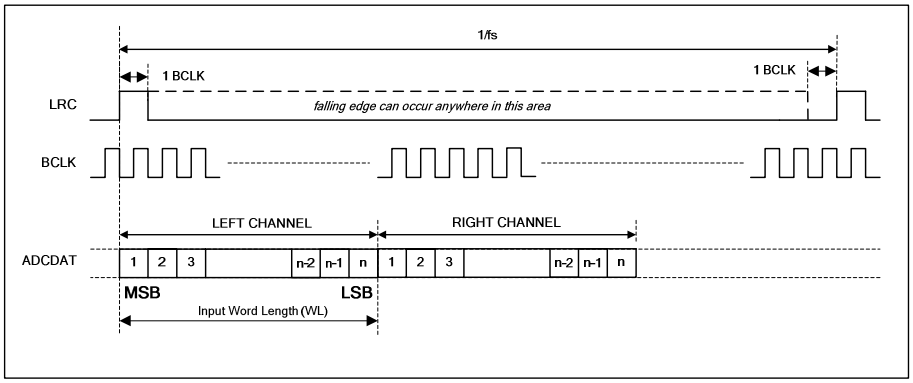


Figure 23 DSP/PCM Mode Audio Interface (Mode B, FRAMEP=1)

AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised below.

Register bit MS selects audio interface operation in master or slave mode. In Master mode BCLK, and FRAME are outputs. The frequency of BCLK and FRAME in master mode are controlled with BCLKDIV. These are divided down versions of master clock. This may result in short BCLK pulses at the end of a frame if there is a non-integer ratio of BCLKs to FRAME clocks.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 Audio interface control	9	LOUTR	0	LOUTR control 0=normal 1=Input mono channel data output on both left and right channels
	8	BCP	0	BCLK polarity 0=normal 1=inverted
	7	FRAMEP	0	Frame clock polarity (for RJ, LJ and I^2S formats) 0=normal 1=inverted DSP Mode control 1 = Configures interface so that MSB is available on 1st BCLK rising edge after FRAME rising edge 0 = Configures interface so that MSB is available on 2nd BCLK rising edge after FRAME rising edge
	6:5	WL	10	Word length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits (see note)
	4:3	FMT	10	Audio interface Data Format Select: 00=Right Justified 01=Left Justified 10=I^2S format 11= DSP/PCM mode
	1	ALRSWAP	0	Controls whether ADC data appears in 'right' or 'left' phases of FRAME clock: 0=ADC data appear in 'left' phase of FRAME 1=ADC data appears in 'right' phase of FRAME
R5 Companding Control	5	WL8	0	8 Bit Word Length Enable Only recommended for use with companding 0=Word Length controlled by WL 1=8 bits

Table 29 Audio Interface Control

Note: Right Justified Mode will only operate with a maximum of 24 bits. If 32-bit mode is selected the device will operate in 24-bit mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 Clock generation control	8	CLKSEL	1	Controls the source of the clock for all internal operation: 0=MCLK 1=PLL output
	7:5	MCLKDIV	010	Sets the scaling for either the MCLK or PLL clock output (under control of CLKSEL) 000=divide by 1 001=divide by 1.5 010=divide by 2 011=divide by 3 100=divide by 4 101=divide by 6 110=divide by 8 111=divide by 12
	4:2	BCLKDIV	000	Configures the BCLK and FRAME output frequency, for use when the chip is master over BCLK. 000=divide by 1 (BCLK=MCLK) 001=divide by 2 (BCLK=MCLK/2) 010=divide by 4 011=divide by 8 100=divide by 16 101=divide by 32 110=reserved 111=reserved
	0	MS	0	Sets the chip to be master over FRAME and BCLK 0=BCLK and FRAME clock are inputs 1=BCLK and FRAME clock are outputs generated by the WM8952 (MASTER)

Table 30 Clock Control

AUDIO SAMPLE RATES

The WM8952 sample rates are set using the SR register bits. The cut-offs for the digital filters and the ALC attack/decay times stated are determined using these values and assume a 256fs master clock rate.

If a sample rate that is not explicitly supported by the SR register settings is required then the closest SR value to that sample rate should be chosen, the filter characteristics and the ALC attack, decay and hold times will scale appropriately.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Additional control	3:1	SR	000	Approximate sample rate (configures the coefficients for the internal digital filters): 000=48kHz 001=32kHz 010=24kHz 011=16kHz 100=12kHz 101=8kHz 110-111=reserved

Table 31 Sample Rate Control

MASTER CLOCK AND PHASE LOCKED LOOP (PLL)

The WM8952 has an on-chip phase-locked loop (PLL) circuit that can be used to:

- Generate master clocks for the WM8952 audio functions from another external clock, e.g. in telecoms applications.
- Generate an output clock, on GPIO, for another part of the system (derived from an existing audio master clock).

Table 32 shows the PLL and internal clocking arrangement on the WM8952.

The PLL is enabled or disabled by the PLLEN register bit.

Note: In order to minimise current consumption, the PLL is disabled when the VMIDSEL[1:0] bits are set to 00b. VMIDSEL[1:0] must be set to a value other than 00b to enable the PLL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power Management 1	5	PLLEN	0	PLL enable 0=PLL off 1=PLL on

Table 32 PLLEN Control Bit

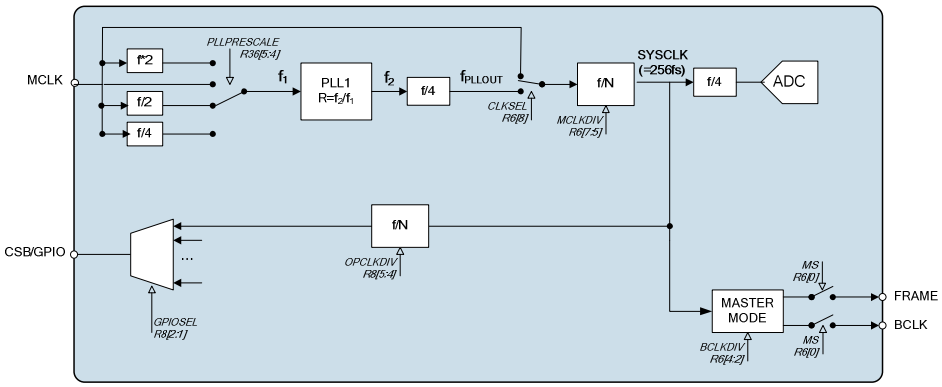


Figure 24 PLL and Clock Select Circuit

The PLL frequency ratio R = f_2/f_1 (see Table 33) can be set using the register bits PLLK and PLLN:

$N = \text{int } R$

$K = \text{int } (2^{24} (R - N))$

N controls the ratio of the division, and K the fractional part.

The PLL output then passes through a fixed divide by 4, and can also be further divided by MCLKDIV[3:0] (see Figure 24). The divided clock (SYSCLK) can be used to clock the WM8952 DSP core.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R36 PLL N value	7	PLL_POWERDOWN	0	PLL POWER 0=ON 1=OFF
	6	FRACEN	1	Fractional Divide within the PLL 0=Disabled (Lower Power) 1=Enabled
	5:4	PLLPRESCALE	00	00 = MCLK input multiplied by 2 (default) 01 = MCLK input not divided 10 = Divide MCLK by 2 before input to PLL 11 = Divide MCLK by 4 before input to PLL
	3:0	PLLN	1000	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.
R37 PLL K value 1	5:0	PLLK [23:18]	0Ch	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).
R38 PLL K Value 2	8:0	PLLK [17:9]	093h	
R39 PLL K Value 3	8:0	PLLK [8:0]	0E9h	

Table 33 PLL Frequency Ratio Control

INTEGER N DIVISION

The integer division ratio (N) is determined by N[3:0] and must be in the range 5 to 12 .

If the PLL frequency is an exact integer (5,6,7,8,9,10,11,12) then FRAC_EN can be set to 0 for low power operation.

INPUT CLOCK (F_1)	DESIRED PLL OUTPUT (F_2)	DIVISION REQUIRED (R)	FRACTIONAL DIVISION (K)	INTEGER DIVISION (N)	SDM
11.2896MHz	90.3168MHz	8	0	8	0
12.2880MHz	98.3040MHz	8	0	8	0

Table 34 PLL Modes of Operation (Integer N mode)

FRACTIONAL K MODE

The Fractional K bits provides K[23:0] provide finer divide resolution for the PLL frequency ratio (up to $1/2^{24}$). If these are used then FRAC_EN must be set. The relationship between the required division X, the fractional division K[23:0] and the integer division N[3:0] is:

$K = 2^{24} (R – N)$

where $0 < (R – N) < 1$ and K is rounded to the nearest whole number.

EXAMPLE:

PLL input clock (f_1) is 12MHz and the required clock (SYSCLK) is 12.288MHz.

R should be chosen to ensure 5 < N < 13. There is a fixed divide by 4 in the PLL and a selectable divider (MCLKDIV[3:0]) after the PLL which should be set to divide by 2 to meet this requirement.

Enabling the divide by 2 sets the required f_2 = 4 * 2 * 12.288MHz = 98.304MHz.

R = 98.304 / 12 = 8.192

N = int R = 8

K = int (2^{24} x (8.192 – 8)) = 3221225 = 3126E9h

So N[3:0] will be 8h and K[23:0] will be 3126E9h to produce the desired 98.304MHz clock.

The PLL performs best when f_2 is around 90MHz. Its stability peaks at N=8. Some example settings are shown in Table 35.

MCLK (MHz)	**DESIRED OUTPUT** (MHz)	**F2** (MHz)	**PRESCALE DIVIDE**	**POSTSCALE DIVIDE (MCLKDIV)**	**R**	**N** (Hex)	**K** (Hex)
12	11.2896	90.3168	1	2	7.5264	7	86C226
12	12.2880	98.3040	1	2	8.192	8	3126E9
13	11.2896	90.3168	1	2	6.947446	6	F28BD4
13	12.2880	98.3040	1	2	7.561846	7	8FD525
14.4	11.2896	90.3168	1	2	6.272	6	45A1CA
14.4	12.2880	98.3040	1	2	6.826667	6	D3A06E
19.2	11.2896	90.3168	2	2	9.408	9	6872B0
19.2	12.2880	98.3040	2	2	10.24	A	3D70A3
19.68	11.2896	90.3168	2	2	9.178537	9	2DB492
19.68	12.2880	98.3040	2	2	9.990243	9	FD809F
19.8	11.2896	90.3168	2	2	9.122909	9	1F76F8
19.8	12.2880	98.3040	2	2	9.929697	9	EE009E
24	11.2896	90.3168	2	2	7.5264	7	86C226
24	12.2880	98.3040	2	2	8.192	8	3126E9
26	11.2896	90.3168	2	2	6.947446	6	F28BD4
26	12.2880	98.3040	2	2	7.561846	7	8FD525
27	11.2896	90.3168	2	2	6.690133	6	BOAC93
27	12.2880	98.3040	2	2	7.281778	7	482296

Table 35 PLL Frequency Examples

COMPANDING

The WM8952 supports A-law and μ-law companding. This can be enabled by writing the appropriate value to the ADC_COMP register bit. If packed mode companding is desired the WL8 register bit is available. It will override the normal audio interface WL bits to give an 8-bit word length. Refer to Table 29 Audio Interface Control for setting the output word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 Companding control	2:1	ADC_COMP	0	ADC companding 00=off 01=reserved 10=μ-law 11=A-law

Table 36 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

μ-law (where μ=255 for the U.S. and Japan):

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu)$ $\quad -1 \le x \le 1$

A-law (where A=87.6 for Europe):

$F(x) = A|x| / (1 + \ln A)$ } for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ } for $1/A \le x \le 1$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ-law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSB's of data.

Companding converts 13 bits (μ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. The input data range is separated into 8 levels, allowing low amplitude signals better precision than that of high amplitude signals. This is to exploit the operation of the human auditory system, where louder sounds do not require as much resolution as quieter sounds. The companded signal is an 8-bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits).

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 37 8-bit Companded Word Composition

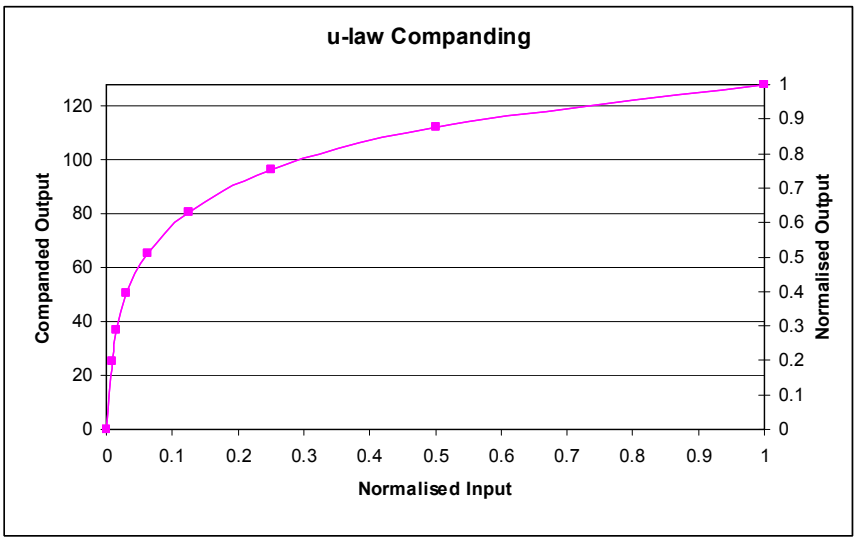


Figure 25 u-Law Companding

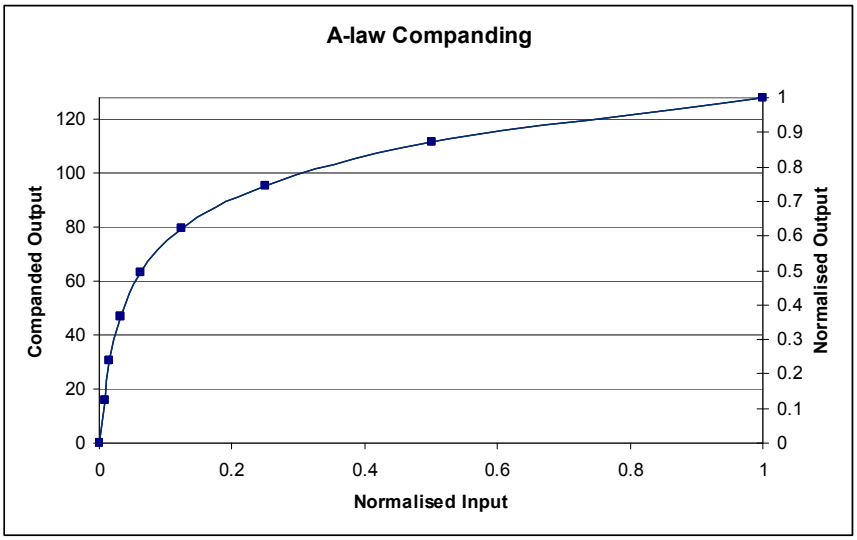


Figure 26 A-Law Companding

GENERAL PURPOSE INPUT/OUTPUT

In 2-wire mode, the CSB pin is not required and it can be used as a GPIO pin. In the WM8952, a separate GPIO pin is available and this can be used for GPIO in 3-wire mode. Also in 3 wire mode, the MODE / GPIO can be configured as a GPIO by setting the MODE_GPIO register bit

Whichever pin is used for GPIO, it is controlled from the GPIO control register R8. The GPIOSEL bits allow the chosen pin to be configured to perform a variety of useful tasks as shown in Table 38

Note that SLOWCLKEN must be enabled when using the jack detect function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 GPIO control	5:4	OPCLKDIV	00	PLL Output clock division ratio 00=divide by 1 01=divide by 2 10=divide by 3 11=divide by 4
	3	GPIOPOL	0	GPIO Polarity invert 0=Non inverted 1=Inverted
	2:0	GPIOSEL	000	GPIO function select: 000=GPIO off 010=Temp ok 100=SYSCLK clock o/p 101=PLL lock All other values: Reserved

Table 38 GPIO Control

CONTROL INTERFACE

SELECTION OF CONTROL MODE AND 2-WIRE MODE ADDRESS

The control interface can operate as either a 3-wire or 2-wire interface. The MODE / GPIO pin determines the 2 or 3 wire mode as shown in Table 39.

The WM8952 is controlled by writing to registers through a serial control interface. A control word consists of 24 bits. The first 7 bits (B23 to B16) are address bits that select which control register is accessed. The remaining 16 bits (B15 to B0) are register bits, corresponding to the 16 bits in each control register.

MODE / GPIO	INTERFACE FORMAT
Low	2 wire
Hi-Z	3 wire
High	3 wire

Table 39 Control Interface Mode Selection

USE OF MODE AS A GPIO PIN IN 3-WIRE MODE

In 3-wire mode, MODE can be used as a GPIO pin. If MODE is being used as a GPIO output, the partner device doesn't have to drive MODE - the pin will be pulled-up internally causing 3-wire mode will be selected. The GPIO function is enabled by setting the MODE_GPIO register bit. The MODE pin can then be controlled using the GPIO register bits as described in Figure 27. To use MODE as a GPIO input, MODE must be undriven or driven high at start-up. Specifically MODE must be high or hi-Z during an initial write to the control interface which sets the MODE_GPIO register bit. After MODE_GPIO has been set, 3-wire mode selection is overridden internally and the MODE pin can be used freely as a GPIO input or output.

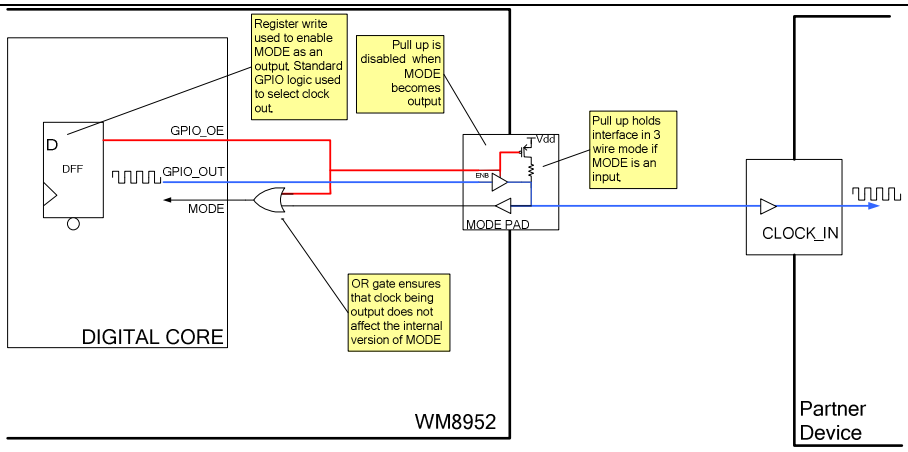


Figure 27 Example Usage of MODE Pin to Generate a Clock Out in 3-wire Mode

This example shows how the MODE_GPIO register bit interfaces to the MODE pad in the case there MODE is used as a GPIO output. When MODE_GPIO is set, the internal version of MODE is overridden to high and the MODE pin output driver is enabled. The pull up, which is used to default 3-wire mode at start-up, is disabled as a power saving measure. MODE_GPIO cannot be set in 2-wire mode - this would prevent correct operation of the control interface. Internal timing is arranged to ensure that the override is in place before the pull-up is disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 GPIO Control	7	MODE_GPIO	0	Selects MODE pin as a GPIO pin 0 = MODE is an input. MODE selects 2-wire mode when low and 3-wire mode when high. 1 = MODE can be an input or output under the control of the GPIO control register. Interface operates in 3-wire mode regardless of what happens on the MODE pin.

Table 40 Mode is GPIO Control

Auto-incremental writes are supported in 2 wire and 3 wire modes. This is enabled by default.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 Control Interface	1	AUTOINC	1	Auto-Incremental write enable 0=Auto-Incremental writes disabled 1=Auto-Incremental writes enabled

Table 41 Control Interface

3-WIRE SERIAL CONTROL MODE

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB/GPIO latches in a complete control word consisting of the last 16 bits.

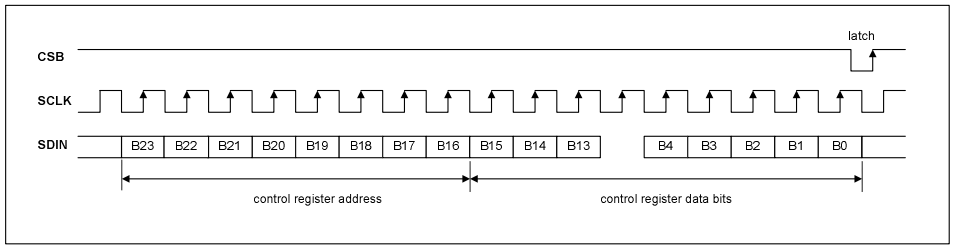


Figure 28 3-Wire Serial Control Interface

READBACK IN 3-WIRE MODE

The following two timing diagrams are also supported.

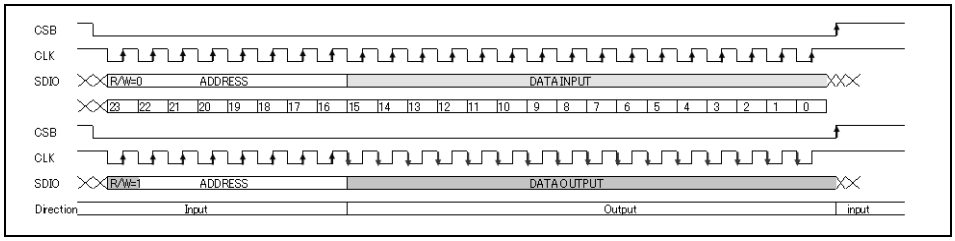


Figure 29 Alternative 3-Wire Serial Control Timing

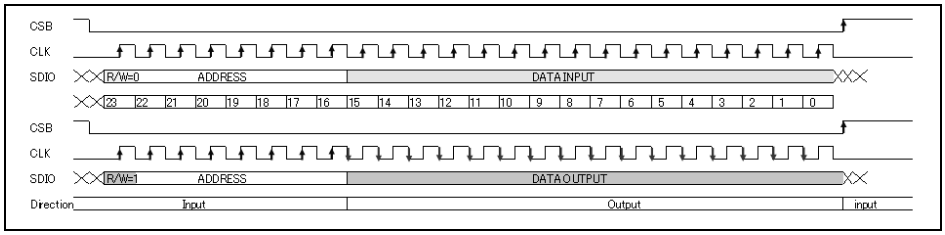


Figure 30 Alternative 3-Wire Serial Control Timing

A limited number of Readback addresses are provided to enable ALC operation to be monitored and to establish the identity and revision of the device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 Software Reset	15:0	CHIP_ID		Readback the CHIP ID
R1 Power Management 1	2:0	DEVICE_REVISON		Readback the DEVICE_REVISON

Table 42 Readback Registers

2-WIRE SERIAL CONTROL MODE

The WM8952 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit device address (this is not the same as the 7-bit address of each register in the WM8952).

The WM8952 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8952, then the WM8952 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1' when operating in write only mode, the WM8952 returns to the idle condition and wait for a new start condition and valid address.

During a write, once the WM8952 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8952 register address plus the first bit of register data). The WM8952 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8952 acknowledges again by pulling SDIN low.

Transfers are complete when there is a low to high transition on SDIN while SCLK is high. After a complete sequence the WM8952 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

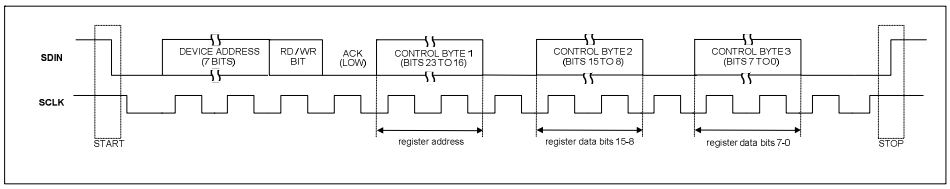


Figure 31 2-Wire Serial Control Interface

In 2-wire mode the WM8952 has a fixed device address, 0011010.

RESETTING THE CHIP

The WM8952 can be reset by performing a write of any value to the software reset register (address 0 hex). This will cause all register values to be reset to their default values. In addition to this there is a Power-On Reset (POR) circuit which ensures that the registers are set to default when the device is powered up.

POWER SUPPLIES

The WM8952 requires the following power supplies:

AVDD and AGND: Analogue supply, powers all analogue functions. AVDD can range from 2.5V to 3.6V and has the most significant impact on overall power consumption. A larger AVDD slightly improves audio quality.

DVDD: Digital core supply, powers all digital functions except the audio and control interfaces. DVDD can range from 1.71V to 3.6V, and has no effect on audio quality. The return path for DVDD is DGND.

It is possible to use the same supply voltage for these. However, digital and analogue supplies should be routed and decoupled separately on the PCB to keep digital switching noise out of the analogue signal paths.

RECOMMENDED POWER UP/DOWN SEQENCE

In order to minimise output pop and click noise, it is recommended that the WM8952 device is powered up and down using one of the following sequences:

Power Up:

1. Turn on external power supplies. Wait for supply voltages to settle.
2. Reset internal registers to default state (software reset).
3. Enable non-VMID derived bias generator (VMID_OP_EN = 1) and level shifters (LVLSHIFT_EN = 1).
4. Select Clock source to MCLK (CLKSEL = 0) and audio mode (Master or Slave).
5. Enable Power on Bias Control (POB_CTRL = 1) and VMID soft start (SOFT_START = 1).
6. Set VMIDSEL[1:0] bits for 50kΩ reference string impedance.
7. Wait for the VMID supply to settle. *Note 2.
8. Enable analogue amplifier bias control (BIASEN = 1) and VMID buffer (BUFIOEN = 1). *Notes 1 and 2.
9. Disable Power on Bias Control (POB_CTRL = 0) and VMID soft start (SOFT_START = 0).

Power Down:

1. Enable non-VMID derived bias generator (VMID_OP_EN = 1).
2. Enable on Bias Control (POB_CTRL = 1).
3. Disable analogue amplifier bias control (BIASEN = 0) and VMID (VMIDSEL[1:0] bits set to OFF).
4. Enable Fast VMID Discharge (TOGGLE = 1) to discharge VMID capacitor.
5. Wait for VMID capacitor to fully discharge.
6. Reset all registers to their default state (software reset).
7. Turn off external power supply voltages.

Notes:

1. This step enables the internal device bias buffer and the VMID buffer for unassigned inputs. This will provide a startup reference for all inputs. This will cause the inputs to ramp towards VMID in a way that is controlled and predictable.
2. Choose the value of VMIDSEL bits based on the startup time (VMIDSEL = 10 for the slowest startup, VMIDSEL = 11 for the fastest startup). Startup time is defined by the value of the VMIDSEL bits (the reference impedance) and the external decoupling capacitor on VMID.

In addition to the power on sequence, it is recommended that the zero cross functions are used when changing the volume in the PGAs to avoid any audible pops and clicks.

POWER MANAGEMENT

VMID

The analogue circuitry will not work when VMID is disabled (VMIDSEL[1:0] = 00b). The impedance of the VMID resistor string, together with the decoupling capacitor on the VMID pin will determine the start-up time of the VMID circuit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	1:0	VMIDSEL	00	Reference string impedance to VMID pin (determines startup time): 00=off (open circuit) 01=50kΩ 10=250kΩ 11=5kΩ (for fastest startup)

Table 43 VMID Impedance Control

BIASEN

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	3	BIASEN	0	Analogue amplifier bias control 0=Disabled 1=Enabled

Table 44 BIASEN Control

ESTIMATED SUPPLY CURRENTS

When either the ADC is enabled it is estimated that approximately 4mA will be drawn from DVDD when fs=48kHz (This will be lower at lower sample rates). When the PLL is enabled an additional 700 microamps will be drawn from DVDD.

Table 45 shows the estimated 3.3V AVDD current drawn by various circuits, by register bit.

REGISTER BIT	AVDD CURRENT (MILLIAMPS)
PLLEN	1.4mA (with clocks applied)
MICBEN	0.5mA
BIASEN	0.3mA
BUFIOEN	0.1mA
VMIDSEL	5K=>0.3mA, less than 0.1mA for 50k/250k
BOOSTEN	0.2mA
INPPGAEN	0.2mA
ADCEN	2.6mA

Table 45 AVDD Supply Current

POP MINIMISATION

Register SOFT_START is the enable bit for the VMID soft-start function. Setting the bit to 1 causes charging of the VMID decoupling cap to follow a soft-start profile which minimises pops. This soft-start profile has minimal impact on VMID charge time.

Fast VMID discharge is enabled using TOGGLE. Setting to 1 opens a low impedance discharge path from VMID to GND. This function can be used during power down to reduce the discharge time of the VMID decoupling cap. Must be set to 0 for normal operation.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Additional Control	5	SOFT_START	0	VMID Soft Start 0=disabled 1=enabled
	4	TOGGLE	0	Fast VMID Discharge 0=normal 1=enable (used during power-down)

Table 46 POP Minimisation Control

THERMAL SHUTDOWN

To protect the WM8952 from overheating a thermal shutdown circuit is included. The thermal shutdown can be configured to produce an interrupt when the device reaches approximately 125°C. See General Purpose Input/Output section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49 Output control	1	TSDEN	1	Thermal Shutdown Enable 0 : thermal shutdown disabled 1 : thermal shutdown enabled

Table 47 Thermal Shutdown

REGISTER MAP

ADDR		Register Name	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Default Value (Bin)
Dec	Hex																		
0	00	Software Reset	SOTWARE RESET ON WRITE / CHIP ID ON READ																1000_1001_0100_0000
1	01	Power management 1	0	0	0	0	0	0	0	0	LVLSHIFT_EN	AUXEN	PLLEN	MICBEN	BIASEN	0 DEVICE_REVISION[2:0]	VMIDSEL[1:0]		0000_0000_0000_0000
2	02	Power management 2	0	0	0	0	0	0	0	0	0	0	0	BOOSTEN	0	INPPGAEN	0	ADCEN	0000_0000_0000_0000
3	03	Power management 3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
4	04	Audio Interface	0	0	0	0	0	0	0	BCP	FRAMEP	WL[1:0]		FMT[1:0]		0	ALRSWAP	0	0000_0000_0101_0000
5	05	Companding control	0	0	0	0	0	0	0	0	0	0	WL8	0	0	ADC_COMP[1:0]		0	0000_0000_0000_0000
6	06	Clock Gen control	0	0	0	0	0	0	0	CLKSEL	MCLKDIV[2:0]			BCLKDIV[2:0]			0	MS	0000_0001_0100_0000
7	07	Additional control	0	0	0	0	0	0	0	0	0	0	SOFT_START	TOGGLE	SR[2:0]			SLOWCLKEN	0000_0000_0000_0000
8	08	GPIO Stuff	0	0	0	0	0	0	0	0	MODE_GPIO	0	OPCLKDIV[1:0]		GPIOPOL	GPIOSEL[2:0]			0000_0000_0000_0000
9	09	Control Interface	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AUTOINC	0	0000_0000_0000_0010
10	0A	Reserved																	
11	0B	Reserved	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0000_0000_1111_1111
12	0C	Reserved																	
13	0D	Reserved																	
14	0E	ADC Control	0	0	0	0	0	0	0	HPFEN	HPFAPP	HPFCUT[2:0]			0	0	0	ADCPOL	0000_0001_0000_0000
15	0F	ADC Digital Vol	0	0	0	0	0	0	0	0	ADCVOL[7:0]								0000_0000_1111_1111
16	10	Notch Filter 1	NF0_UP	NF0_EN	NF0_A0[13:0]														0000_0000_0000_0000
17	11	Notch Filter 2	NF0_UP	0	NF0_A1[13:0]														0000_0000_0000_0000
18	12	Notch Filter 3	NF1_UP	NF1_EN	NF1_A0[13:0]														0000_0000_0000_0000
19	13	Notch Filter 4	NF1_UP	0	NF1_A1[13:0]														0000_0000_0000_0000
20	14	Notch Filter 5	NF2_UP	NF2_EN	NF2_A0[13:0]														0000_0000_0000_0000
21	15	Notch Filter 6	NF2_UP	0	NF2_A1[13:0]														0000_0000_0000_0000
22	16	Notch Filter 7	NF3_UP	NF3_EN	NF3_A0[13:0]														0000_0000_0000_0000
23	17	Notch Filter 8	NF3_UP	NF3_LP	NF3_A1[13:0]														0000_0000_0000_0000
24	18	Reserved																	
25	19	Reserved																	
26	1A	Reserved																	
27	1B	Reserved																	
28	1C	Reserved																	
29	1D	Reserved																	
30	1E	Reserved																	
31	1F	Reserved																	
32	20	ALC control 1	ALCGAIN[5:0]						0	ALCSEL	0	0	ALCMAX[2:0]			ALCMIN[2:0]			0000_0000_0011_1000
33	21	ALC control 2	0	0	0	0	0	0	0	0	ALCHLD[3:0]				ALCLVL[3:0]				0000_0000_0000_1011
34	22	ALC control 3	0	0	0	0	0	0	0	ALCMODE	ALCDCY[3:0]				ALCATK[3:0]				0000_0000_0011_0010
35	23	Noise Gate	0	0	0	0	0	0	0	0	0	0	0	0	NGEN	NGTH[2:0]			0000_0000_0000_0000
36	24	PLL N	0	0	0	0	0	0	0	0	PLL_POWERDOWN	FRACEN	PLL_PRESCALE[1:0]		PLLN[3:0]				0000_0000_0100_1000
37	25	PLL K 1	0	0	0	0	0	0	0	0	0	0	PLLK[23:18]						0000_0000_0000_1100
38	26	PLL K 2	0	0	0	0	0	0	0	PLLK[17:9]									0000_0000_1001_0011
39	27	PLL K 3	0	0	0	0	0	0	0	PLLK[8:0]									0000_0000_1110_1001
40	28	Reserved																	
41	29	Reserved																	
42	2A	Spare Register	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ALCZC	0	0000_0000_0011_0000
43	2B	Reserved																	
44	2C	Input ctrl	0	0	0	0	0	0	0	MICBVSEL	0	0	0	0	AUXMODE	AUX2INPPGA	MICN2INPPGA	MICP2INPPGA	0000_0000_0000_0010
45	2D	INP PGA gain ctrl	0	0	0	0	0	0	0	0	INPPGAZC	INPPGAMUTE	INPPGAVOL[5:0]						0000_0000_0101_0000
46	2E	Reserved																	
47	2F	ADC BOOST ctrl	0	0	0	0	0	0	0	PGABOOST	0	MICP2BOOSTVOL[2:0]			0	AUX2BOOSTVOL[2:0]			0000_0000_0000_0000
48	30	Reserved																	
49	31	Thermal Shuldown	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TSDEN	0	0000_0000_0000_0010
50	32	Reserved																	
51	33	Reserved																	
52	34	Reserved																	
53	35	Reserved																	
54	36	Reserved																	
55	37	Reserved																	
56	38	Reserved																	

Note: Bits marked in green are readable. Other bits are write-only.

REGISTER BITS BY ADDRESS

Notes:

1. Default values of N/A indicate non-latched data bits (e.g. software reset or volume update bits).

2. Register bits marked as "Reserved" should not be changed from the default.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
0 (00h)	[15:0]	RESET / CHIP_ID	N/A	Writing to this register will apply a software reset. Reading from this register will return the device id	Resetting the Chip / Control Interface
1 (01h)	15:8		000h	Reserved	
	7	LVLSHIFT_EN	0	Enable bit for the level shifters. 1 for normal operation, 0 for standby.	Power Management
	6	AUXEN	0	Auxilliary input buffer enable 0 = OFF 1 = ON	Auxiliary Inputs
	5	PLLEN	0	PLL enable 0=PLL off 1=PLL on	Master Clock and Phase Locked Loop (PLL)
	4	MICBEN	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON	Microphone Biasing Circuit
	3	BIASEN	0	Analogue amplifier bias control 0=Disabled 1=Enabled	Power Management
	2:0	DEVICE_REVISION	000	Readback from this register will return the device revision in this position	Control Interface
	2	BUFIOEN	0	Enable bit for the VMID buffer. The VMID buffer is used to maintain a buffered VMID voltage on all analogue input pins. 1. for normal operation 0. for standby (where inputs settle to GND).	Enabling the Outputs
	1:0	VMIDSEL	00	Reference string impedance to VMID pin: 00=off (open circuit) 01=50kΩ 10=250kΩ 11=5kΩ	Power Management
2 (02h)	15:5		000h	Reserved	
	4	BOOSTEN	0	Input BOOST enable 0 = Boost stage OFF 1 = Boost stage ON	Input Boost
	3		0	Reserved	
	2	INPPGAEN	0	Input microphone PGA enable 0 = disabled 1 = enabled	Input Signal Path
	1		0	Reserved	
	0	ADCEN	0	ADC Enable Control 0 = ADC disabled 1 = ADC enabled	Analogue to Digital Converter (ADC)
3 (03h)	15:0		00h	Reserved	
4 (04h)	15:9		0000000	Reserved	
	8	BCP	0	BCLK polarity 0=normal 1=inverted	Digital Audio Interfaces

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7	FRAMEP	0	Frame clock polarity 0=normal 1=inverted	Digital Audio Interfaces
				DSP Mode control 1 = Configures the interface so that MSB is available on 1st BCLK rising edge after FRAME rising edge 0 = Configures the interface so that MSB is available on 2nd BCLK rising edge after FRAME rising edge	
	6:5	WL	10	Word length 00=16 bits 01=20 bits 10=24 bits 11=32 bits	Digital Audio Interfaces
	4:3	FMT	10	Audio interface Data Format Select: 00=Right Justified 01=Left Justified 10=I2S format 11= DSP/PCM mode	Digital Audio Interfaces
	2		0	Reserved	
	1	ALRSWAP	0	Controls whether ADC data appears in 'right' or 'left' phases of FRAME clock: 0=ADC data appear in 'left' phase of FRAME 1=ADC data appears in 'right' phase of FRAME	Digital Audio Interfaces
	0		0	Reserved	
5 (05h)	15:6		000h	Reserved	
	5	WL8	0	8 Bit Word Length for companding 0=Word Length controlled by WL 1=8 bits	Digital Audio Interfaces
	4:3			Reserved	
	2:1	ADC_COMP	00	ADC companding 00=off 01=reserved 10=μ-law 11=A-law	Digital Audio Interfaces
	0			Reserved	
6 (06h)	15:9		00h	Reserved	
	8	CLKSEL	1	Controls the source of the clock for all internal operation: 0=MCLK 1=PLL output	Digital Audio Interfaces
	7:5	MCLKDIV	010	Sets the scaling for either the MCLK or PLL clock output (under control of CLKSEL) 000=divide by 1 001=divide by 1.5 010=divide by 2 011=divide by 3 100=divide by 4 101=divide by 6 110=divide by 8 111=divide by 12	Digital Audio Interfaces

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:2	BCLKDIV	000	Configures the BCLK and FRAME output frequency, for use when the chip is master over BCLK. 000=divide by 1 (BCLK=MCLK) 001=divide by 2 (BCLK=MCLK/2) 010=divide by 4 011=divide by 8 100=divide by 16 101=divide by 32 110=reserved 111=reserved	Digital Audio Interfaces
	1		0	Reserved	
	0	MS	0	Sets the chip to be master over FRAME and BCLK 0=BCLK and FRAME clock are inputs 1=BCLK and FRAME clock are outputs generated by the WM8952 (MASTER)	Digital Audio Interfaces
7 (07h)	15:6		00000	Reserved	
	6			Reserved	
	5	SOFT_START	0	VMID Soft Start 0=disabled 1=enabled	POP Minimisation
	4	TOGGLE	0	Fast VMID Discharge 0=normal 1=enable (used during power-down)	POP Minimisation
	3:1	SR	000	Approximate sample rate (configures the coefficients for the internal digital filters): 000=48kHz 001=32kHz 010=24kHz 011=16kHz 100=12kHz 101=8kHz 110-111=reserved	Audio Sample Rates
	0	SLOWCLKEN	0	Enables the Timeout Clock for zero cross detection.	Zero Cross Timeout
8 (08h)	15:8		00h	Reserved	
	7	MODE_GPIO	0	Selects MODE as a GPIO pin 0 = MODE is an input. MODE selects 2-wire mode when low and 3-wire mode when high. 1 = MODE can be an input or output under the control of the GPIO control register. Interface operates in 3-wire mode regardless of when happens on the MODE pin.	Control Interface
	6		0	Reserved	
	5:4	OPCLKDIV	00	PLL Output clock division ratio 00=divide by 1 01=divide by 2 10=divide by 3 11=divide by 4	General Purpose Input Output
	3	GPIOPOL	0	GPIO Polarity invert 0=Non inverted 1=Inverted	General Purpose Input Output

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	GPIOSEL	000	GPIO function select: 000=GPIO off 010=Temp ok 100=SYSCLK clock o/p 101=PLL lock All other values: Reserved	General Purpose Input Output
9 (09h)	15:2			Reserved	
	1	AUTOINC	1	Auto-Incremental write enable 0=Auto-Incremental writes disabled 1=Auto-Incremental writes enabled	Control Interface
	0		0	Reserved	
10 (0Ah)	15:0		0000h	Reserved	
11 (0Bh)	15:0		00FFh	Reserved	
12 (0Ch)	15:0			Reserved	
13 (0Dh)	15:0			Reserved	
14 (0Eh)	15:9		00h	Reserved	
	8	HPFEN	1	High Pass Filter Enable 0=disabled 1=enabled	Analogue to Digital Converter (ADC)
	7	HPFAPP	0	Select audio mode or application mode 0=Audio mode (1st order, fc = ~3.7Hz) 1=Application mode (2nd order, fc = HPFCUT)	Analogue to Digital Converter (ADC)
	6:4	HPFCUT	000	Application mode cut-off frequency See Table 14 for details.	Analogue to Digital Converter (ADC)
	3:1		00	Reserved	
	0	ADCPOL	0	ADC Polarity 0=normal 1=inverted	Analogue to Digital Converter (ADC)
15 (0Fh)	15:8		00h	Reserved	
	7:0	ADCVOL	11111111	ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB	Analogue to Digital Converter (ADC)
16 (10h)	15	NF0_UP	0	Notch filter 0 update. The notch filter 0 values used internally only update when one of the NF0_UP bits is set high.	Analogue to Digital Converter (ADC)
	14	NF0_EN	0	Notch filter 0 enable: 0=Disabled 1=Enabled	Analogue to Digital Converter (ADC)
	13:0	NF0_A0	0000h	Notch Filter 0 a0 coefficient	Analogue to Digital Converter (ADC)
17 (11h)	15	NF0_UP	0	Notch filter 0 update. The notch filter 0 values used internally only update when one of the NF0_UP bits is set high.	Analogue to Digital Converter (ADC)
	14		0	Reserved	
	13:0	NF0_A1	0000h	Notch Filter 0 a1 coefficient	Analogue to Digital Converter (ADC)
18 (12h)	15	NF1_UP	0	Notch filter 1 update. The notch filter 1 values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	14	NF1_EN	0	Notch Filter 1 enable. 0=Disabled 1=Enabled	Analogue to Digital Converter (ADC)
	13:0	NF1_A0	0000h	Notch Filter 1 a0 coefficient	Analogue to Digital Converter (ADC)
19 (13h)	15	NF1_UP	0	Notch filter 1 update. The notch filter 1 values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	14		0	Reserved	
	13:0	NF1_A1	0000h	Notch Filter 1 a1 coefficient	Analogue to Digital Converter (ADC)
20 (14h)	15	NF2_UP	0	Notch filter 2 update. The notch filter 2 values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	14	NF2_EN	0	Notch Filter 2 enable. 0=Disabled 1=Enabled	Analogue to Digital Converter (ADC)
	13:0	NF2_A0	0000h	Notch Filter 2 a0 coefficient	Analogue to Digital Converter (ADC)
21 (15h)	15	NF2_UP	0	Notch filter 2 update. The notch filter 2 values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	14		0	Reserved	
	13:0	NF2_A1	0000h	Notch Filter 2 a1 coefficient	Analogue to Digital Converter (ADC)
22 (16h)	15	NF3_UP	0	Notch filter 3 update. The notch filter 3 values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	14	NF3_EN	0	Notch Filter 3 enable 0=Disabled 1=Enabled	Analogue to Digital Converter (ADC)
	13:0	NF3_A0	0000h	Notch Filter 3 a0 coefficient	Analogue to Digital Converter (ADC)
23 (17h)	15	NF3_UP	0	Notch filter 3 update. The notch filter 3 values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	14	NF3_LP	0	Notch Filter 3 mode select 0 = Notch Filter mode 1 = Low Pass Filter mode	Analogue to Digital Converter (ADC)
	13:0	NF3_A1	0000h	Notch Filter 3 a1 coefficient	Analogue to Digital Converter (ADC)
24 (18h)	15:0		0032h	Reserved	
25 (19h)	15:0		0000h	Reserved	
26 (1Ah)	15:0		0000h	Reserved	
27 (1Bh)	15:0		0000h	Reserved	
28 (1Ch)	15:0		0000h	Reserved	
29 (1Dh)	15:0		0000h	Reserved	
30 (1Eh)	15:0		0000h	Reserved	
31(1Fh)	15:0		0000h	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
32 (20h)	15:10	ALCGAIN[5:0]	000000	Readback from this register will return the ALC gain in this position	Input Limiter / Automatic Level Control (ALC)
	9		0	Reserved	
	8	ALCSEL	0	ALC function select 0=ALC disabled 1=ALC enabled	Input Limiter / Automatic Level Control (ALC)
	7:6		00	Reserved	
	5:3	ALCMAX	111	Set Maximum Gain of PGA	Input Limiter / Automatic Level Control (ALC)
	2:0	ALCMIN	000	Set minimum gain of PGA	Input Limiter / Automatic Level Control (ALC)
33 (21h)	15:8		000h	Reserved	
	7:4	ALCHLD	000	ALC hold time before gain is increased.	Input Limiter / Automatic Level Control (ALC)
	3:0	ALCLVL	1011	ALC threshold level. Sets the desired signal level.	Input Limiter / Automatic Level Control (ALC)
34 (22h)	15:9		00h	Reserved	
	8	ALCMODE	0	Determines the ALC mode of operation: 0=Normal mode 1=Limiter mode.	Input Limiter / Automatic Level Control (ALC)
	7:4	ALCDCY	0011	Decay (gain ramp-up) time	Input Limiter / Automatic Level Control (ALC)
	3:0	ALCATK	0010	ALC attack (gain ramp-down) time	Input Limiter / Automatic Level Control (ALC)
35 (23h)	15:4		000h	Reserved	
	3	NGEN	0	Noise gate function enable 1 = enable 0 = disable	Input Limiter / Automatic Level Control (ALC)
	2:0	NGTH	000	Noise gate threshold	Input Limiter / Automatic Level Control (ALC)
36 (24h)	15:8		00h	Reserved	
	7	PLL_POWERDOWN	0	PLL POWER 0=On 1=Off	Master Clock and Phase Locked Loop (PLL)
	6	FRACEN	1	Fractional Divide within the PLL 0=Disabled (Lower Power) 1=Enabled	Master Clock and Phase Locked Loop (PLL)
	5:4	PLLPRESCALE	00	00 = MCLK input multiplied by 2 (default) 01 = MCLK input not divided 10 = Divide MCLK by 2 before input to PLL 11 = Divide MCLK by 4 before input to PLL	Master Clock and Phase Locked Loop (PLL)
	3:0	PLLN[3:0]	1100	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.	Master Clock and Phase Locked Loop (PLL)
37 (25h)	15:6		000h	Reserved	
	5:0	PLLK[23:18]	001100	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Master Clock and Phase Locked Loop (PLL)
38 (26h)	15:9		00h	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	8:0	PLLK[17:9]	010010011	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Master Clock and Phase Locked Loop (PLL)
39 (27h)	15:9		00h	Reserved	
	8:0	PLLK[8:0]	011101001	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Master Clock and Phase Locked Loop (PLL)
40 (28h)	15:0		0000h	Reserved	
41 (29h)	15:0		0000h	Reserved	
42 (2Ah)	15:2		0	Reserved	ALC Control 4
	1	ALCZC	0 (zero cross off)	ALC uses zero cross detection circuit. 0 = Disabled (recommended) 1 = Enabled	
	0		0	Reserved	
43 (2Bh)	15:0		0000h	Reserved	
44 (2Ch)	15:9		00h	Reserved	
	8	MBVSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.75 * AVDD	Input Signal Path
	7:4		0h	Reserved	
	3	AUXMODE	0	Auxiliary Input Mode 0 = inverting buffer 1 = mixer (on-chip input resistor bypassed)	Input Signal Path
	2	AUX2INPPGA	0	Select AUX amplifier output as input PGA signal source. 0=AUX not connected to input PGA 1=AUX connected to input PGA amplifier negative terminal.	Input Signal Path
	1	MICN2INPPGA	1	Connect MICN to input PGA negative terminal. 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.	Input Signal Path
	0	MICP2INPPGA	0	Connect input PGA amplifier positive terminal to MICP or VMID. 0 = input PGA amplifier positive terminal connected to VMID 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string	Input Signal Path
45 (2Dh)	15:8		00h	Reserved	
	7	INPPGAZC	0	Input PGA zero cross enable: 0=Update gain when gain register changes 1=Update gain on 1st zero cross after gain register write.	Input Signal Path
	6	INPPGAMUTE	1	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).	Input Signal Path
	5:0	INPPGAVOL	010000	Input PGA volume 000000 = -12dB 000001 = -11.25db . 010000 = 0dB . 111111 = 35.25dB	Input Signal Path
46 (2Eh)	15:0		0000h	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
47 (2Fh)	15:9		00h	Reserved	
	8	PGABOOST	0	Input Boost 0 = PGA output has +0dB gain through input BOOST stage. 1 = PGA output has +20dB gain through input BOOST stage.	Input Signal Path
	7		0	Reserved	
	6:4	MICP2BOOSTVOL	000	Controls the MICP pin to the input boost stage (NB, when using this path set MICP2INPPGA=0): 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage … 111=+6dB gain through boost stage	Input Signal Path
	3		0	Reserved	
	2:0	AUX2BOOSTVOL	000	Controls the auxiliary amplifier to the input boost stage: 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage … 111=+6dB gain through boost stage	Input Signal Path
48 (30h)	15:0		0000h	Reserved	
49 (31h)	15:2		000h	Reserved	
	1	TSDEN	1	Thermal Shutdown Enable 0 : thermal shutdown disabled 1 : thermal shutdown enabled	Output Switch
	0	VROI	0	VREF (AVDD/2 or 1.5xAVDD/2) to analogue output resistance 0: approx 1kΩ 1: approx 30 kΩ	Analogue Outputs
50 (32h)	15:0		0000h	Reserved	
51 (33h)	15:0		0000h	Reserved	
52 (34h)	15:0		0000h	Reserved	
53 (35h)	15:0		0000h	Reserved	
54 (36h)	15:9		0079h	Reserved	
55 (37h)	15:0		0000h	Reserved	
56 (38h)	15:8		0000h	Reserved	

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.025dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.025	dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs	-60			dB
Group Delay			21/fs		
ADC High Pass Filter					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		

Table 48 Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region
3. Note that this delay applies only to the filters and does not include additional delays through other digital circuits. See Table 49 for the total delay.

PARAMETER	MIN	TYP	MAX	UNIT
Total Delay (ADC analogue input to digital audio interface output)	28/fs	30/fs	32/fs	fs

Table 49 Total Group Delay

Notes

1. Wind noise filter is disabled.

ADC FILTER RESPONSES

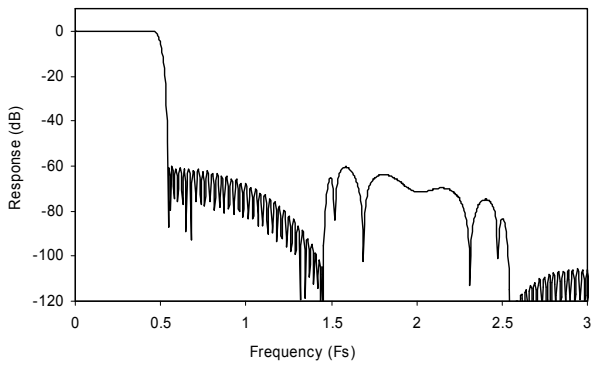


Figure 32 ADC Digital Filter Frequency Response

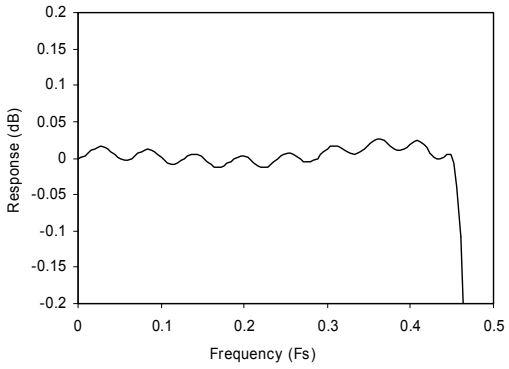


Figure 33 ADC Digital Filter Ripple

HIGHPASS FILTER

The WM8952 has a selectable digital high pass filter in the ADC filter path. This filter has two modes, audio and applications. In audio mode the filter is a 1st order IIR with a cut-off of around 3.7Hz. In applications mode the filter is a 2nd order high pass filter with a selectable cut-off frequency.

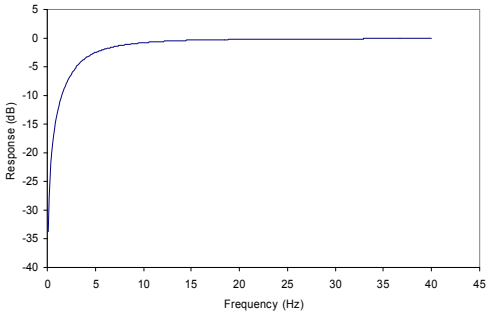


Figure 34 ADC High Pass Filter Response, HPFAPP=0

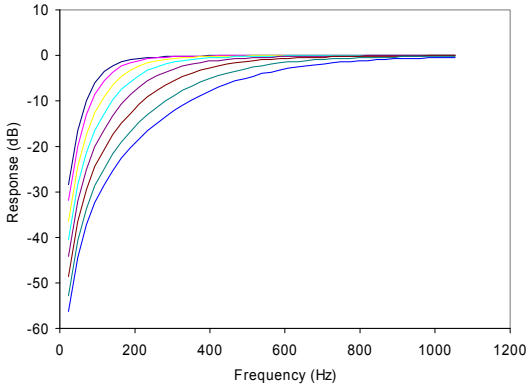


Figure 35 ADC High Pass Filter Responses (48kHz), HPFAPP=1, all cut-off settings shown.

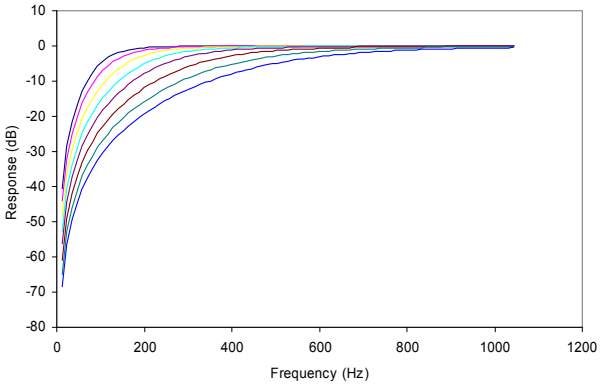


Figure 36 ADC High Pass Filter Responses (24kHz), HPFAPP=1, all cut-off settings shown.

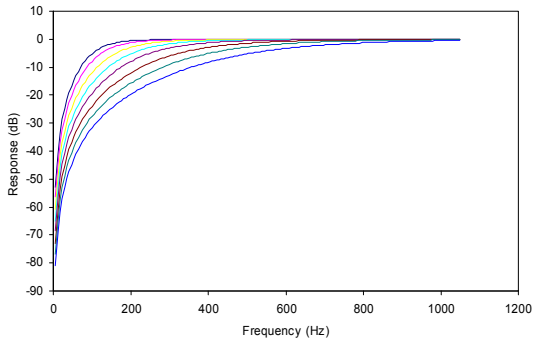


Figure 37 ADC High Pass Filter Responses (12kHz), HPFAPP=1, all cut-off settings shown.

NOTCH FILTERS AND LOW PASS FILTER

The WM8952 supports four programmable notch filters. The fourth notch filter can be configured as a low pass filter. The following illustrates three digital notch filters, followed by a single low pass filter in the ADC filter path. Both the centre frequency and -3dB bandwidth are programmable for the notch filters. The cut off frequency is programmable for the low pass filter. The following graphs show the responses of 1) a single notch filter at three chosen centre frequencies, with three bandwidths for each, 2) the low pass filter at three chosen cut off frequencies and 3) the cascade of three notch filters followed by the low pass filter, each with a different centre / cut off frequency with three bandwidths for each.

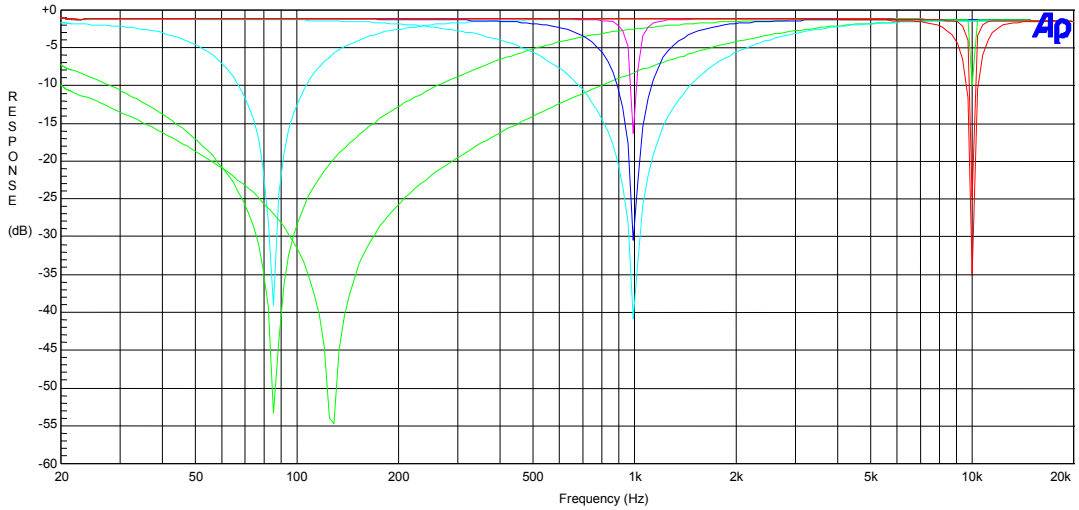


Figure 38 ADC Notch Filter Responses (48kHz); fc=100Hz, 1kHz, 10kHz; fb = 100Hz, 600Hz, 2kHz

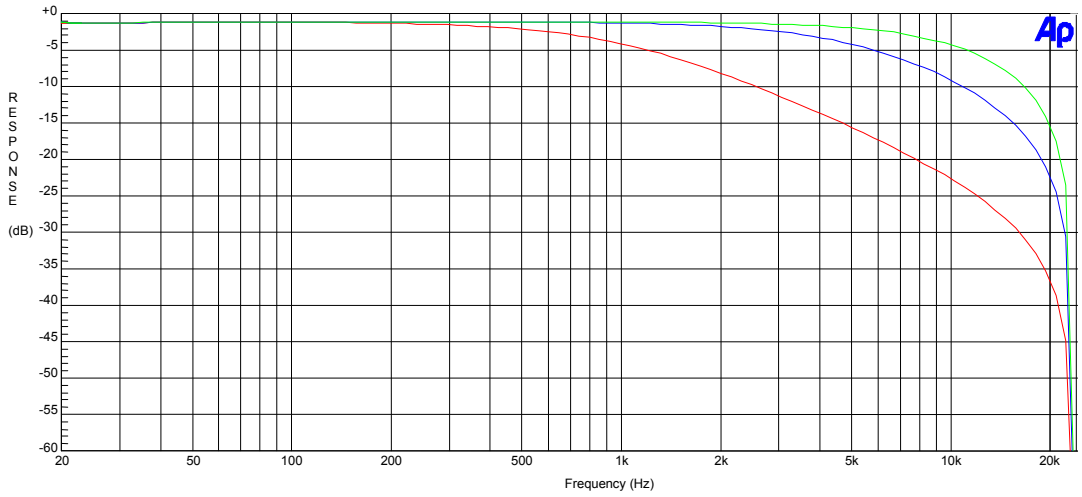


Figure 39 ADC Low Pass Filter Responses (48kHz); fc= 1kHz, 5kHz, 10kHz

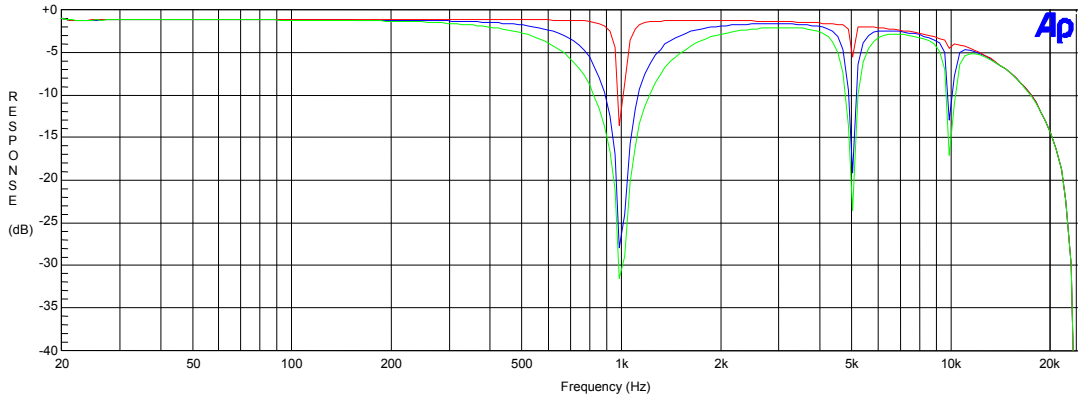


Figure 40 Cumulative Notch + Low Pass Filters Responses (48kHz); NF0 fc = 1kHz; NF1 fc = 5kHz; NF2 fc = 10kHz; LPF fc = 11kHz; fb = 100Hz, 600Hz, 2kHz

Notch Filter Worked Example

The following example illustrates how to calculate the a0 and a1 coefficients for a desired centre frequency and -3dB bandwidth.

f_c = 1000 Hz

f_b = 100 Hz

f_s = 48000 Hz

$w_0 = 2\pi f_c / f_s$ = 2π *x (1000 / 48000) = 0.1308996939 rads*

$w_b = 2\pi f_b / f_s$ = 2π *x (100 / 48000) = 0.01308996939 rads*

$$a_0 = \frac{1-\tan(w_b/2)}{1+\tan(w_b/2)} = \frac{1-\tan(0.01308996939/2)}{1+\tan(0.01308996939/2)} = 0.9869949627$$

$$a_1 = -(1+a_0)\cos(w_0) = -(1+0.9869949627)\cos(0.1308996939) = -1.969995945$$

NFn_A0 = -a0 x 2^{13} = -8085 (rounded to nearest whole number)

NFn_A1 = -a1 x 2^{12} = 8069 (rounded to nearest whole number)

These values are then converted to a 14-bit sign / magnitude notation:

NFn_A0[13] = 1; NFn_A0[12:0] = 13'h1F95; NFn_A0 = 14'h3F95 = 14'b11111110010101

NFn_A1[13] = 0; NFn_A1[12:0] = 13'h1F85; NFn_A1 = 14'h1F85 = 14'b01111110000101

RECOMMENDED EXTERNAL COMPONENTS

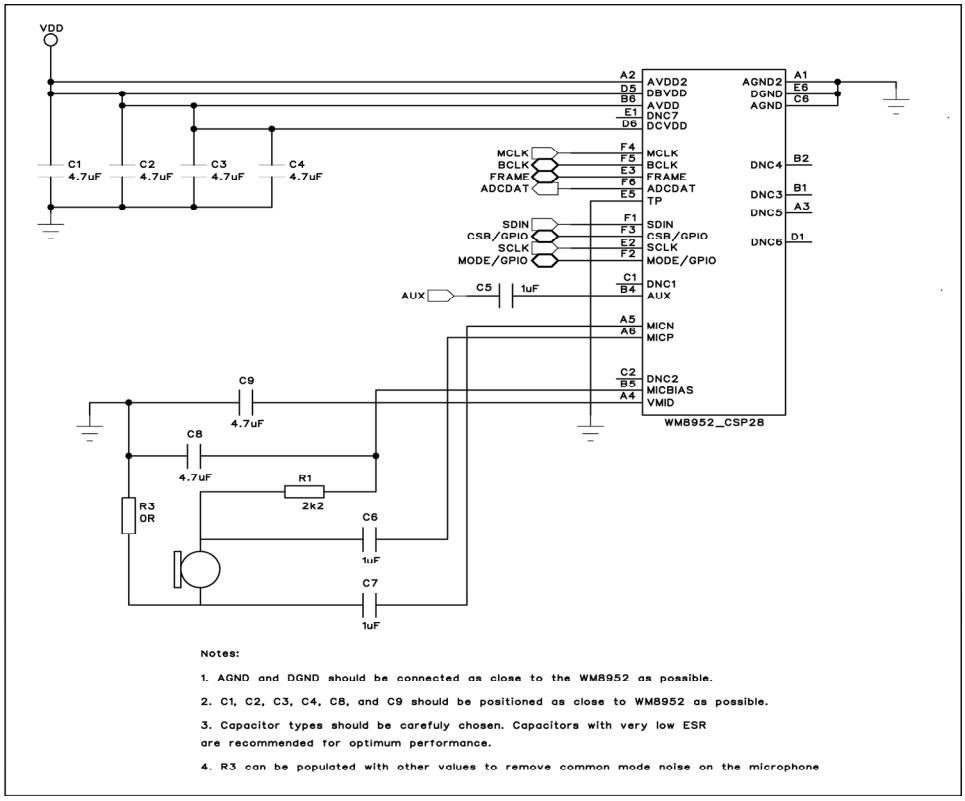
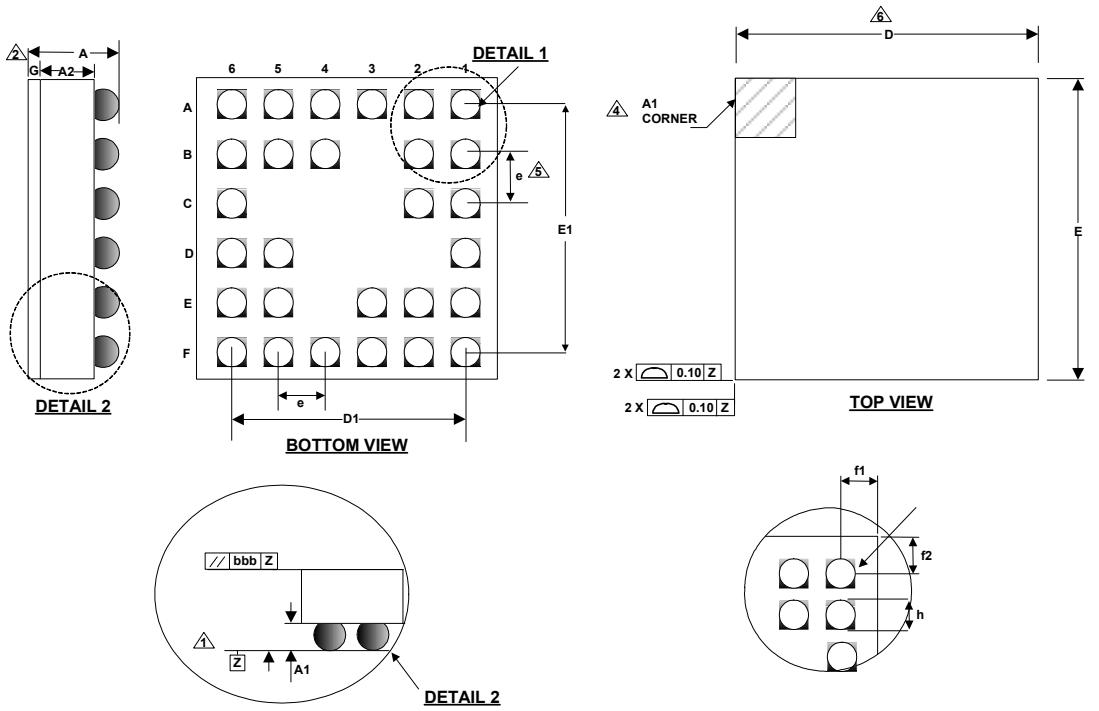


Figure 41 Recommended External Components

PACKAGE DIAGRAM

B: 28 BALL W-CSP PACKAGE 2.590 x 2.500 x 0.7mm BODY, 0.40 mm BALL PITCH **DM054.A**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.615	0.7	0.785	
A1	0.195	0.220	0.245	
A2	0.385	0.410	0.435	
D		2.590 BSC		
D1		2.000 BSC		
E		2.500 BSC		
E1		2.000 BSC		
e		0.400 BSC		5
f1	0.275			
f2	0.230			
g	0.035	0.070	0.105	
h		0.260 BSC		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
01/12/08	3.0	BDC	Changed to Pre Production status
25/04/11	3.1	JMacD	Removed QFN package option and references in datasheet.
		TS	Changed reel QTY to 3,500 devices