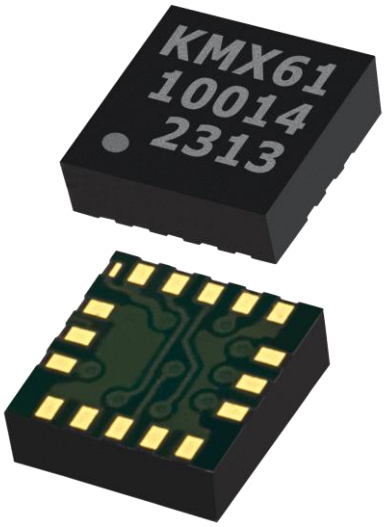
Kionix®	**Digital Tri-axis Magnetometer/ Tri-axis Accelerometer Specifications**	**PART NUMBER:** **KMX61-1021** **Rev. 1.0** **July 14**

Product Description



KMX61 is a 6 Degrees-of-Freedom inertial sensor system that features 14-bit digital outputs accessed through I^2C communication. The KMX61 sensor consists of a tri-axial magnetometer plus a tri-axial accelerometer coupled with an ASIC. It is packaged in a 3x3x0.9mm Land Grid Array (LGA) package. The ASIC is realized in standard 0.18um CMOS technology and features flexible user programmable ±2g/±4g/±8g full scale range for the accelerometer. Accelerometer and Magnetometer data can be accumulated in an internal 512 byte FIFO buffer and transmitted to the application processor.

Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. Capacitance changes are amplified and converted into digital signals which are processed by a dedicated digital signal processing unit. The digital signal processor applies filtering, bias and sensitivity adjustment, as well as temperature compensation.

Magnetic sensing is based on the principle of magnetic impedance. The magnetic sensor detects very small magnetic fields by passing an electric pulse through a special electron spin aligned amorphous wire. Due to the high Curie temperature of the wire, the sensor's thermal performance shows excellent stability.

Noise performance is excellent with bias stability over temperature. Bias errors resulting from assembly can be trimmed digitally by the user. These sensors can accept supply voltages between 1.8V and 3.3V, and digital communication voltages between 1.8 and 3.3V.

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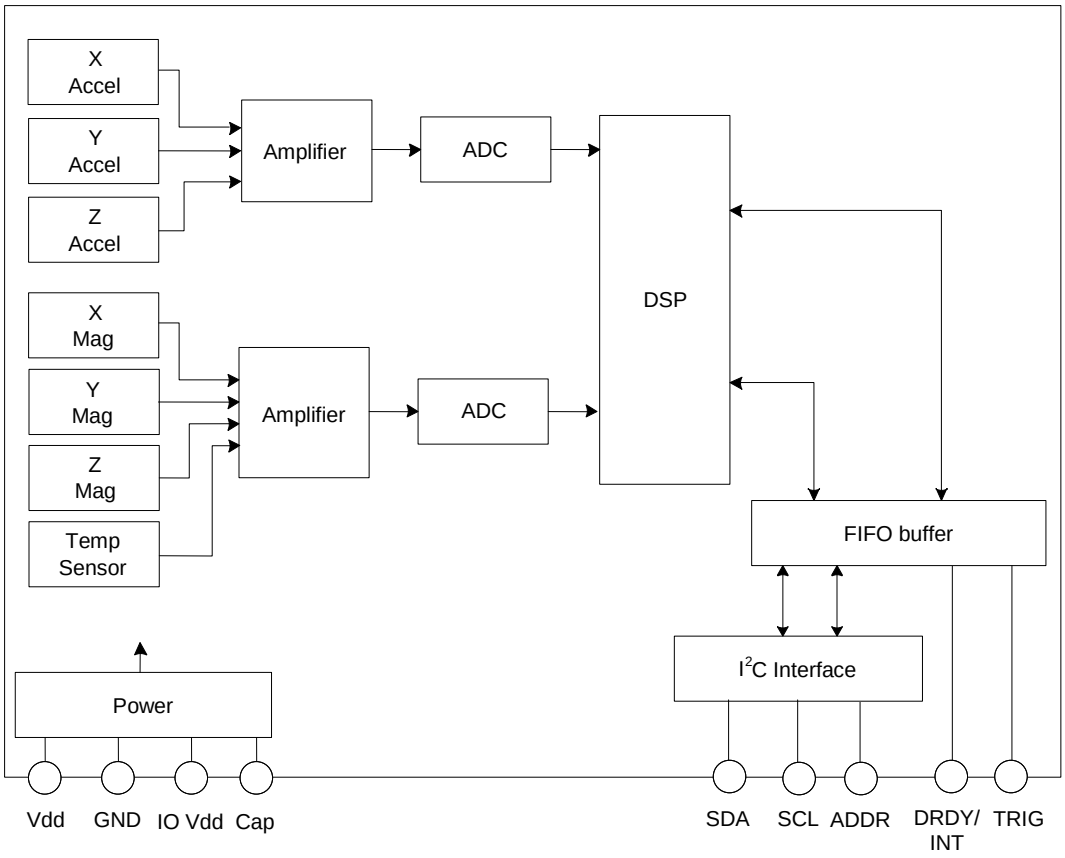
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Functional Diagram



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Product Specifications

Note: Specifications are for operation at Vdd = 2.5V and T = 25ºC unless stated otherwise

Table 1. Magnetometer

Parameters	Units	Value
Operating Temperature Range	ºC	-40 to 85
Full Scale Range	± µT	1200
Digital Bit Depth	bits	14
Offset at Zero Magnetic Field	± µT	0
Offset Temperature Coefficient	± µT/ºC	0.3
Magnetic Sensitivity	± µT/LSB	0.146
Sensitivity Temperature Coefficient.	± %/ºC	0.05
Integral Non-Linearity	% of FS	0.5
Noise[1] (at 50Hz ODR)	µT (RMS)	0.4
Cross Axis Sensitivity	% of FS	-1.1 (S_{xy}) 3.6 (S_{xz}) 2.1 (S_{yx}) 0.3 (S_{yz}) 0.8 (S_{zx}) -1.7 (S_{zy})
Maximum Exposed Field[2]	µT	1,000,000

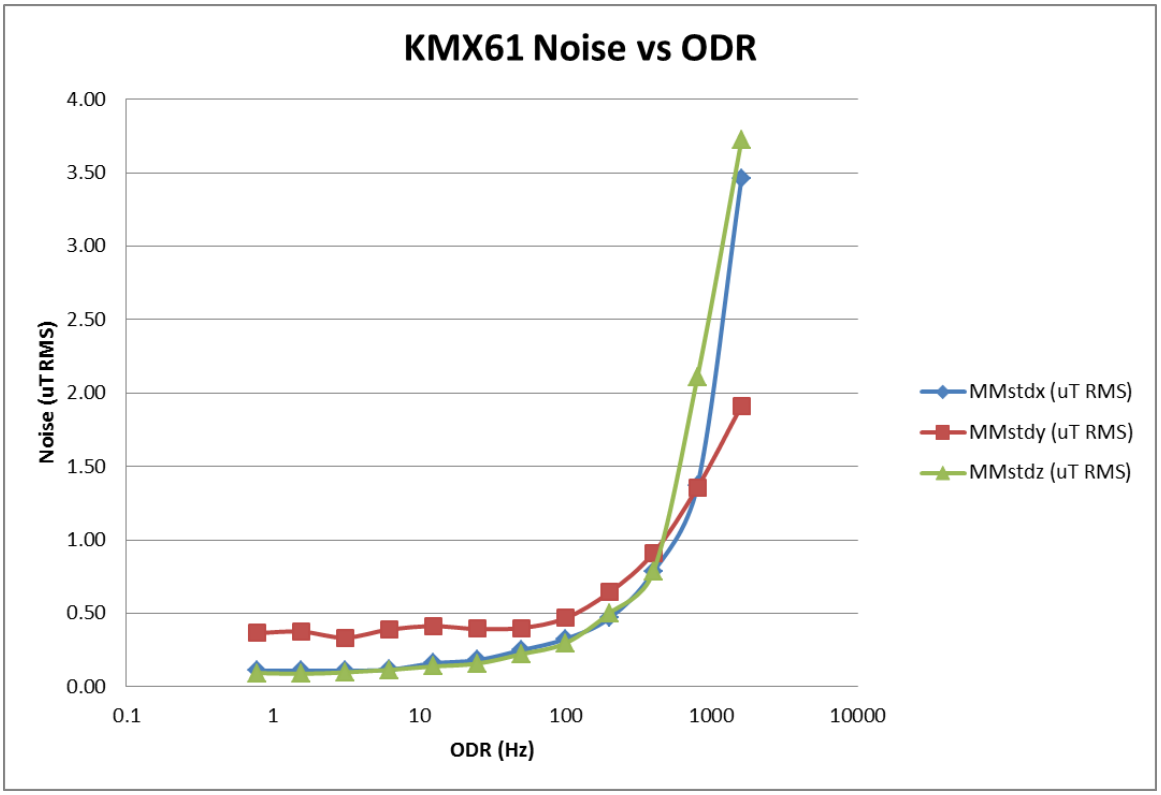
Notes:

1. See plot below for noise performance over ODR for all three axes.
2. No permanent effect on Zero Magnetic Field Offset.

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Table 2. Accelerometer

Parameters		Units	Value
Operating Temperature Range		ºC	-40 to 85
Full Scale Range	GSEL1=0, GSEL=0	g	± 2
	GSEL1=0, GSEL0=1		± 4
	GSEL1=1, GSEL0=0		± 8
Digital Bit Depth[4]			12 or 14
Zero-g Offset		mg	±25
Zero-g Offset Temperature Coefficient		± mg/ºC	0.25
Sensitivity	GSEL1=0, GSEL=0 (± 2g)	mg/LSB	0.98
	GSEL1=0, GSEL0=1 (± 4g)		1.95
	GSEL1=1, GSEL0=0 (± 8g)		3.91
Sensitivity Temperature Coefficient		± %/ºC	0.03
Positive Self Test Output change on Activation		g	1.4 (x) 0.7 (y) 0.6 (z)
Negative Self Test Output change on Activation		g	-0.15 (x) -0.4 (y) -0.4 (z)
Sensor Mechanical Resonance (-3dB)[1]		Hz	3500 (xy) 1800 (z)
Integral Non-Linearity		% of FS	1
Cross Axis Sensitivity[2]		± %	0.5 (S_{xy}) -0.4 (S_{xz}) 0.2 (S_{yx}) -0.2 (S_{yz}) 0.2 (S_{zx}) 0.7 (S_{zy})
Noise[3] (at 50Hz)		mg (RMS)	1.25

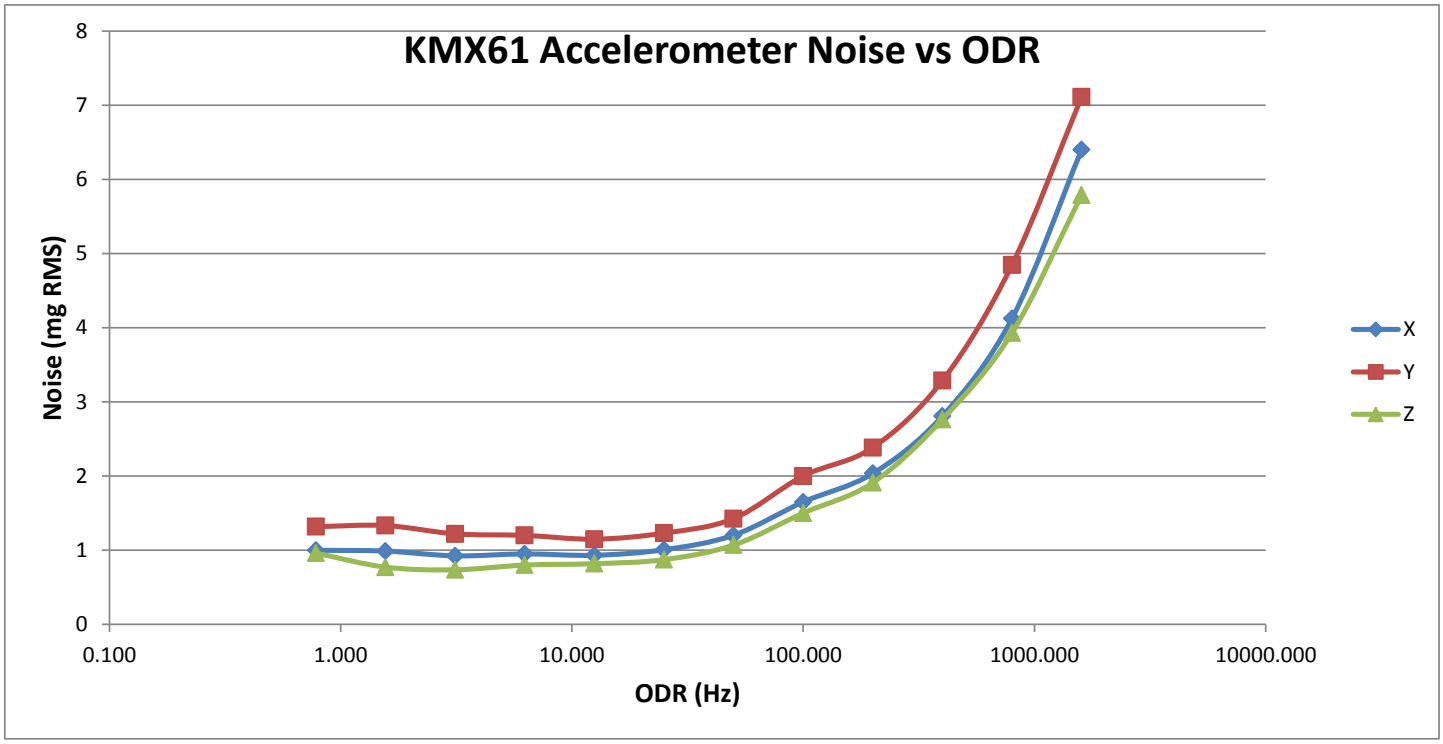
Notes:

1. Resonance as defined by the dampened mechanical sensor.
2. As measured in a test socket. The cross axis sensitivity that is measured is the by-product of positional inaccuracies at all stages of test and assembly.
3. See plot below for noise performance over ODR for all three axes.
4. 14 bit depth for 8g mode available, and 12 bit depth for 2g, 4g, and 8g

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Table 3. Electrical

Parameters		Units	Min	Typical	Max
Supply Voltage (Vdd)	Operating	V	1.8	2.5	3.3
I/O Pads Supply Voltage (Vio)		V	1.7		Vdd
Current Consumption	Operating (mag + accel)	µA		400	
	Magnetometer only			300	
	Accelerometer only			150	
	Standby			1	5
Output Low Voltage[1]		V	-	-	0.3 * Vio
Output High Voltage		V	0.9 * Vio	-	-
Input Low Voltage		V	-	-	0.2 * Vio
Input High Voltage		V	0.8 * Vio	-	-
I^2C Communication Rate[2,3]		MHz	0.1	0.4	3.4
Output Data Rate		Hz	0.781	100	1600
Filter -3dB Cutoff[4]		Hz		ODR/2	
Internal Oscillator Tolerance		%	-10		10

Notes:

1. Assuming I^2C communication and minimum 1.5kΩ pull-up resistor on SCL and SDA.
2. Assuming max bus capacitance load of 20pF.
3. The I^2C bus supports Standard-Mode, Fast-Mode and High Speed Mode.
4. User selectable via ODR control register setting

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KMX61 Transition Timing Diagram

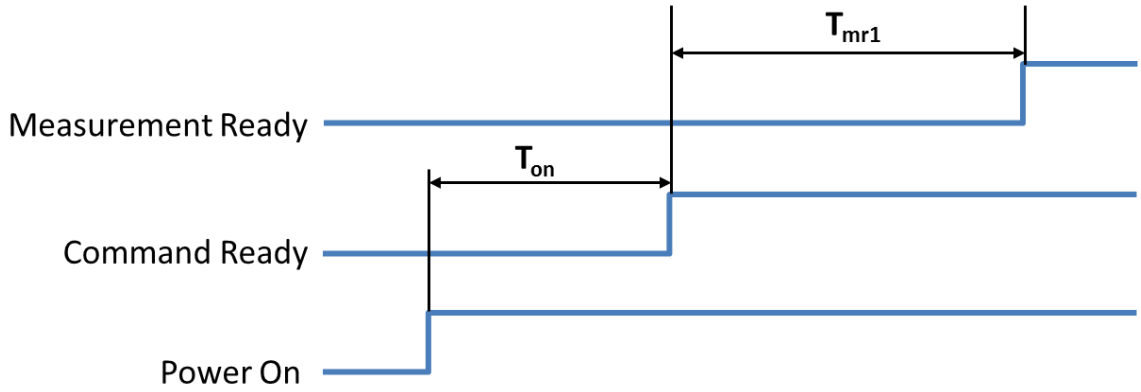


Table 4. Transition Timing

Symbol	Description	Units	Min	Typ	Max
T_{on}	Power On to Ready State (Power on Reset Time)	ms		10	
T_{mr1}	Inactive to Active State (Measurement Ready varies by ODR)	ms		Table 5	

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KMX61 Start Up Time

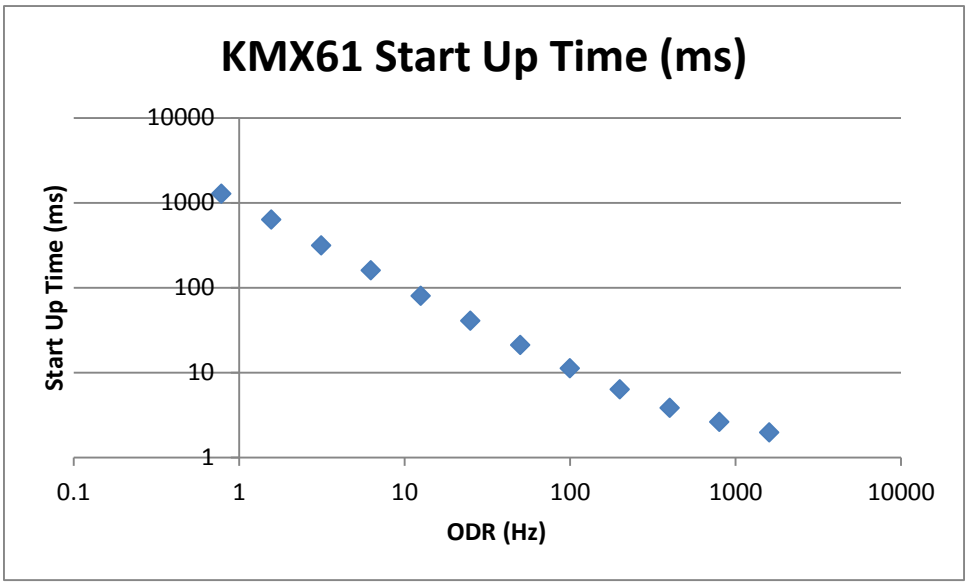


Table 5. Start Up Time

Time from sensor enable to Valid output.

KMX61 Start Up Time (ms)	
ODR (Hz)	Time (ms)
1600	2.0
800	2.6
400	3.8
200	6.3
100	11
50	21
25	40
12.5	79
6.25	158
3.125	312
1.5625	629
0.78125	1260

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KMX61 I²C Timing Diagram

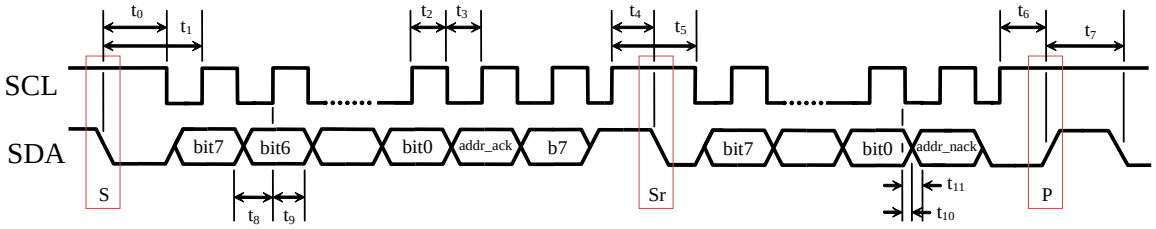


Table 6. I²C Timing (Fast Mode)

Number	Description	MIN	MAX	Units
t_0	SDA low to SCL low transition (Start event)	50	-	ns
t_1	SDA low to first SCL rising edge	100	-	ns
t_2	SCL pulse width: high	100	-	ns
t_3	SCL pulse width: low	100	-	ns
t_4	SCL high before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: high during a S/Sr/P event	100	-	ns
t_6	SCL high before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: high	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I²C CLK	2.5	-	us

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Table 7. Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (Vdd)	Absolute Limits	V	-0.3	-	3.6
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000



Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.



This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout."

HF

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

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Application Schematic

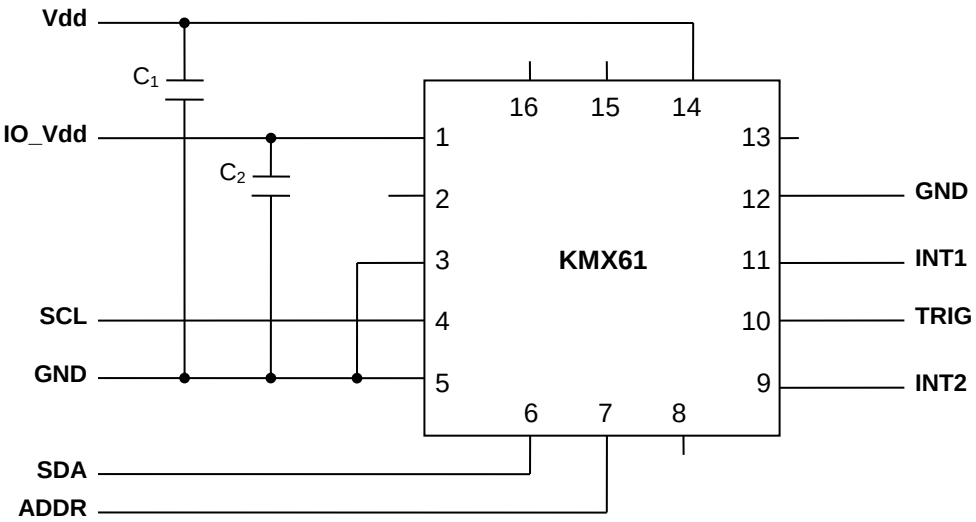


Table 8. KMX61 Pin Descriptions

Pin	Name	Description
1	IO Vdd	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
2	Reserved	Leave this pin unconnected or alternatively couple this pin to ground with a 1 uF ceramic capacitor.
3	GND	Ground
4	SCL	I^2C Serial Clock
5	GND	Ground
6	SDA	I^2C Serial Data
7	ADDR	I^2C Address pin .This pin can be connected to IO_VDD or GND to determine the I2C Device Address.
8	NC	Not Internally Connected
9	INT2	Physical Interrupt 2
10	TRIG	Trigger input for buffer. Connect to GND if not used.
11	INT1	Physical Interrupt 1
12	GND	Ground
13	NC	Not Internally Connected
14	Vdd	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
15	NC	Not Internally Connected
16	NC	Not Internally Connected

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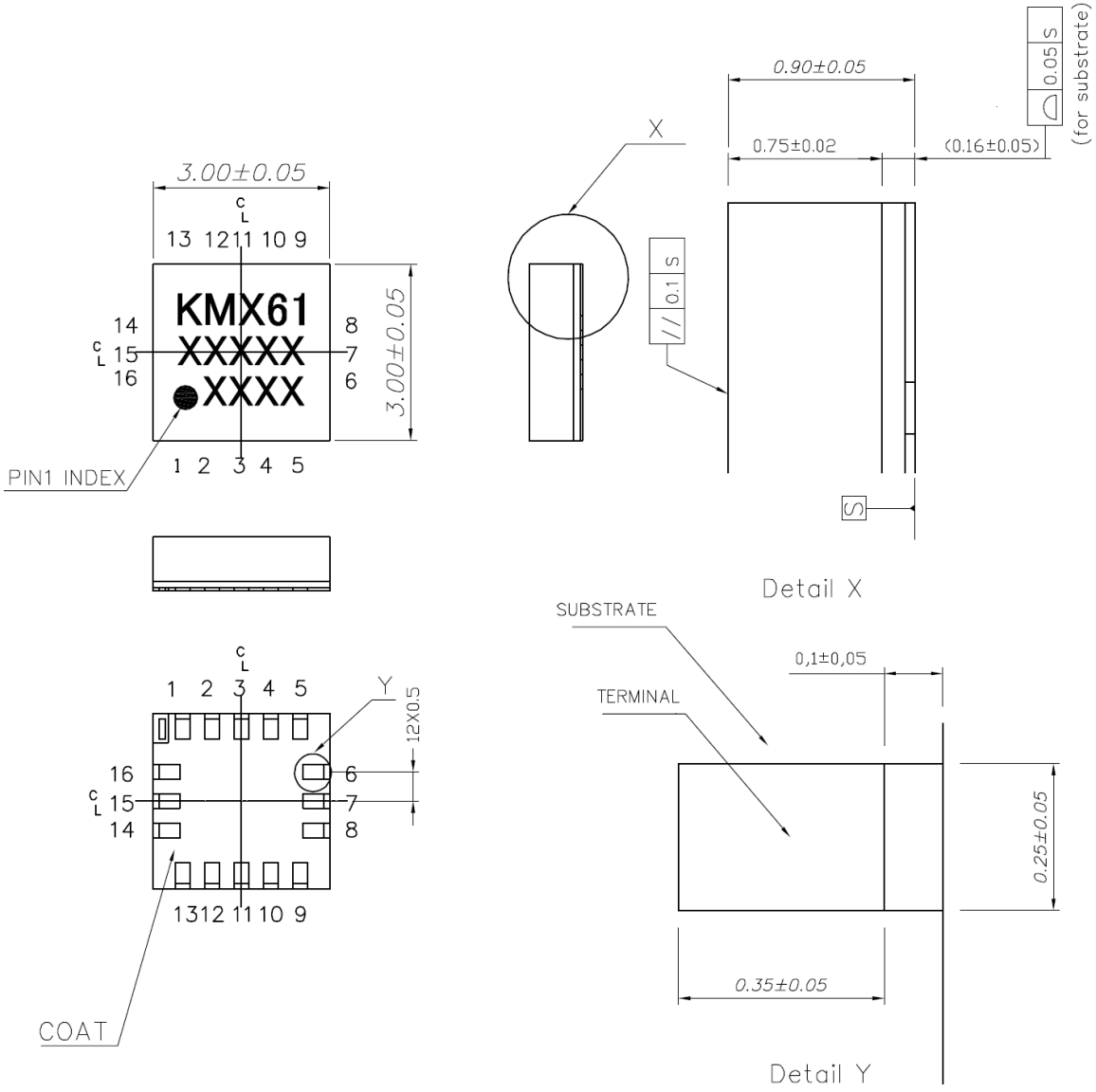
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Package Dimensions and Orientation:

Dimensions

3 x 3 x 0.9 mm LGA



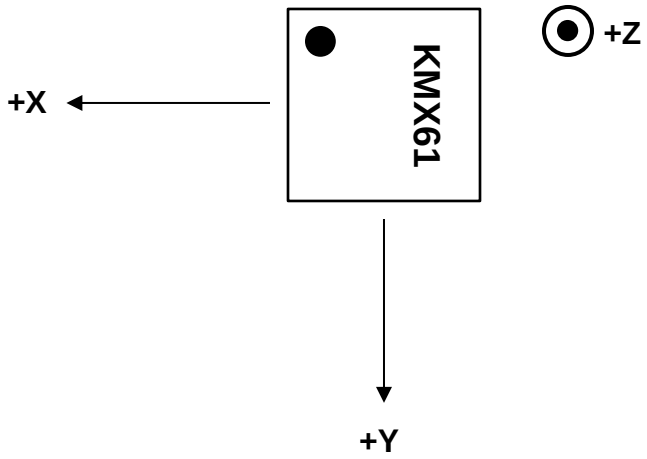
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Orientation

When device is moved in +X, +Y, or +Z direction, the corresponding accelerometer output will increase. When the +X, +Y, or +Z arrow is directed toward North, the magnetometer output of that axis is positive.



Board Layout

Please avoid mounting this product on the part in which magnetic field disturbance exists, such as near any parts containing ferrous materials.

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KMX61 Digital Interface

The Kionix KMX61 digital sensor has the ability to communicate on the I^2C digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system processors. The I2C interface is compliant with high-speed mode, fast mode and standard mode I2C protocols.

The serial interface terms and descriptions as indicated in Table 8 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 8. Serial Interface Terminologies

I^2C Serial Interface

As previously mentioned, the KMX61 has the ability to communicate on an I^2C bus. I^2C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The system Master provides the serial clock signal and addresses Slave devices on the bus. The KMX61 always operates as a Slave device during standard Master-Slave I^2C operation.

I^2C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I^2C bus is considered free when both lines are high.

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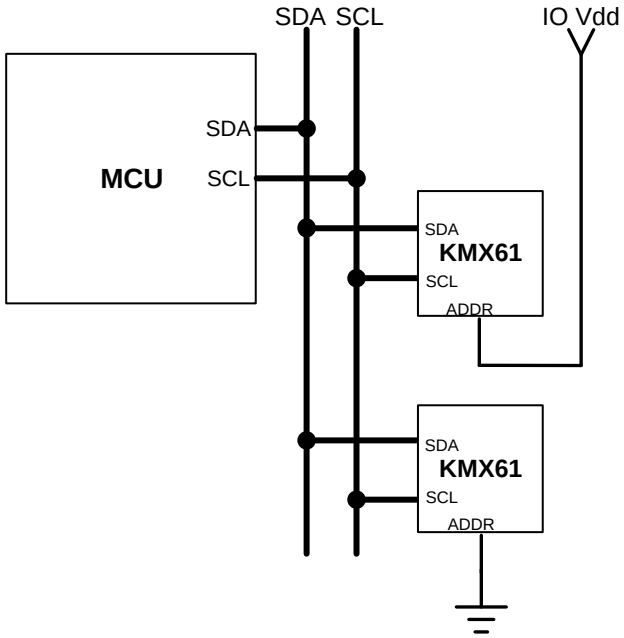


Figure 1. Multiple KMX61 I²C Connection

Description	Address Pad	7 bit Address	Address	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
I2C Wr	IO_VDD	0Fh	1Eh	0	0	0	1	1	1	1	0
I2C Rd	IO_VDD	0Fh	1Fh	0	0	0	1	1	1	1	1
I2C Wr	GND	0Eh	1Ch	0	0	0	1	1	1	0	0
I2C Rd	GND	0Eh	1Dh	0	0	0	1	1	1	0	1

Table 9. I2C Address

I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally-stored address. If they match, the device considers itself addressed by the Master. The KMX61's Slave Address is comprised of two programmable parts, which allows for connection of multiple KMX61's to the same I²C bus. The LSB is determined by the

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assignment of ADDR to GND or IO_Vdd. Figure 1 and Table above shows how two KMX61's would be implemented on an I2C bus.

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I^2C bus is now free. Note that if the KMX61 is accessed through I^2C protocol before the startup is finished a NACK signal is sent.

Writing to a KMX61 8-bit Register

Upon power up, the Master must write to the KMX61's control registers to set its operational mode. Therefore, when writing to a control register on the I^2C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KMX61 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KMX61 to which 8-bit register the Master will be writing the data. Since this is I^2C mode, the MSB of the RA command should always be zero (0). The KMX61 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KMX61 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KMX61 is now stored in the appropriate register. The KMX61 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page. When the auto-increment feature reaches register address 0x7F (Buffer Read), it stops and does not advance to register address 0x80. A new read command must be issued for registers above 0x7F. The part then continues to auto-increment until it reaches address 0xFF.

Reading from a KMX61 8-bit Register

When reading data from a KMX61 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KMX61 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KMX61 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KMX61 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KMX61 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page.

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Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I^2C bus and how the Master and Slave interact during these transfers. Table 10 defines the I^2C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 10. I^2C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

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HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5. HS-mode data transfer of the Master writing one byte to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	S	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

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Power Modes

The KMX61 has four power modes: Off, Stand-by, Sleep, Enabled. The part exists in one of these four modes at any given time. Off and Stand-by modes have very low current consumptions.

Power Mode	Bus State	V_{IO}	V_{dd}	Function	Outputs
Off	-	OFF	OFF	No sensor activity	Not available
		ON	OFF		
		OFF	ON		
Stand-by	Active	ON	ON	Waiting activation command	Not available
Sleep	Active	ON	ON	Accelerometer active looking for motion wake up	Accel registers only – no buffer, no DRDY int
Enabled	Active	ON	ON	All functionalities available	All sensors available

Off mode

One or both of the power supplies (V_{dd} or V_{IO}) are not powered. The sensor is completely inactive and neither reporting nor communicating. Bus communication actions of other devices are not disturbed if they are using the same bus interface as this component.

Initial Startup

The preferred startup sequence is to turn on V_{IO} before V_{dd}, but if V_{dd} is turned on first, the component will not affect the bus communications (no latch-up or other problems during engine system level wake-up).

Power On Reset (POR) is performed every time when:

1. V_{IO} supply is valid
2. V_{dd} power supply is going to valid level

OR

1. V_{IO} power supply is going to valid level
2. V_{dd} supply is valid

When POR occurs, the registers are loaded from OTP and the part is put into Stand-by mode.

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Stand-by mode

The primary function of the stand-by mode is to ensure fast wake-up to active mode and to minimize current consumption. This mode is set as default when both power supplies are applied and the POR function occurs. A Soft Reset command also performs the POR function and puts the part into Stand-by mode.

Stand-by mode is a low power waiting state for fast turn on time. Bus communication actions of other components are not disturbed if they are using the same bus. There is only one possible way to change to active mode – a register command from the external application processor via the I^2C bus.

Sleep mode

While in sleep mode, the accelerometer is periodically taking a measurement to detect if there is any motion. Data in the accelerometer registers is being updated, however, there is no data ready interrupt being reported. Also, no data is being sent to the buffer.

Enable mode

Stand-by-mode can be changed to Enabled mode by writing to register STBY_REG.

This engages the full functionality of accelerometer and/or magnetometer measurements in a higher power, higher resolution mode. The host has the ability to change settings in the control register back to Stand-by mode for either or both the accelerometer and magnetometer. If enabled, the back to sleep function will put the part into the Sleep mode.

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KMX61 Embedded Registers

The KMX61 has 49 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and also describes bit functions of each register. Table 11 below provides a listing of the accessible 8-bit registers and their addresses.

Table 11. I^2C Register Map

I2C Address (Hex)	Register Name	Type R/W
00h	WHO_AM_I	R
01h	INS1	R
02h	INS2	R
03h	STATUS_REG	R
0Ah	ACCEL_XOUT_L	R
0Bh	ACCEL_XOUT_H	R
0Ch	ACCEL_YOUT_L	R
0Dh	ACCEL_YOUT_H	R
0Eh	ACCEL_ZOUT_L	R
0Fh	ACCEL_ZOUT_H	R
10h	TEMP_OUT_L	R
11h	TEMP_OUT_H	R
12h	MAG_XOUT_L	R
13h	MAG_XOUT_H	R
14h	MAG_YOUT_L	R
15h	MAG_YOUT_H	R
16h	MAG_ZOUT_L	R
17h	MAG_ZOUT_H	R
18h	XOUT_HPF_L	R
19h	XOUT_HPF_H	R
1Ah	YOUT_HPF_L	R
1Bh	YOUT_HPF_H	R
1Ch	ZOUT_HPF_L	R
1Dh	ZOUT_HPF_H	R
24h	SN_1	R

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25h	SN_2	R
26h	SN_3	R
27h	SN_4	R
28h	INL	W
29h	STBY_REG	R/W
2Ah	CNTL1	R/W
2Bh	CNTL2	R/W
2Ch	ODCNTL	R/W
2Dh	INC1	R/W
2Eh	INC2	R/W
2Fh	INC3	R/W
3Ch	COTR	R
3Dh	WUFTH	R/W
3Eh	WUFC	R/W
3Fh	BTH	R/W
40h	BTSC	R/W
4Ch	TEMP_EN_CNTL	R/W
60h	SELF_TEST	W
76h	BUF_THRESH_H	R/W
77h	BUF_THRESH_L	R/W
78h	BUF_CTRL1	R/W
79h	BUF_CTRL2	R/W
7Ah	BUF_CLEAR	W
7Bh	BUF_STATUS_REG	R
7Ch	BUF_STATUS_H	R
7Dh	BUF_STATUS_L	R
7Eh	BUF_READ	R

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Magnetometer Outputs

These registers contain 14-bits of valid magnetic field data for each axis. The data is protected from overwrite during each read, and can be converted from digital counts to magnetic field strength (μT) per Figure 2 below.

14-bit Data	Magnetic field μT
0111 1111 1111 11	+1199.8535 μT
0111 1111 1111 10	+1199.7070 μT
…	…
…	…
0000 0000 0000 01	+0.1465 μT
0000 0000 0000 00	0 μT
1111 1111 1111 11	-0.1465 μT
…	…
…	…
1000 0000 0000 01	-1199.8535 μT
1000 0000 0000 00	-1200.0000 μT

Figure 2. Magnetic field (μT) Calculation

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Accelerometer Outputs

These registers contain up to 14-bits of valid acceleration data for each axis depending on the setting of the GSEL bits in CTRL_REG1. The acceleration outputs are represented in 14-bit valid 8g data when GSEL = '11'. The acceleration outputs are represented in 12-bit valid 2g, 4g, or 8g data when GSEL = '00', GSEL = '01', or GSEL = '10'. The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per Figure 3 below. The register acceleration output binary data is represented in N-bit 2's complement format. For example, if N = 12 bits, then the Counts range is from -2048 to 2047.

14-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = +/-8g
0111 1111 1111 11	8191	+7.999g
0111 1111 1111 10	8190	+7.998g
…	…	…
0000 0000 0000 01	1	+0.001g
0000 0000 0000 00	0	0.000g
1111 1111 1111 11	-1	-0.001g
…	…	…
1000 0000 0000 01	-8191	-7.999g
1000 0000 0000 00	-8192	-8.000g

12-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111 1111	2047	+1.999g	+3.998g	+7.996g
0111 1111 1110	2046	+1.998g	+3.996g	+7.992g
…	…	…	…	…
0000 0000 0001	1	+0.001g	+0.002g	+0.004g
0000 0000 0000	0	0.000g	0.000g	0.000g
1111 1111 1111	-1	-0.001g	-0.002g	-0.004g
…	…	…	…	…
1000 0000 0001	-2047	-1.999g	-3.998g	-7.996g
1000 0000 0000	-2048	-2.000g	-4.000g	-8.000g

Figure 3. Acceleration (g) Calculation

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Temperature Output

The temperature registers contain up to 14-bits of temperature data. If only register TEMP_OUT_H is used, then the sensitivity can be considered as 1 count/°C. If both registers TEMP_OUT_H and TEMP_OUT_L are used (14 bits), then sensitivity can be considered as 64 count/°C.

8-bit Register Data TEMP_OUT_H (2's complement)	Equivalent Counts in decimal	Temperature (°C)
0101 0101	85	+85 °C
…	…	…
0000 0001	1	+1 °C
0000 0000	0	0 °C
1111 1111	-1	-1 °C
…	…	…
1101 1000	-40	-40 °C

14-bit Register Data (2's complement)	Equivalent Counts in decimal	Temperature (°C)
0101 0011 0000 01	5312	+84.992 °C
…	…	…
0000 0001 0000 00	64	+1.024 °C
…	…	…
0000 0000 0000 01	1	+0.016 °C
0000 0000 0000 00	0	0.000 °C
1111 1111 1111 10	-1	-0.016 °C
…	…	…
1111 1110 1111 11	-64	-1.024 °C
…	…	…
1101 1000 1111 00	-2500	-40.000 °C

Figure 4. Temperature (°C) Calculation

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Register Descriptions

WHO_AM_I

This register can be used for supplier recognition, as it can be factory written to a known byte value. The default value is 0x12h.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
WHO_AM_I	00h	R	12h	WAI<7>	WAI<6>	WAI<5>	WAI<4>	WAI<3>	WAI<2>	WAI<1>	WAI<0>

INS1

Interrupt source register 1 –This Register tells which function caused an interrupt.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
INS1	01h	R	na	0	BFI	WMI	DRDY_ACCEL	DRDY_MAG	0	WUFS	BTS

BFI *- indicates that the buffer is full. This bit is cleared when the data is read or the interrupt release register (INL Register) is read.*
BFI = 0 – Buffer is not full
BFI = 1 – Buffer is full

WMI *- indicates that user-defined buffer watermark has been reached. This bit is cleared when the data is read or cleared to below the WMI threshold.*
WMI = 0 – Buffer watermark not reached
WMI = 1 – Buffer watermark reached

DRDY_ACCEL *- indicates that new acceleration data is available. This bit is cleared when the data is read or the interrupt release register (INL Register) is read.*
DRDY = 0 – New acceleration data not available
DRDY = 1 – New acceleration data available

DRDY_MAG *- indicates that new magnetometer data is available. This bit is cleared when the data is read or the interrupt release register (INL Register) is read.*
DRDY = 0 – New acceleration data not available
DRDY = 1 – New acceleration data available

WUFS *- Wake up, This bit is cleared when the interrupt source latch register (INL Register) is read.*
WUFS = 1 – Motion has activated the interrupt
WUFS = 0 – No motion

BTS *– Back to Sleep interrupt*
BTS = 0 – normal operating mode, motion is occurring
BTS = 1 – lack of motion has activated the interrupt

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INS2

Interrupt source register 2 – This Register reports the axis and direction of the motion that triggered the wakeup interrupt.

	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
INS2	02h	R	na	0	0	XNWU	XPWU	YNWU	YPWU	ZNWU	ZPWU

XNWU *- x negative (x-)*
XPWU *- x positive (x+)*
YNWU *- y negative (y-)*
YPWU *- y positive (y+)*
ZNWU *- z negative (z-)*
ZPWU *- z positive (z+)*

STATUS_REG

Status register.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
STATUS_REG	03h	R	na	0	0	0	INT	0	0	0	0

INT *reports the combined (OR) interrupt information of DRDY, WUFS, and BTS.*
0= no interrupt event, 1= interrupt event has occurred.

ACCEL_OUT

Accelerometer output (12 bit resolution applicable to +/-2g, +/-4g, +/-8g ranges)

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
ACCEL_XOUT_L	0Ah	R	na	ACC_X<3>	ACC_X<2>	ACC_X<1>	ACC_X<0>	0	0	0	0
ACCEL_XOUT_H	0Bh	R	na	ACC_X<11>	ACC_X<10>	ACC_X<9>	ACC_X<8>	ACC_X<7>	ACC_X<6>	ACC_X<5>	ACC_X<4>
ACCEL_YOUT_L	0Ch	R	na	ACC_Y<3>	ACC_Y<2>	ACC_Y<1>	ACC_Y<0>	0	0	0	0
ACCEL_YOUT_H	0Dh	R	na	ACC_Y<11>	ACC_Y<10>	ACC_Y<9>	ACC_Y<8>	ACC_Y<7>	ACC_Y<6>	ACC_Y<5>	ACC_Y<4>
ACCEL_ZOUT_L	0Eh	R	na	ACC_Z<3>	ACC_Z<2>	ACC_Z<1>	ACC_Z<0>	0	0	0	0
ACCEL_ZOUT_H	0Fh	R	na	ACC_Z<11>	ACC_Z<10>	ACC_Z<9>	ACC_Z<8>	ACC_Z<7>	ACC_Z<6>	ACC_Z<5>	ACC_Z<4>

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Accelerometer output (14 bit resolution only when CNTL1 (GSEL = '11'), +/-8g range)

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
ACCEL_XOUT_L	0Ah	R	na	ACC_X<5>	ACC_X<4>	ACC_X<3>	ACC_X<2>	ACC_X<1>	ACC_X<0>	0	0
ACCEL_XOUT_H	0Bh	R	na	ACC_X<13>	ACC_X<12>	ACC_X<11>	ACC_X<10>	ACC_X<9>	ACC_X<8>	ACC_X<7>	ACC_X<6>
ACCEL_YOUT_L	0Ch	R	na	ACC_Y<5>	ACC_Y<4>	ACC_Y<3>	ACC_Y<2>	ACC_Y<1>	ACC_Y<0>	0	0
ACCEL_YOUT_H	0Dh	R	na	ACC_Y<13>	ACC_Y<12>	ACC_Y<11>	ACC_Y<10>	ACC_Y<9>	ACC_Y<8>	ACC_Y<7>	ACC_Y<6>
ACCEL_ZOUT_L	0Eh	R	na	ACC_Z<5>	ACC_Z<4>	ACC_Z<3>	ACC_Z<2>	ACC_Z<1>	ACC_Z<0>	0	0
ACCEL_ZOUT_H	0Fh	R	na	ACC_Z<13>	ACC_Z<12>	ACC_Z<11>	ACC_Z<10>	ACC_Z<9>	ACC_Z<8>	ACC_Z<7>	ACC_Z<6>

TEMP_OUT

Temperature Output

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
TEMP_OUT_L	10h	R	na	Temp<5>	Temp <4>	Temp<3>	Temp <2>	Temp <1>	Temp <0>	0	0
TEMP_OUT_H	11h	R	na	Temp<13>	Temp <12>	Temp<11>	Temp <10>	Temp <9>	Temp <8>	Temp <7>	Temp <6>

MAG_OUT

MAG output.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
MAG_XOUT_L	12h	R	na	MAG_X<5>	MAG_X<4>	MAG_X<3>	MAG_X<2>	MAG_X<1>	MAG_X<0>	0	0
MAG_XOUT_H	13h	R	na	MAG_X<13>	MAG_X<12>	MAG_X<11>	MAG_X<10>	MAG_X<9>	MAG_X<8>	MAG_X<7>	MAG_X<6>
MAG_YOUT_L	14h	R	na	MAG_Y<5>	MAG_Y<4>	MAG_Y<3>	MAG_Y<2>	MAG_Y<1>	MAG_Y<0>	0	0
MAG_YOUT_H	15h	R	na	MAG_Y<13>	MAG_Y<12>	MAG_Y<11>	MAG_Y<10>	MAG_Y<9>	MAG_Y<8>	MAG_Y<7>	MAG_Y<6>
MAG_ZOUT_L	16h	R	na	MAG_Z<5>	MAG_Z<4>	MAG_Z<3>	MAG_Z<2>	MAG_Z<1>	MAG_Z<0>	0	0
MAG_YOUT_H	17h	R	na	MAG_Z<13>	MAG_Z<12>	MAG_Z<11>	MAG_Z<10>	MAG_Z<9>	MAG_Z<8>	MAG_Z<7>	MAG_Z<6>

ACCEL_OUT_HPF

High-pass filtered accelerometer output.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
XOUT_HPF_L	18h	R	na	XHP<3>	XHP<2>	XHP<1>	XHP<0>	0	0	0	0
XOUT_HPF_H	19h	R	na	XHP<11>	XHP<10>	XHP<9>	XHP<8>	XHP<7>	XHP<6>	XHP<5>	XHP<4>
YOUT_HPF_L	1Ah	R	na	YHP<3>	YHP<2>	YHP<1>	YHP<0>	0	0	0	0
YOUT_HPF_H	1Bh	R	na	YHP<11>	YHP<10>	YHP<9>	YHP<8>	YHP<7>	YHP<6>	YHP<5>	YHP<4>
ZOUT_HPF_L	1Ch	R	na	ZHP<3>	ZHP<2>	ZHP<1>	ZHP<0>	0	0	0	0
ZOUT_HPF_H	1Dh	R	na	ZHP<11>	ZHP<10>	ZHP<9>	ZHP<8>	ZHP<7>	ZHP<6>	ZHP<5>	ZHP<4>

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SN

Individual Identification (serial number)

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
SN_1	24h	R	OTP	SN<7>	SN<6>	SN<5>	SN<4>	SN<3>	SN<2>	SN<1>	SN<0>
SN_2	25h	R	OTP	SN<15>	SN<14>	SN<13>	SN<12>	SN<11>	SN<10>	SN<9>	SN<8>
SN_3	26h	R	OTP	SN<23>	SN<22>	SN<21>	SN<20>	SN<19>	SN<18>	SN<17>	SN<16>
SN_4	27h	R	OTP	SN<31>	SN<30>	SN<29>	SN<28>	SN<27>	SN<26>	SN<25>	SN<24>

INL

Interrupt Latch Release – Latched interrupt source information (at INS1 and INS2) is cleared and physical interrupt latched pin is changed to its inactive state when this register is read.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
INL	28h	W	na	0	0	0	0	0	0	0	0

STBY_REG

Stand-by status

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
STBY_REG	29h	R/W	7Fh	ACT_STBY	0	0	0	0	0	MAG_STBY	ACCEL_STBY

ACCEL_STBY *controls the operating mode of the ASIC_AL's accelerometer*

ACCEL_STBY = 0 – operating mode

ACCEL_STBY = 1 – stand-by mode. WUF and BTS engines will not function.

MAG_STBY *controls the operating mode of the ASIC_AL's magnetometer.*

MAG_STBY = 0 – operating mode. Sensor will respond to WUF and BTS engines if those engines are enabled and ACT_STBY=1.

MAG_STBY = 1 – stand-by mode. Sensor will not respond to WUF and BTS engines if those engines are enabled.

ACT_STBY *allows the ASIC_AL to control the operating mode of all of the connected devices based on the activity state of the device*

ACT_STBY = 0 – feature disabled. If both accelerometer and magnetometer are enabled (ACCEL_STBY=0 and MAG_STBY = 0), neither accelerometer nor magnetometer can be disabled independently. The part has to be disabled by setting both ACCEL_STBY and MAG_STBY to one.

ACT_STBY = 1 – Magnetometer will be enabled when the internal accelerometer measures activity and disabled when the internal accelerometer measures inactivity

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CTRL_REG1

Read/Write control register 1

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
CNTL1	2Ah	R/W	00h	BTSE	WUFE	DRDYE	1	0	0	Gsel1	Gsel0

BTSE *enables the Back to Sleep engine*
BTSE = 0 – disable
BTSE = 1 – enable

WUFE *enables the Wake up engine*
WUFE = 0 – disabled
WUFE = 1 – enable

DRDYE *enables the reporting of the availability of new sensor data on the interrupt pin.*
DRDYE = 0 – disable
DRDYE = 1 – enable

GSEL1, GSEL0 *selects the acceleration range of the accelerometer outputs per the following table.*

GSEL1	GSEL0	Range
0	0	+/-2g, 12 bit
0	1	+/-4g, 12 bit
1	0	+/-8g, 12 bit
1	1	+/-8g, 14-bit

Selected Acceleration Range

Note: After a motion wake-up event, Bit 4 of CTRL_REG1 must be re-written as a 1 to obtain full functionality of the magnetometer and accelerometer.

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CTRL_REG2

Read/Write control register:

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
CNTL2	2Bh	R/W	00h	SRST	STPOL	RESERVED	COTC	0	OWUFA	OWUFB	OWUFC

SRST *Software Reset function*

SRST = 0 – no action

SRST = 1 – start POR routine

STPOL *- ST polarity control*

STPOL = 0 – ST polarity is positive

STPOL = 1 – ST polarity is negative.

COTC *enables the command test function*

COTC= 0 – no action

COTC = 1 – sets AAh to COTR register, when the COTR register is read, COTC is cleared and STR = 55h.

OWUF(2:0): *Output Data Rate at which the wake up (motion detection) performs its function.*

OWUFA	OWUFB	OWUFC	Output Data Rate (Hz)
0	0	0	0.781
0	0	1	1.563
0	1	0	3.125
0	1	1	6.25
1	0	0	12.5
1	0	1	25
1	1	0	50
1	1	1	100

ODCNTL

Output data control register

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
ODCNTL	2Ch	R/W	22h	OSMA	OSMB	OSMC	OSMD	OSAA	OSAB	OSAC	OSAD

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OSA(3:0): *Rate at which data samples from the accelerometer will be updated in the register map.*

OSAA	OSAB	OSAC	OSAD	Output Data Rate (Hz)
0	0	0	0	12.5
0	0	0	1	25
0	0	1	0	50
0	0	1	1	100
0	1	0	0	200
0	1	0	1	400
0	1	1	0	800
0	1	1	1	1600
1	0	0	0	0.781
1	0	0	1	1.563
1	0	1	0	3.125
1	0	1	1	6.25

Table 12. Accelerometer Sampling Rate

OSM(3:0): *Rate at which data samples from the magnetometer will be updated in the register map.*

OSMA	OSMB	OSMC	OSMD	Output Data Rate (Hz)
0	0	0	0	12.5
0	0	0	1	25
0	0	1	0	50
0	0	1	1	100
0	1	0	0	200
0	1	0	1	400
0	1	1	0	800
0	1	1	1	1600
1	0	0	0	0.781
1	0	0	1	1.563
1	0	1	0	3.125
1	0	1	1	6.25

Table 13. Magnetometer Sampling Rate

Note: The FIFO buffer will be updated at the faster of the two output data rates (OSM or OSA).

Note: Before changing the ODR of a sensor, both sensors should be in stand by via the STBY_REG. Write the new ODR value(s) to ODCNTL, then enable the sensor(s) via the STBY_REG.

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INC1

Interrupt control 1 – Physical interrupt pin 1 control

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
INC1	2Dh	R/W	10h	BFI1	WMI1	IEN1	IEA1	IEL1	DRDY_A1	DRDY_M1	WUFS/BTS1

BFI1 - *Buffer full interrupt reported on physical interrupt pin 1*
BFI = 0 – disable
BFI = 1 – enable.
WMI1 *- Watermark interrupt reported on physical interrupt pin 1*
WMI1 = 0 – disable
WMI1 = 1 – enable.
IEN1 *- Enable/disable physical interrupt pin 1*
IEN1 = 0 – disable
IEN1 = 1 – enable.
IEA1 *- Interrupt active level control for interrupt pin 1*
IEA1 = 0 – active low
IEA1 = 1 – active high.
IEL1 *- Interrupt latch control for interrupt pin 1*
IEL1 = 0 – latched
IEL1 = 1 – pulsed. In pulse mode the pulse width is 50us for normal mode and 10us for debug mode.
DRDY_A1 *- Accelerometer Data ready reported on physical interrupt pin 1 (DRDYE must be set)*
DRDY_A1 = 0 – disable
DRDY_A1 = 1 – enable.
DRDY_M1 *- Magnetometer Data ready reported on physical interrupt pin 1(DRDYE must be set)*
DRDY_M1 = 0 – disable
DRDY_M1 = 1 – enable.
WUFS/BTS1 *- Wake up/Back to Sleep interrupt reported on physical interrupt pin 1*
WUFS/BTS1 = 0 – disable
WUFS/BTS1 = 1 – enable.

INC2

Interrupt control 2 – Physical interrupt pin 2 control

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
INC2	2Eh	R/W	10h	BFI2	WMI2	IEN2	IEA2	IEL2	DRDY_A2	DRDY_M2	WUFS/BTS2

BFI2 - *Buffer full interrupt reported on physical interrupt pin 2*

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BFI = 0 – disable
BFI = 1 – enable.

WMI2 *- Watermark interrupt reported on physical interrupt pin 2*
WMI1 = 0 – disable
WMI1 = 1 – enable.

IEN2 *- Enable/disable physical interrupt pin 2*
IEN1 = 0 – disable
IEN1 = 1 – enable.

IEA2 *- Interrupt active level control for interrupt pin 2*
IEA1 = 0 – active low
IEA1 = 1 – active high.

IEL2 *- Interrupt latch control for interrupt pin 2*
IEL1 = 0 – latched
IEL1 = 1 – pulsed. In pulse mode the pulse width is 50us for normal mode and 10us for debug mode.

DRDY_A2 *- Accelerometer Data ready reported on physical interrupt pin 2*
DRDY_A1 = 0 – disable
DRDY_A1 = 1 – enable.

DRDY_M2 *- Magnetometer Data ready reported on physical interrupt pin 2*
DRDY_M1 = 0 – disable
DRDY_M1 = 1 – enable.

WUFS/BTS2 *- Wake up/Back to Sleep interrupt reported on physical interrupt pin 2*
WUFS/BTS1 = 0 – disable
WUFS/BTS1 = 1 – enable.

INC3

Interrupt control 3 – This register controls which axis and direction of detected motion can cause an interrupt.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
INC3	2Fh	R/W	3Fh	0	0	NXWUE	PXWUE	NYWUE	PYWUE	NZWUE	PZWUE

NXWUE *- x negative (x-) mask for WUF, 0=disable, 1=enable.*
PXWUE *- x positive (x+) mask for WUF, 0=disable, 1=enable.*
NYWUE *- y negative (y-) mask for WUF, 0=disable, 1=enable.*
PYWUE *- y positive (y+) mask for WUF, 0=disable, 1=enable.*
NZWUE *- z negative (z-) mask for WUF, 0=disable, 1=enable.*
PZWUE *- z positive (z+) mask for WUF, 0=disable, 1=enable.*

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COTR (STR)

This register can be used to verify proper communication functionality. It always has a byte value of 0x55h unless the COTC bit in CTRL_REG2 is set. At that point this value is set to 0xAAh. The byte value is returned to 0x55h after reading this register.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
COTR	3Ch	R	55h	COTR <7>	COTR <6>	COTR <5>	COTR <4>	COTR <3>	COTR <2>	COTR <1>	COTR <0>

WUF_THRESH (ATH)

This register sets the acceleration threshold, WUF Threshold, that is used to detect a general motion input. WUF_THRESH scales with GSEL1-GSEL0 in CTRL_REG1, and the KMX61 will ship from the factory with this value set to correspond to a change in acceleration of 0.5g when configured to +/-8g. Note that to properly change the value of this register, the accelerometer should be in stand by via the STBY_REG.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
WUFTH	3Dh	R/W	08h	WUFTH <7>	WUFTH <6>	WUFTH <5>	WUFTH <4>	WUFTH <3>	WUFTH <2>	WUFTH <1>	WUFTH <0>

WUF_TIMER

This register is the initial count register for the motion detection timer (0 to 255 counts). Every count is calculated as 1/ODR delay period, where the Motion Wake Up ODR is user-defined per the OWUF bits in CTRL_REG2. A new state must be valid as many measurement periods before the change is accepted. Note that to properly change the value of this register, the accelerometer should be in stand by via the STBY_REG.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
WUFC	3Eh	R/W	00h	WUFC <7>	WUFC <6>	WUFC <5>	WUFC <4>	WUFC <3>	WUFC <2>	WUFC <1>	WUFC <0>

BTS_THRESH (BTH)

This register sets the acceleration threshold, BTS Threshold, which is used to signify when there is no motion input. BTS_THRESH scales with GSEL1-GSEL0 in CTRL_REG1, and the KMX61 will ship from the factory with this value set to correspond to a change in acceleration of 0.5g when configured to +/-8g. Note that to properly change the value of this register, the accelerometer should be in stand by via the STBY_REG.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
BTH	3Fh	R/W	08h	BTH<7>	BTH<6>	BTH<5>	BTH<4>	BTH<3>	BTH<2>	BTH<1>	BTH<0>

BTS_TIMER

This register is the initial count register for the motion detection timer (0 to 255 counts). Every count is calculated as 1/ODR delay period, where the Motion Wake Up ODR is user-defined per the OWUF bits in CTRL_REG2. A new state must be valid as many measurement periods before the change is

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accepted. Note that to properly change the value of this register, the accelerometer should be in stand by via the STBY_REG.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
BTSC	40h	R/W	00h	BTSC <7>	BTSC <6>	BTSC <5>	BTSC <4>	BTSC <3>	BTSC <2>	BTSC <1>	BTSC <0>

SELF_TEST

When 0xCA is written to this register, the accelerometer self-test function is enabled. Electrostatic-actuation of the accelerometer, results in a DC shift of the X, Y and Z axis outputs. Writing 0x00 to this register will return the accelerometer to normal operation.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
SELF_TEST	60h	W	na	1	1	0	0	1	0	1	0

BUF_THRESH

Read/write control register that controls the buffer sample threshold.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
BUF_THRESH_H	76h	R/W	00h	0	SMT_TH<8>	SMT_TH<7>	SMT_TH<6>	SMT_TH<5>	SMT_TH<4>	SMT_TH<3>	SMT_TH<2>
BUF_THRESH_L	77h	R/W	00h	0	0	0	0	0	0	SMT_TH<1>	SMT_TH<0>

***SMP_TH[8:0] Sample Threshold**; determines the number of data bytes that will trigger a watermark interrupt or will be saved prior to a trigger event. The maximum number of data bytes is 512.*

Buffer Model	Sample Function
Bypass	None
FIFO	Specifies how many buffer samples are needed to trigger a watermark interrupt.
Stream	Specifies how many buffer samples are needed to trigger a watermark interrupt.
Trigger	Specifies how many buffer samples before the trigger event are retained in the buffer.
FILO	Specifies how many buffer samples are needed to trigger a watermark interrupt.

Table 14. Sample Threshold Operation by Buffer Mode

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BUF_CTRL1

Read/write control register that controls sample buffer operation.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
BUF_CTRL1	78h	R/W	00h	BUFE	0	BUF_FIE	0	0	0	BUF_M<1>	BUF_M<0>

BUFE *controls activation of the sample buffer.*

BUFE = 0 – sample buffer inactive

BUFE = 1 – sample buffer active

BUF_FIE *controls the buffer full interrupt*

BUF_FIE = 0 – the buffer full interrupt, BFI is disabled

BUF_FIE = 1 – the buffer full interrupt, BFI will be triggered when the buffer is full

BUF_M1, BUF_M0 *selects the operating mode of the sample buffer per Table 15.*

BUF_M1	BUF_M0	Mode	Description
0	0	FIFO	The buffer collects *BUFFER_FULL_BYTES* bytes of data until full, collecting new data only when the buffer is not full.
0	1	Stream	The buffer holds the last *BUFFER_FULL_BYTES* bytes of data. Once the buffer is full, the oldest data is discarded to make room for newer data.
1	0	Trigger	When a trigger event occurs (logic high input on TRIG pin), the buffer holds the last data set of SMP[6:0] samples before the trigger event and then continues to collect data until full. New data is collected only when the buffer is not full.
1	1	FILO	The buffer holds the last *BUFFER_FULL_BYTES* bytes of data. Once the buffer is full, the oldest data is discarded to make room for newer data. Reading from the buffer in this mode will return the most recent data first.

Table 15. Selected Buffer Mode

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BUF_CTRL2

Read/write control register that controls sample buffer operation.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
BUF_CTRL2	79h	R/W	00h	BUF_MAG	BUF_ACC	0	0	0	0	0	0

BUF_MAG *controls the magnetometer input into the sample buffer.*
BUF_MAG = 0 – Magnetometer data is not input into the sample buffer
BUF_MAG = 1 – Magnetometer data is input into the sample buffer

BUF_ACC *controls the Accelerometer input into the sample buffer.*
BUF_ACC = 0 – Accelerometer data is not input into the sample buffer
BUF_ACC = 1 – Accelerometer data is input into the sample buffer

BUF_CLEAR

Latched buffer status information and the entire sample buffer are cleared when any data is written to this register.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
BUF_CLEAR	7Ah	W	00h	0	0	0	0	0	0	0	0

BUF_STATUS_REG

This register reports the status of the sample buffer trigger function.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
BUF_STATUS_REG	7Bh	R	00h	BUF_TRIG	0	0	0	0	0	0	0

BUF_TRIG *reports the status of the buffer's trigger function if this mode has been selected. When using trigger mode, a buffer read should only be performed after a trigger event.*

BUF_STATUS

This register reports the status of the sample buffer.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
BUF_STATUS_H	7Ch	R	00h	0	SMP_LEV<8>	SMP_LEV<7>	SMP_LEV<6>	SMP_LEV<5>	SMP_LEV<4>	SMP_LEV<3>	SMP_LEV<2>
BUF_STATUS_L	7Dh	R	00h	0	0	0	0	0	0	SMP_LEV<1>	SMP_LEV<0>

SMP_LEV[8:0] Sample Level*; reports the number of data bytes that have been stored in the sample buffer. If this register reads 0, no data has been stored in the buffer.*

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BUF_READ

Data in the buffer can be read according to the BUF_M settings in BUF_CTRL1 by executing this command. More samples can be retrieved by continuing to toggle SCL after the read command is executed. Data should advance by using auto-increment. Additional samples cannot be written to the buffer while data is being read from the buffer using auto-increment mode. Output data is in 2's Complement format.

Register	Addr	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
BUF_READ	7Eh	R	na	0	0	0	0	0	0	0	0

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Sample Buffer Feature Description

The 512 byte sample buffer feature of the ASIC_AL accumulates and outputs data based on how it is configured. There are 4 buffer modes available. Data is collected at the highest ODR specified by OSMA:OSMD or OSAA:OSAD in the Output Data Control Register. Each buffer mode accumulates data, reports data, and interacts with status indicators in a slightly different way.

FIFO Mode

Data Accumulation

Sample collection stops when the buffer is full.

Data Reporting

Data is reported with the oldest byte of the oldest sample first (X_L or X based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or reading greater than SMPX.

BUF_RES=0:

SMPX = SMP_LEV[8:0] – SMP_TH[8:0]

Equation 6. Samples Above Sample Threshold

Stream Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 1).

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Trigger Mode

Data Accumulation

When a logic high signal occurs on the TRIG pin, the trigger event is asserted and SMP[8:0] samples prior to the event are retained. Sample collection continues until the buffer is full.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

When a physical interrupt occurs and there are at least SMP[8:0] samples in the buffer, BUF_TRIG in BUF_STATUS_REG2 is asserted.

FILO Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the newest byte of the newest sample first (Z_H or Z based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 1).

Buffer Operation

The following diagrams illustrate the operation of the buffer conceptually. Actual physical implementation has been abstracted to offer a simplified explanation of how the different buffer modes operate. Regardless of the selected mode, the buffer fills sequentially, two-byte at a time and one set_count number of bytes at the highest ODR. Figure 5 shows one 12-byte data sample with accelerometer and magnetometer enabled. The next Figures represent a 10-sample version of the buffer (for simplicity), with Sample Threshold set to 8.

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	Index	Byte	
	0	ACCEL X_L	<---- FIFO read pointer
	1	ACCEL X_H	
	2	ACCEL Y_L	
	3	ACCEL Y_H	
	4	ACCEL Z_L	
	5	ACCEL Z_H	
	6	MAG X_L	
	7	MAG X_H	
	8	MAG Y_L	
	9	MAG Y_H	
	10	MAG Z_L	
	11	MAG Z_H	<---- FILO read pointer
buffer write pointer ---->	12		

Figure 5. One Buffer Sample with accelerometer and magnetometer enabled.

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Note in Figure 6 the location of the FILO read pointer versus that of the FIFO read pointer. The buffer write pointer shows where the next sample will be written to the buffer.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	← FILO read pointer
buffer write pointer →	3		
	4		
	5		
	6		
	7		← Sample Threshold
	8		
	9		

Figure 6. Buffer Filling

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The buffer continues to fill sequentially until the Sample Threshold is reached. Note in Figure 7 the location of the FILO read pointer versus that of the FIFO read pointer.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	← FILO read pointer
buffer write pointer →	7		← Sample Threshold
	8		
	9		

Figure 7. Buffer Approaching Sample Threshold

In FIFO, Stream, and FILO modes, a watermark interrupt is issued when the number of samples in the buffer reaches the Sample Threshold. In trigger mode, this is the point where the oldest data in the buffer is discarded to make room for newer data.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	
	7	Data7	← Sample Threshold/FILO read pointer
buffer write pointer →	8		
	9		

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Figure 8. Buffer at Sample Threshold

In trigger mode, data is accumulated in the buffer sequentially until the Sample Threshold is reached. Once the Sample Threshold is reached, the oldest samples are discarded when new samples are collected. Note in Figure 9 how Data0 was thrown out to make room for Data8.

	Index	Sample	
	0	Data1	← Trigger read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
Trigger write pointer →	7	Data8	← Sample Threshold
	8		
	9		

Figure 9. Additional Data Prior to Trigger Event

After a trigger event occurs, the buffer no longer discards the oldest samples, and instead begins accumulating samples sequentially until full. The buffer then stops collecting samples, as seen in Figure 10. This results in the buffer holding SMP_TH[8:0] samples prior to the trigger event, and SMPX samples after the trigger event.

Index	Sample	
0	Data1	← Trigger read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	

Figure 10. Additional Data After Trigger Event

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In FIFO, Stream, FILO, and Trigger (after a trigger event has occurred) modes, the buffer continues filling sequentially after the Sample Threshold is reached. Sample accumulation after the buffer is full depends on the selected operation mode. FIFO and Trigger modes stop accumulating samples when the buffer is full, and Stream and FILO modes begin discarding the oldest data when new samples are accumulated.

Index	Sample	
0	Data0	← FIFO read pointer
1	Data1	
2	Data2	
3	Data3	
4	Data4	
5	Data5	
6	Data6	
7	Data7	← Sample Threshold
8	Data8	
9	Data9	← FILO read pointer

Figure 11. Buffer Full

After the buffer has been filled in FILO or Stream mode, the oldest samples are discarded when new samples are collected. Note in Figure 12 how Data0 was thrown out to make room for Data10.

Index	Sample	
0	Data1	← FIFO read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	← FILO read pointer

Figure 12. Buffer Full – Additional Sample Accumulation in Stream or FILO Mode

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In FIFO, Stream, or Trigger mode, reading one sample from the buffer will remove the oldest sample and effectively shift the entire buffer contents up, as seen in Figure 13.

Index	Sample	
0	Data1	← FIFO read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	← FILO read pointer
buffer write pointer → 9		

Figure 13. FIFO Read from Full Buffer

In FILO mode, reading one sample from the buffer will remove the newest sample and leave the older samples untouched, as seen in Figure 14.

Index	Sample	
0	Data0	← FIFO read pointer
1	Data1	
2	Data2	
3	Data3	
4	Data4	
5	Data5	
6	Data6	
7	Data7	← Sample Threshold
8	Data8	← FILO read pointer
buffer write pointer → 9		

Figure 14. FILO Read from Full Buffer

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Revision History

REVISION	DESCRIPTION	DATE
1.0	Initial Release	23 June 14

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