ADNS-3040
Ultra Low-Power Optical Mouse Sensor

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant



Description

The ADNS-3040 is an ultra low-power optical navigation sensor. It has a new, low-power architecture and automatic power management modes, making it ideal for battery-and power-sensitive applications such as cordless input devices.

The ADNS-3040 is capable of high-speed motion detection – up to 20 ips and 8g. In addition, it has an on-chip oscillator and LED driver to minimize external components.

The ADNS-3040 along with the ADNS-3120-001 lens, ADNS-2220 clip and HLMP-ED80-PS000 LED form a complete and compact mouse tracking system. There are no moving parts, which means high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

The sensor is programmed via registers through a four-wire serial port. It is packaged in a 20-pin DIP.

Features

- Low power architecture
- Self-adjusting power-saving modes for longest battery life
- High speed motion detection up to 20 ips and 8g
- SmartSpeed self-adjusting frame rate for optimum performance
- Motion detect pin output
- Internal oscillator – no clock input needed
- Selectable 400 and 800 cpi resolution
- Wide operating voltage: 2.6V-3.6V nominal
- Four wire serial port
- Minimal number of passive components

Applications

- Optical Mice
- Optical trackballs
- Integrated input devices
- Battery-powered input devices

Theory of Operation

The ADNS-3040 is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The ADNS-3040 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values.

An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into PS2, USB, or RF signals before sending them to the host PC or game console.

Pinout of ADNS-3040 Optical Mouse Sensor

Pin	Name	Description
1	NCS	Chip select (active low input)
2	MISO	Serial data output (Master In/Slave Out)
3	SCLK	Serial clock input
4	MOSI	Serial data input (Master Out/Slave In)
5	MOTION	Motion Detect (active low output)
6	XY_LED	LED control
7	LED_GND	Ground for LED current
8	NC	No connection
9	AGND	Analog Ground
10	SHTDWN	Shutdown (active high input)
11	AVDD	Analog Supply Voltage
12	GND	Ground
13	GND	Ground
14	AGND	Analog Ground
15	VDD	Supply Voltage
16	GND	Ground
17	NC	No connection
18	NC	No connection
19	AGND	Analog Ground
20	NC	No connection

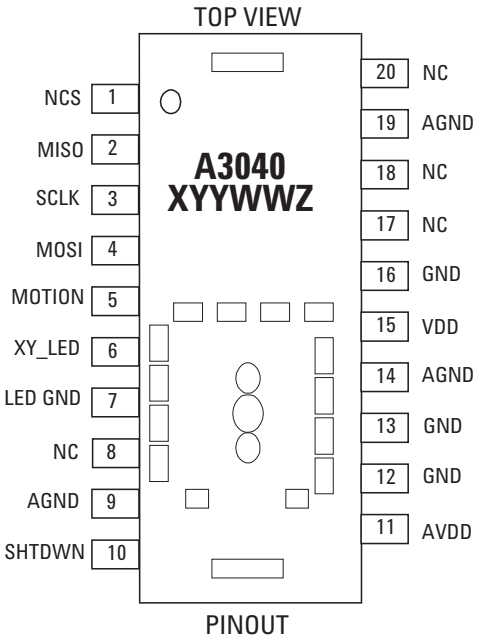
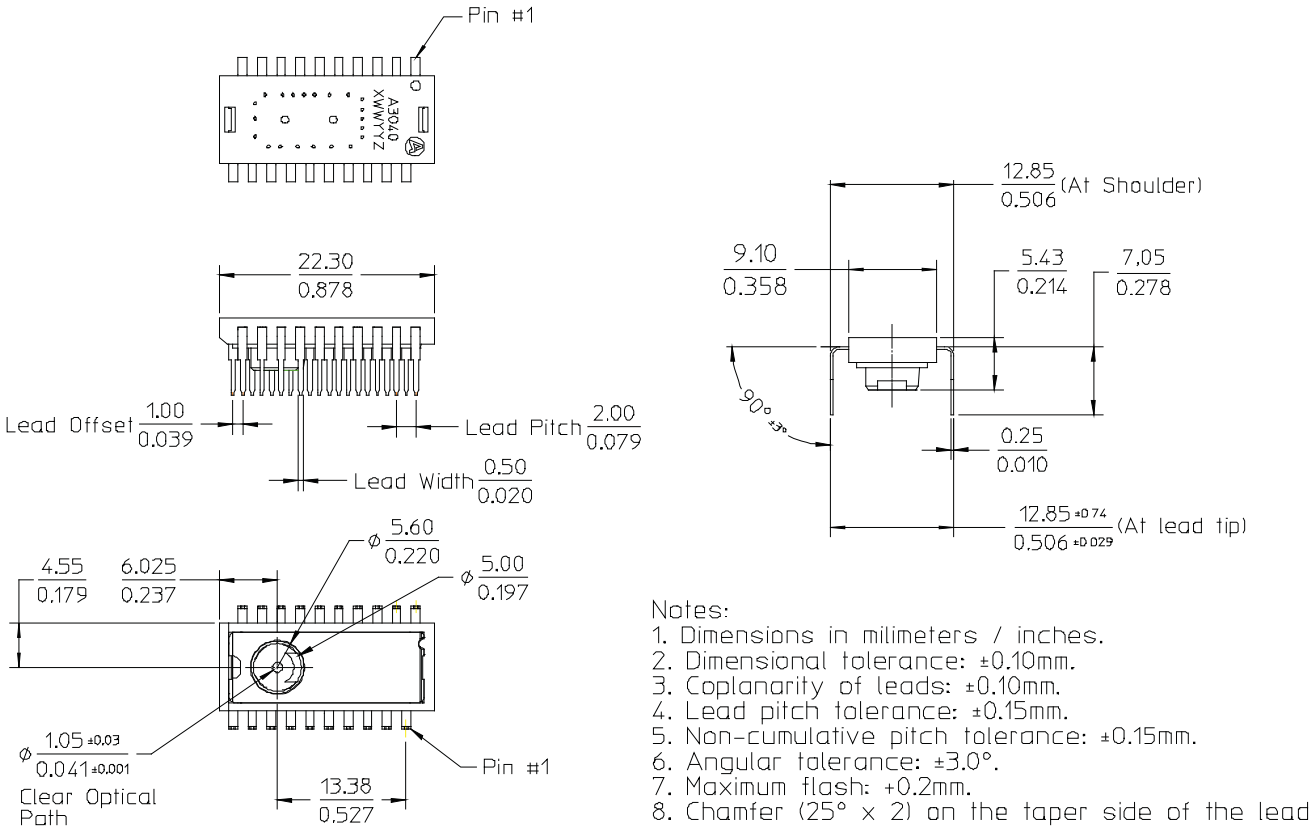


Figure 1. Package outline drawing (top view)



Notes:
1. Dimensions in milimeters / inches.
2. Dimensional tolerance: ±0.10mm.
3. Coplanarity of leads: ±0.10mm.
4. Lead pitch tolerance: ±0.15mm.
5. Non-cumulative pitch tolerance: ±0.15mm.
6. Angular tolerance: ±3.0°.
7. Maximum flash: +0.2mm.
8. Chamfer (25° x 2) on the taper side of the lead

Figure 2. Package outline drawing

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD

Overview of Optical Mouse Sensor Assembly

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment.

The components interlock as they are mounted onto defined features on the base plate.

The ADNS-3040 sensor is designed for mounting on a through-hole PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The ADNS-3120-001 lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor, base plate, and clip with the LED.

The ADNS-2220 clip holds the LED in relation to the lens. The LED must be inserted into the clip and the LED's leads formed prior to loading on the PCB. The clip interlocks the sensor to the lens, and through the lens to the alignment features on the base plate.

The HLMP-ED80-PS000 LED is recommended for illumination.

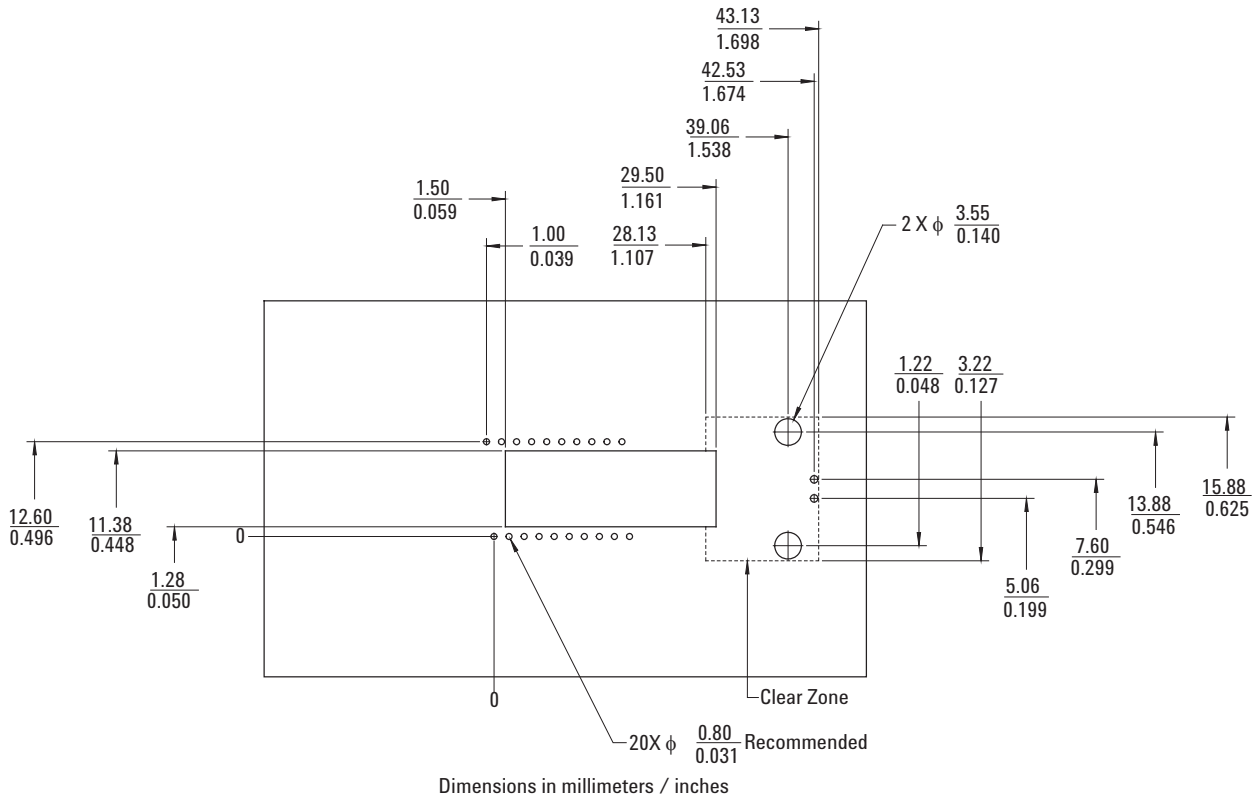


Figure 3. Recommended PCB mechanical cutouts and spacing

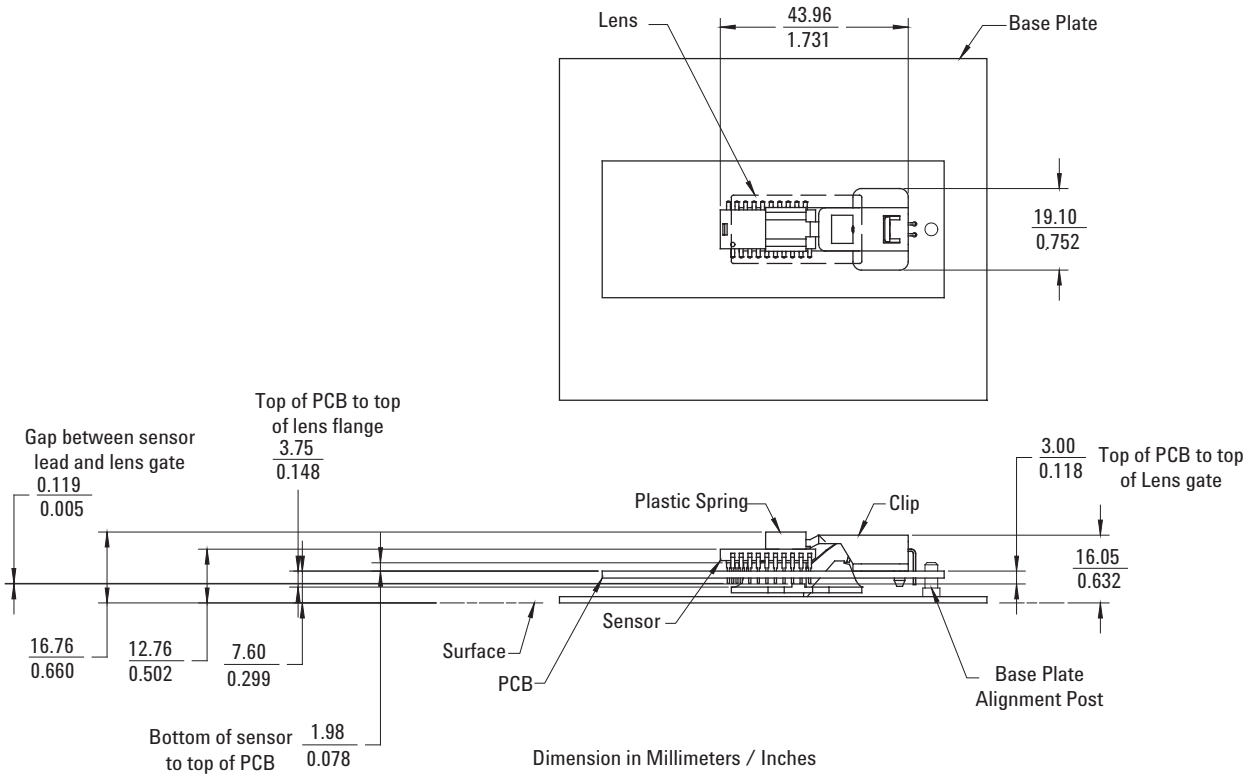


Figure 4. 2D Assembly drawing of ADNS-3040 (top and side view)

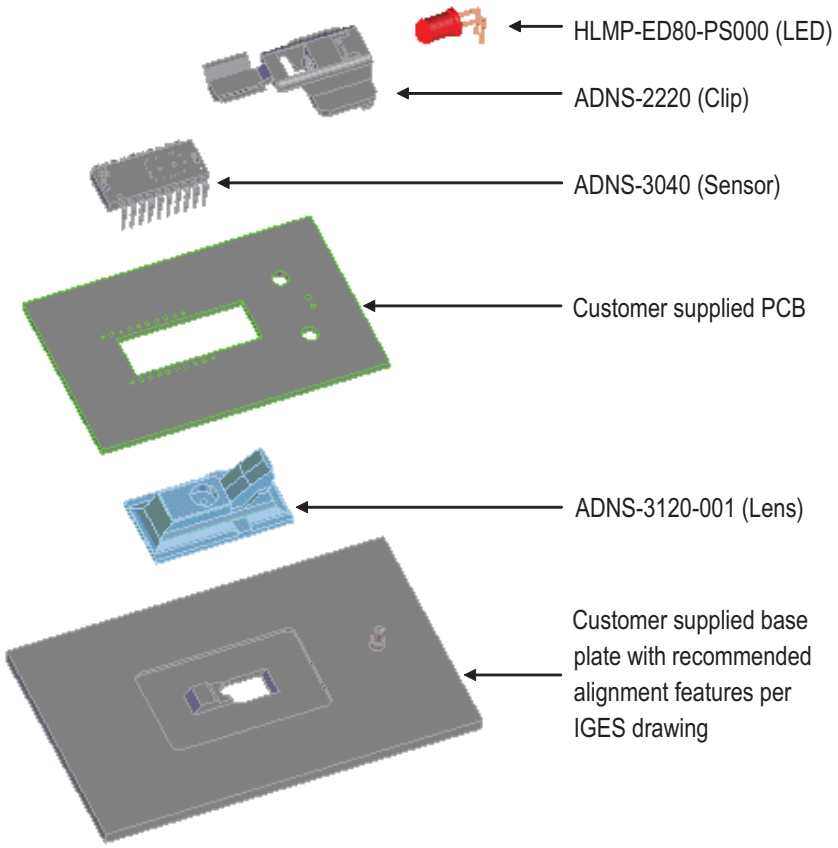


Figure 5. Exploded view

PCB Assembly Considerations

1. Insert the sensor and all other electrical components into PCB.
2. Insert the LED into the assembly clip and bend the leads 90 degrees.
3. Insert the LED/clip assembly into PCB.
4. Wave Solder the entire assembly in a no-wash solder process utilizing solder fixture. The solder fixture is needed to protect the sensor during the solder process. It also sets the correct sensor-to-PCB distance as the lead shoulders do not normally rest on the PCB surface. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
5. Place the lens onto the base plate.
6. Remove the protective kapton tape from optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture. Recommend not to place the PCB facing up during the entire mouse assembly process. Recommend to hold the PCB first vertically for the kapton removal process.
7. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The sensor aperture ring should self-align to the lens.
8. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
9. Install mouse top case. There **MUST** be a feature in the top case to press down onto the clip to ensure all components are interlocked to the correct vertical height.

Design considerations for improved ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the Avago Technologies supplied IGES file and ADNS-3120-001 lens.

Typical Distance	Millimeters
Creepage	16.0
Clearance	2.1

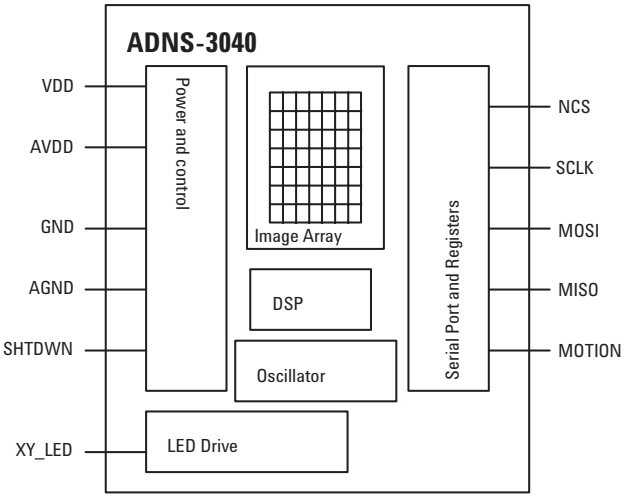


Figure 6. Block diagram of ADNS-3040 optical mouse sensor

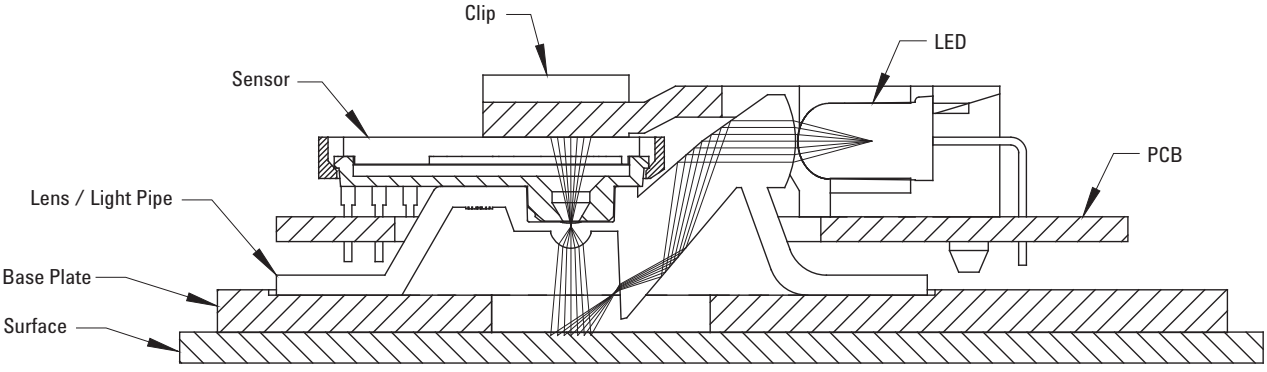
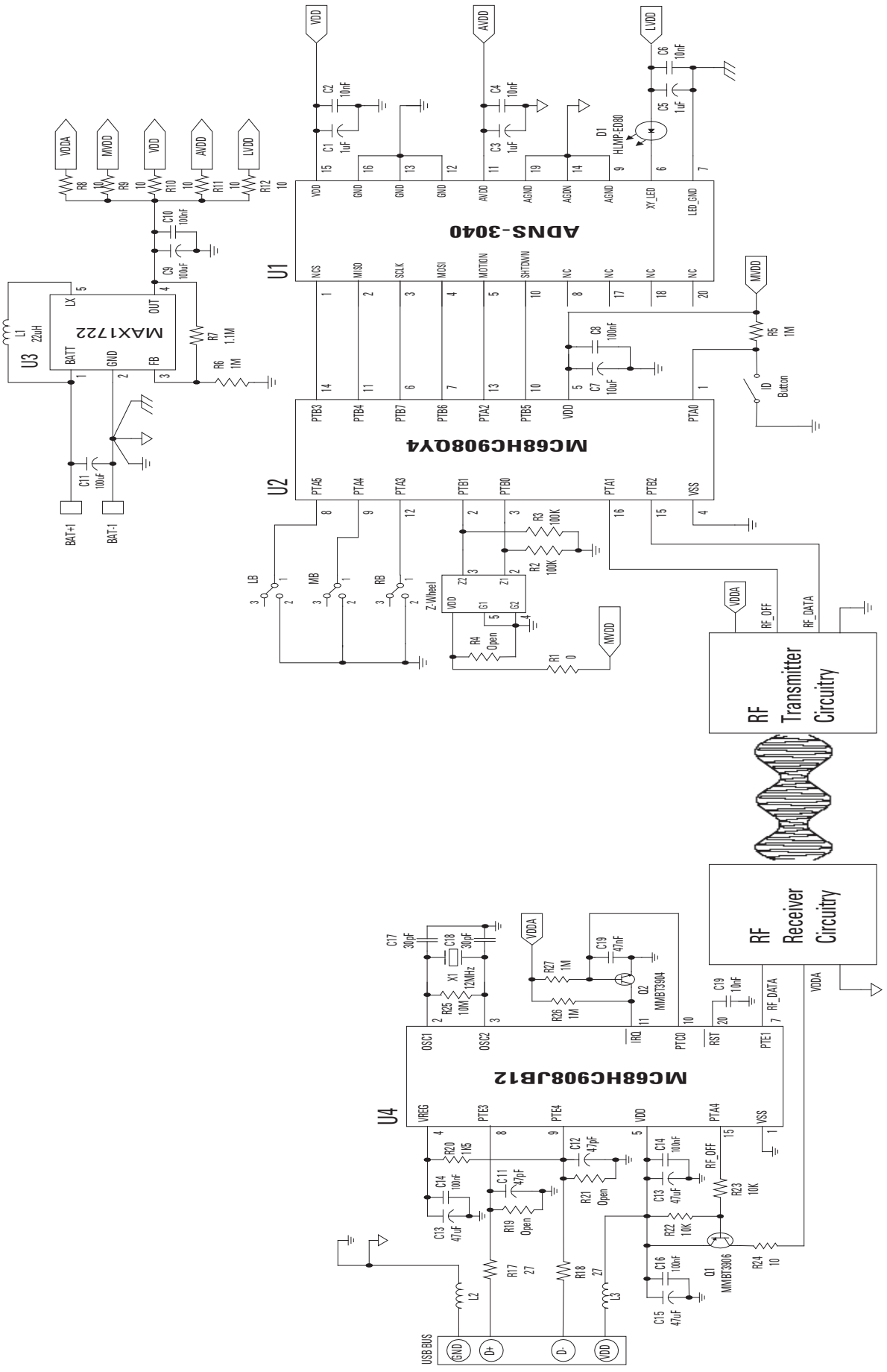


Figure 7. Sectional view of PCB assembly highlighting optical mouse components

Note
that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should **NOT** be used.



Notes The supply and ground paths should be laid out using a star topology.

Figure 8. Schematic Diagram for Interface between ADNS-3040 and microcontroller

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- UL flammability level UL94 V-0.
- Provides sufficient ESD creepage/clearance distance to avoid discharge up to 15kV when assembled into a mouse according to usage instructions above.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Lead Solder Temp			260	°C	For 10 seconds, 1.6mm below seating plane.
Supply Voltage	V_{DD}	-0.5	3.7	V	
ESD			2	kV	All pins, human body model MIL 883 Method 3015
Input Voltage	V_{IN}	-0.5	V_{DD}+0.5	V	All Pins
Latchup Current	I_{OUT}		20	mA	All Pins

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power supply voltage - for HLMP-ED80-PS000 LED *	V_{DD}	2.6		3.6	Volts	Including noise.
Power supply rise time	V_{RT}	0.001		100	ms	0 to 2.6V
Supply noise(Sinusoidal)	V_{NA}			100	mV p-p	10kHz-50MHz
Serial Port Clock Frequency	f_{SCLK}			1	MHz	Active drive, 50% duty cycle.
Distance from lens reference plane to surface	Z	2.45	2.55	2.65	mm	Results in 0.2 mm DOF, See drawing below
Speed	S			20	in/sec	
Acceleration	A			8	g	
Load Capacitance	C_{OUT}			100	pF	MOTION, MISO

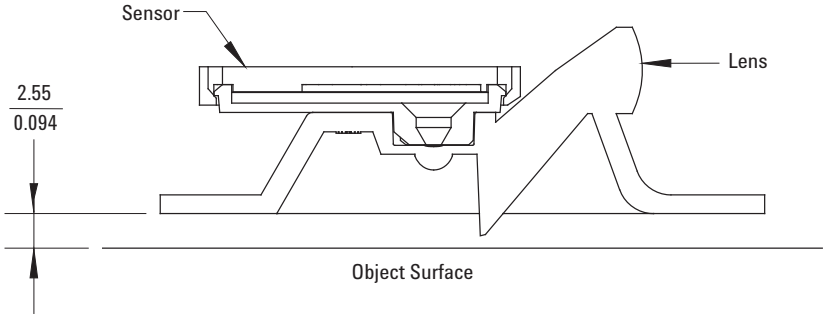


Figure 9. Distance from lens reference plane to surface

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V_{DD3}=2.6V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Motion delay after reset	$t_{MOT-RST}$			23	ms	From SW_RESET register write to valid motion, assuming motion is present
Shutdown	t_{STDWN}			50	ms	From STDWN pin active to low current
Wake from shutdown	t_{WAKEUP}	1			s	From STDWN pin inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown and Forced Rest", also note $t_{MOT-RST}$
Forced Rest enable	$t_{REST-EN}$			1	s	From RESTEN bits set to low current
Wake from Forced Rest	$t_{REST-DIS}$			1	s	From RESTEN bits cleared to valid motion
MISO rise time	t_{r-MISO}		150	300	ns	C_L = 100pF
MISO fall time	t_{f-MISO}		150	300	ns	C_L = 100pF
MISO delay after SCLK	$t_{DLY-MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO hold time	$t_{HOLD-MISO}$	0.5		$1/f_{SCLK}$	µs	Data held until next falling SCLK edge
MOSI hold time	$t_{HOLD-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI setup time	$t_{SETUP-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI time between write commands	t_{SWW}	30			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI time between write and read commands	t_{SWR}	20			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI time between read and subsequent commands	$t_{SRW}t_{SRR}$	500			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI read address-data delay	t_{SRAD}	4			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS inactive after motion burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK active	$t_{NCS-SCLK}$	120			ns	From NCS falling edge to first SCLK rising edge
SCLK to NCS inactive (for read operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS inactive (for write operation)	$t_{SCLK-NCS}$	20			us	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO high-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION rise time	$t_{r-MOTION}$		150	300	ns	C_L = 100pF
MOTION fall time	$t_{F-MOTION}$		150	300	ns	C_L = 100pF
SHTDWN pulse width	$t_{P-STDWN}$	1			s	
Transient Supply Current	I_{DDT}			45	mA	Max supply current during a V_{DD} ramp from 0 to 2.6V

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V_{DD}=2.6 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
DC Supply Current in various modes	I_{DD_RUN} I_{DD_REST1} I_{DD_REST2} I_{DD_REST3}		2.9 0.5 0.1 0.03	10 1.8 0.4 0.15	mA	Average current, including LED current. No load on MISO, MOTION.
Peak Supply Current				40	mA	Peak current in 100kHz bandwidth, including LED current.
Shutdown Supply Current	$I_{DDSTDWN}$		1	12	µA	SCLK, MOSI and NCS must be within 300mV of GND or V_{DD}. STDWN must be within 300mV of V_{DD}.
Input Low Voltage	V_{IL}			0.6	V	SCLK, MOSI, NCS, STDWN
Input High Voltage	V_{IH}	VDD - 0.6			V	SCLK, MOSI, NCS, STDWN
Input hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS, STDWN
Input leakage current	I_{leak}		±1	±10	µA	Vin=VDD-0.6V, SCLK, MOSI, NCS, STDWN
XY_LED Current	I_{LED}		13	25	mA	XY_LED pin voltage should be greater than 0.15V and less than 1.4V. XY_LED current is pulsed, so average value is much lower
Output Low Voltage	V_{OL}			0.7	V	I_{OUT}=1mA, MISO, MOTION
Output High Voltage	V_{OH}	VDD-0.7			V	I_{OUT}=-1mA, MISO, MOTION
Input Capacitance	C_{in}			10	pF	MOSI, NCS, SCLK, STDWN

Typical Performance Characteristics

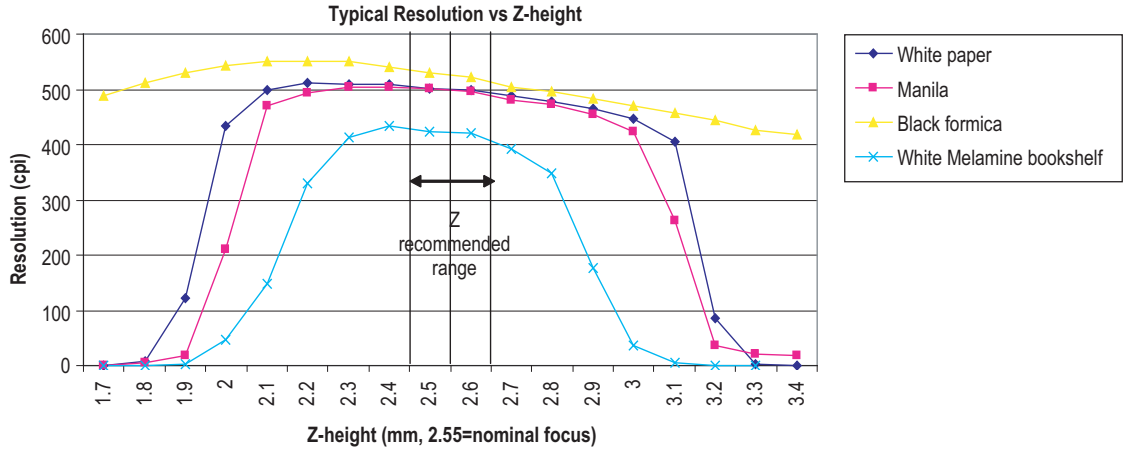


Figure 10. Mean Resolution vs. Z (White Paper).

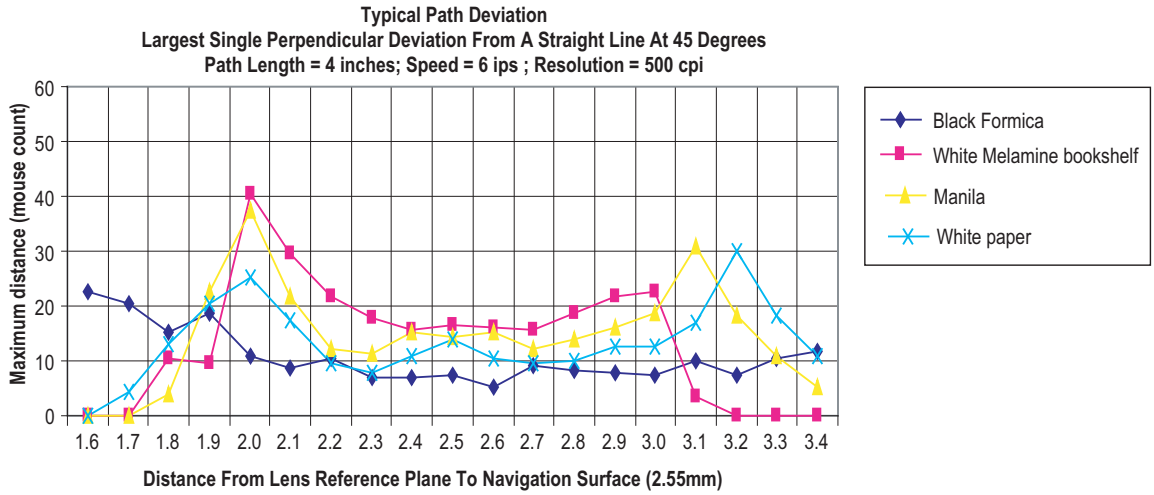


Figure 11. Average error vs. distance (mm)

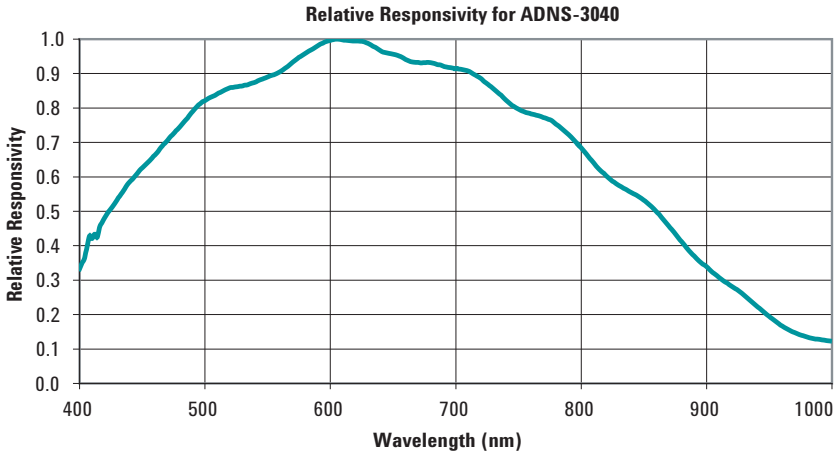


Figure 12. Relative Responsivity

Power management modes

The ADNS-3040 has three power-saving modes. Each mode has a different motion detection period, affecting response time to mouse motion (Response Time). The sensor automatically changes to the appropriate mode, depending on the time since the last reported motion (Downshift Time). The parameters of each mode are shown in the following table.

Motion Pin Timing

The motion pin is a level-sensitive output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is data in the Delta_X or Delta_Y registers. Clearing the motion bit (by reading Delta_Y and Delta_X, or writing to the Motion register) will put the motion pin high.

LED Mode

For power savings, the LED will not be continuously on. ADNS-3040 will flash the LED only when needed.

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-3040, and to read out the motion information.

The port is a four wire serial port. The host micro-controller always initiates communication; the ADNS-3040 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

Mode	Response Time (nominal)	Downshift Time (nominal)
Rest 1	16.5 ms	237 ms
Rest 2	82 ms	8.4 s
Rest 3	410 ms	504 s

The lines that comprise the SPI port:

SCLK:
Clock input. It is always generated by the master (the micro-controller).

MOSI:
Input data. (Master Out/Slave In)

MISO:
Output data. (Master In/Slave Out)

NCS:
Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to the ADNS-3040, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADNS-3040 reads MOSI on rising edges of SCLK.

Read Operation

A read operation, defined as data going from the ADNS-3040 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-3040 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

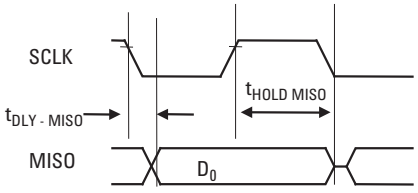


Figure 16. MISO Delay and Hold Time

NOTE:
The $0.5/f_{SCLK}$ minimum high state of SCLK is also the minimum MISO data hold time of the ADNS-3040. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-3040 will hold the state of data on MISO until the falling edge of SCLK.

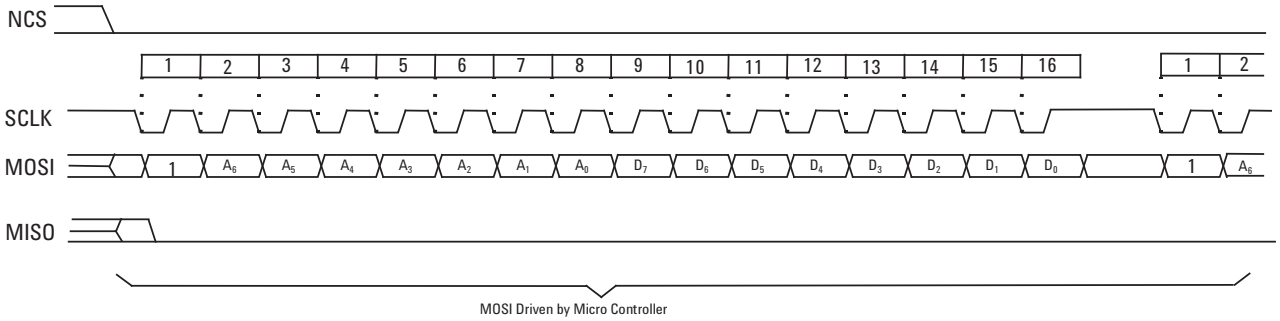


Figure 13. Write Operation

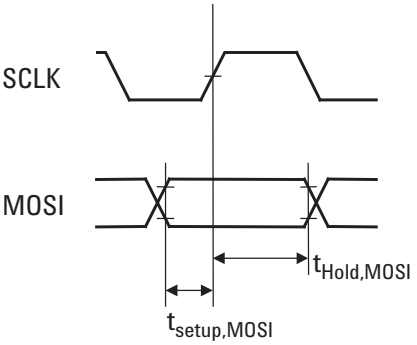


Figure 14. MOSI Setup and Hold Time

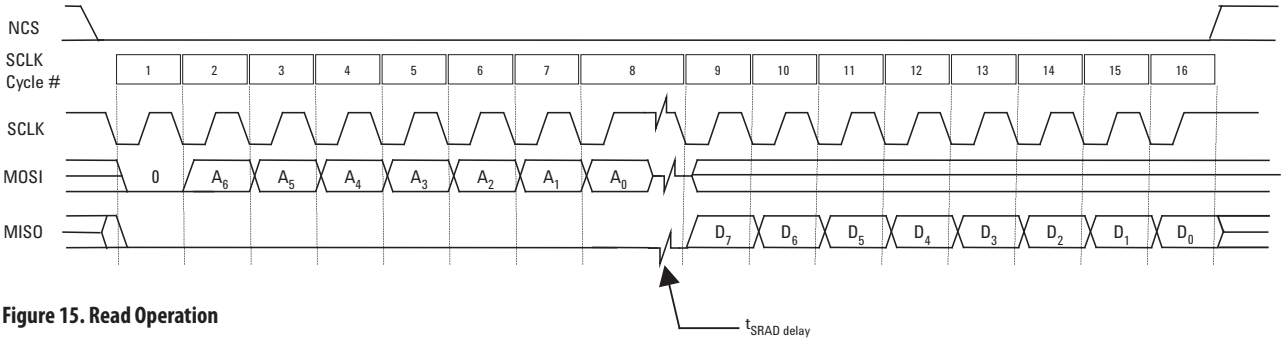


Figure 15. Read Operation

Required timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADNS-3040 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by reading the Motion_Burst register. The ADNS-3040 will respond with the contents of the Motion, Delta_Y, Delta_X, SQUAL, Shutter_Upper, Shutter_Lower and Maximum_Pixel registers in that order. The burst transaction can be terminated after the first 3 bytes of the sequence are read by bringing the NCS pin high. After sending the register address, the micro-controller must wait t_{SRAD} and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data is latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

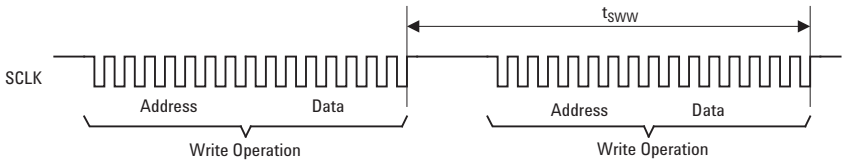


Figure 17. Timing between two write commands

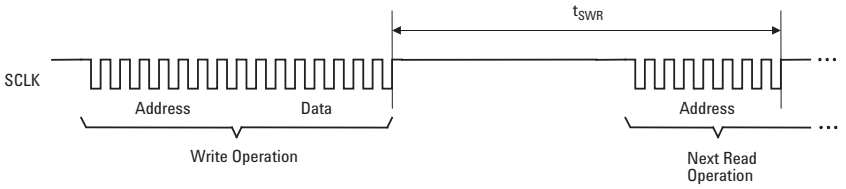


Figure 18. Timing between write and read commands

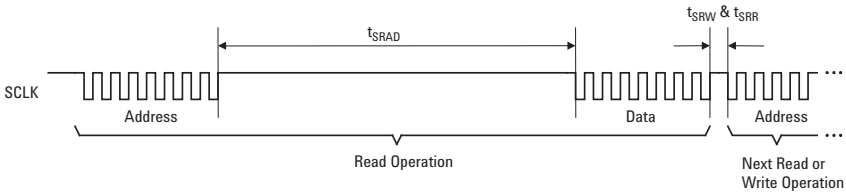


Figure 19. Timing between read and either write or subsequent read commands

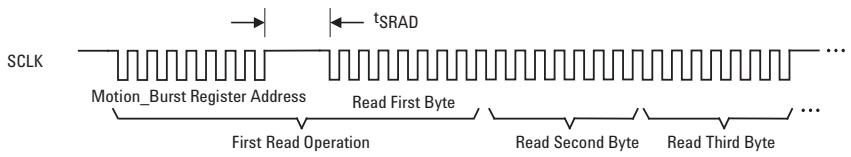


Figure 20. Motion Burst Timing

Notes on Power-up

The ADNS-3040 does not perform an internal power up self-reset; the POWER_UP_RESET register must be written every time power is applied. The appropriate sequence is as follows:

1. Apply power
2. Drive NCS high, then low to reset the SPI port
3. Write 0x5a to register 0x3a
4. Read from registers 0x02, 0x03 and 0x04 (or read these same 3 bytes from burst motion register 0x42) one time regardless the state of the motion pin.

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

State of Signal Pins After VDD is Valid

Pin	On Power-Up	NCS high before reset	NCS Low before reset	After Reset
NCS	functional	high	low	functional
MISO	undefined	undefined	functional	depends on NCS
SCLK	ignored	ignored	functional	depends on NCS
MOSI	ignored	ignored	functional	depends on NCS
XY_LED	undefined	undefined	undefined	functional
MOTION	undefined	undefined	undefined	functional
SHT-DWN	must be low	must below	must be low	functional

Notes on Shutdown and Forced Rest

The ADNS-3040 can be set to Rest mode through the Configuration_Bits register (0x11). This is to allow for further power savings in applications where the sensor does not need to operate all the time.

The ADNS-3040 can be set to Shutdown mode by asserting the SHTDWN pin. For proper operation, SHTDWN pulse width must be at least t_{STDWN}. Shorter pulse widths may cause the chip to enter an undefined state. In addition, the SPI port should not be accessed when SHTDWN is asserted. (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during shutdown. After deasserting SHTDWN, a full reset must be initiated. Wait t_{WAKEUP} before accessing the SPI port, then write 0x5A to the POWER_UP_RESET register. Any register settings must then be reloaded.

Pin	SHTDWN active
NCS	Functional*
MISO	Undefined
SCLK	Undefined
MOSI	Undefined
XY_LED	Low current
MOTION	Undefined

* NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It can be in either state if the sensor is the only device in addition to the microcontroller.

Note:
There are long wakeup times from shutdown and forced Rest. These features should not be used for power management during normal mouse motion.

Registers

The ADNS-3040 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	Product_ID	R	0x0D
0x01	Revision_ID	R	0x02
0x02	Motion	R/W	0x00
0x03	Delta_Y	R	Any
0x04	Delta_X	R	Any
0x05	SQUAL	R	Any
0x06	Shutter_Upper	R	Any
0x07	Shutter_Lower	R	Any
0x08	Maximum_Pixel	R	Any
0x09	Pixel_Sum	R	Any
0x0a	Minimum_Pixel	R	Any
0x0b	Pixel_Grab	R/W	Any
0x0c	CRC0	R	Any
0x0d	CRC1	R	Any
0x0e	CRC2	R	Any
0x0f	CRC3	R	Any
0x10	Self_Test	W	
0x11	Configuration_Bits	R/W	0x03
0x12-0x2d	Reserved		
0x2e	Observation	R/W	Any
0x2f-0x38	Reserved		
0x3a	POWER_UP_RESET	W	
0x3b-0x3d	Reserved		
0x3e	Inverse_Revision_ID	R	0xFD
0x3f	Inverse_Product_ID	R	0xF2
0x42	Motion_Burst	R	Any

Product ID **Address: 0x00**

Access: Read Reset Value: 0x0D

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: 8-Bit unsigned integer

USAGE: This register contains a unique identification assigned to the ADNS-3040. The value in this register does not change; it can be used to verify that the serial communications link is functional.

Revision ID **Address: 0x01**

Access: Read Reset Value: 0x02

Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Data Type: 8-Bit unsigned integer

USAGE: This register contains the IC revision. It is subject to change when new IC versions are released.

Motion **Address: 0x02**

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MOT	PIXRDY	PIXFIRST	OVF	Reserved	Reserved	Reserved	Reserved

Data Type: Bit field.

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, then the user should read registers 0x03 and 0x04 to get the accumulated motion. Read this register before reading the Delta_Y and Delta_X registers.

Writing anything to this register clears the MOT and OVF bits, Delta_Y and Delta_X registers. The written data byte is not saved.

Internal buffers can accumulate more than eight bits of motion for X or Y. If either one of the internal buffers overflows, then absolute path data is lost and the OVF bit is set. This bit is cleared once some motion has been read from the Delta_X and Delta_Y registers, and if the buffers are not at full scale. Since more data is present in the buffers, the cycle of reading the Motion, Delta_X and Delta_Y registers should be repeated until the motion bit (MOT) is cleared. Until MOT is cleared, either the Delta_X or Delta_Y registers will read either positive or negative full scale. If the motion register has not been read for long time, at 400 cpi it may take up to 16 read cycles to clear the buffers, at 800 cpi, up to 32 cycles. To clear an overflow, write anything to this register.

The PIXRDY bit will be set whenever a valid pixel data byte is available in the Pixel_Dump register. Check that this bit is set before reading from Pixel_Dump. To ensure that the Pixel_Grab pointer has been reset to pixel 0,0 on the initial write to Pixel_Grab, check to see if PIXFIRST is set to high.

Field Name	Description
MOT	Motion since last report **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers
PIXRDY	Pixel Dump data byte is available in Pixel_Dump register **0 = data not available** 1 = data available
PIXFIRST	This bit is set when the Pixel_Grab register is written to or when the complete pixel array has been read, initiating an increment to pixel 0,0. **0 = Pixel_Grab data not from pixel 0,0** 1 = Pixel_Grab data is from pixel 0,0
OVF	Motion overflow, ΔY and/or ΔX buffer has overflowed since last report **0 = no overflow** 1 = Overflow has occurred

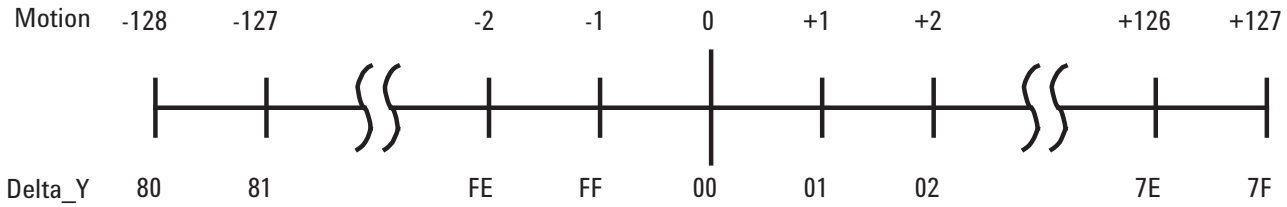
Delta Y **Address: 0x03**

access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number.

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



NOTES: Avago Technologies RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

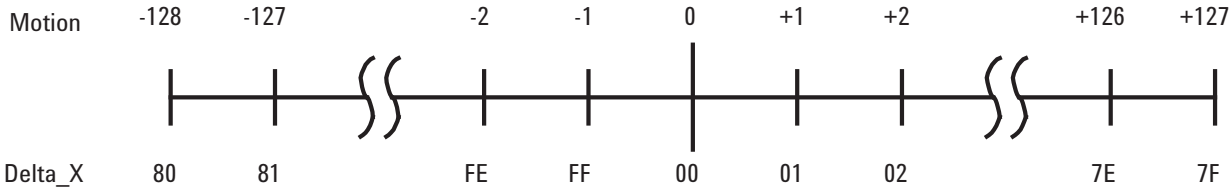
Delta X **Address: 0x04**

Access: Read Reset Values: Undefined

Bit	7	6	5	4	3	2	1	0
	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type: Eight bit 2's complement number.

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



NOTES: Avago Technologies RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

SQUAL **Address: 0x05**

Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type: Upper 8 bits of a 9-bit unsigned integer.

USAGE: SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame.

The maximum SQUAL register value is 167. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 500 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor. SQUAL is typically maximized when the navigation surface is at the optimum distance from the imaging lens (the nominal Z-height).

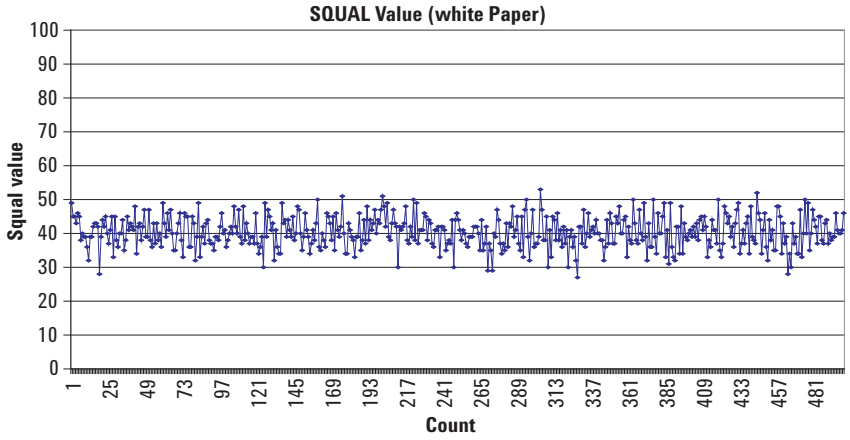


Figure 21. SQUAL values (white paper)

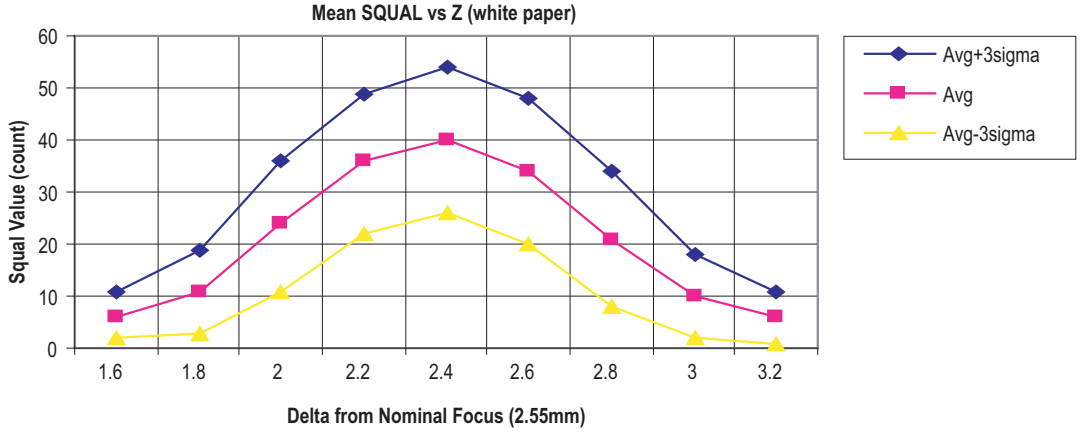


Figure 22. Mean SQUAL vs. Z (white paper)

Shutter_Upper **Address: 0x06**

Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Shutter_Lower **Address: 0x07**

Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Data Type: Sixteen bit unsigned integer.

USAGE: Units are clock cycles. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

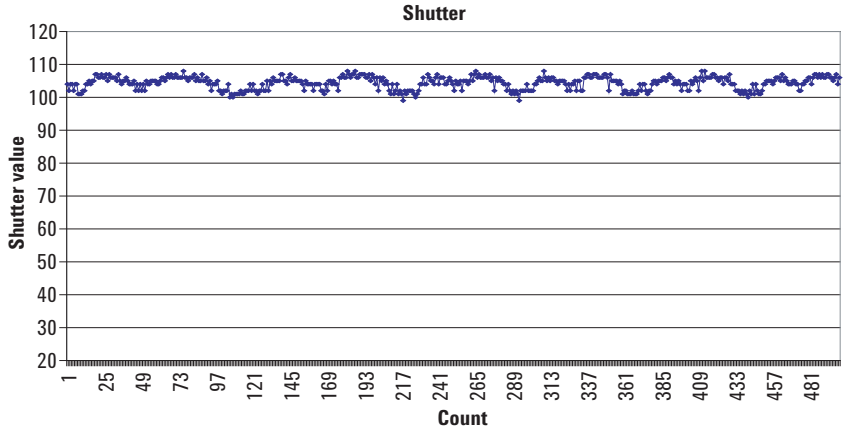


figure 23. Shutter values (white paper)

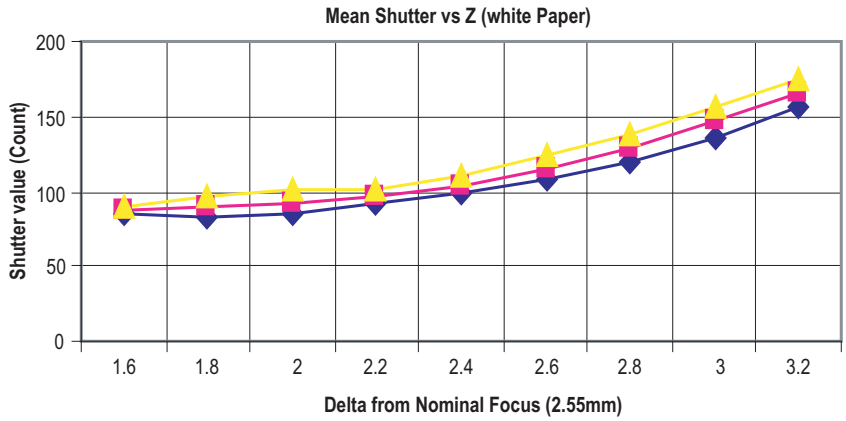


Figure 24. Mea n Shutter vs. Z (white paper)

Maximum Pixel **address: 0x08**

Access: Read Reset Value: Underfined

Bit	7	6	5	4	3	2	1	0
	MP_7	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Eight-bit number.

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 254. The maximum pixel value can vary with every frame.

Pixel_Sum **Address: 0x09**

Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	AP_7	AP_6	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0

Data Type: High 8 bits of an unsigned 17-bit integer.

USAGE: This register is used to find the average pixel value. It reports the seven bits of a 16-bit counter, which sums all pixels in the current frame. It may be described as the full sum divided by 512. To find the average pixel value, use the following formula:

Average Pixel = Register Value * 128/121 = Register Value * 1.06

The maximum register value is 240. The minimum is 0. The pixel sum value can change on every frame.

Minimum_Pixel **Address: 0x0a**

Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	MP_7	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Eight-bit number.

USAGE: Minimum Pixel value in current frame. Minimum value = 0, maximum value = 254. The minimum pixel value can vary with every frame.

Pixel_Grab **Address: 0x0b**

Access: Read/Write Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	PD_7	PD_6	PD_5	PD_4	PD_3	PD_2	PD_1	PD_0

Data Type: Eight-bit word.

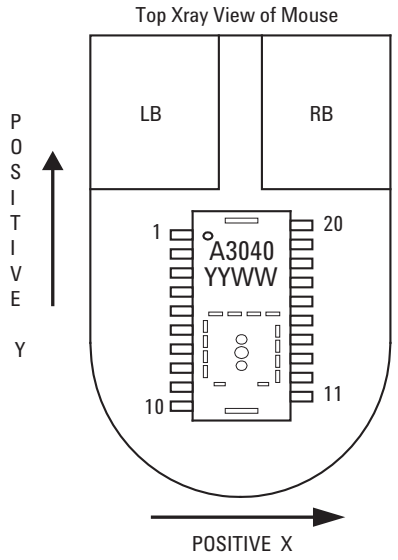
USAGE: For test purposes, the sensor will read out the contents of the pixel array, one pixel per frame. To start a pixel grab, write anything to this register to reset the pointer to pixel 0,0. Then read the PIXRDY bit in the Motion register. When the PIXRDY bit is set, there is valid data in this register to read out. After the data in this register is read, the pointer will automatically increment to the next pixel. Reading may continue indefinitely; once a complete frame's worth of pixels has been read, PIXFIRST will be set to high to indicate the start of the first pixel and the address pointer will start at the beginning location again.

Pixel Address Map (Looking through the ADNS-3120-001 Lens)

First Pixel

0	22	44	66	88	110	132	154	176	198	220	242	264	286	308	330	352	374	396	418	440	462
1	23	45	67	89	111	133	155	177	199	221	243	265	287	309	331	353	375	397	419	441	463
2	24	46	68	90	112	134	156	178	200	222	244	266	288	310	332	354	376	398	420	442	464
3	25	47	69	91	113	135	157	179	201	223	245	267	289	311	333	355	377	399	421	443	465
4	26	48	70	92	114	136	158	180	202	224	246	268	290	312	334	356	378	400	422	444	466
5	27	49	71	93	115	137	159	181	203	225	247	269	291	313	335	357	379	401	423	445	467
6	28	50	72	94	116	138	160	182	204	226	248	270	292	314	336	358	380	402	424	446	468
7	29	51	73	95	117	139	161	183	205	227	249	271	293	315	337	359	381	403	425	447	469
8	30	52	74	96	118	140	162	184	206	228	250	272	294	316	338	360	382	404	426	448	470
9	31	53	75	97	119	141	163	185	207	229	251	273	295	317	339	361	383	405	427	449	471
10	32	54	76	98	120	142	164	186	208	230	252	274	296	318	340	362	384	406	428	450	472
11	33	55	77	99	121	143	165	187	209	231	253	275	297	319	341	363	385	407	429	451	473
12	34	56	78	100	122	144	166	188	210	232	254	276	298	320	342	364	386	408	430	452	474
13	35	57	79	101	123	145	167	189	211	233	255	277	299	321	343	365	387	409	431	453	475
14	36	58	80	102	124	146	168	190	212	234	256	278	300	322	344	366	388	410	432	454	476
15	37	59	81	103	125	147	169	191	213	235	257	279	301	323	345	367	389	411	433	455	477
16	38	60	82	104	126	148	170	192	214	236	258	280	302	324	346	368	390	412	434	456	478
17	39	61	83	105	127	149	171	193	215	237	259	281	303	325	347	369	391	413	435	457	479
18	40	62	84	106	128	150	172	194	216	238	260	282	304	326	348	370	392	414	436	458	480
19	41	63	85	107	129	151	173	195	217	239	261	283	305	327	349	371	393	415	437	459	481
20	42	64	86	108	130	152	174	196	218	240	262	284	306	328	350	372	394	416	438	460	482
21	43	65	87	109	131	153	175	197	219	241	263	285	307	329	351	373	395	417	439	461	483

Last Pixel



CRC0 **Address: 0x0c**

Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	$CRC0_7$	$CRC0_6$	$CRC0_5$	$CRC0_4$	$CRC0_3$	$CRC0_2$	$CRC0_1$	$CRC0_0$

Data Type: Eight-bit number

USAGE: Register 0x0c reports the first byte of the system self test results. Value = 0xAF. See Self Test register 0x10.

CRC1 **Address: 0x0d**

Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	$CRC1_7$	$CRC1_6$	$CRC1_5$	$CRC1_4$	$CRC1_3$	$CRC1_2$	$CRC1_1$	$CRC1_0$

Data Type: Eight bit number

USAGE: Register 0x0c reports the second byte of the system self test results. Value = 0x4E. See Self Test register 0x10.

CRC2 **Address: 0x0e**

Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	$CRC2_7$	$CRC2_6$	$CRC2_5$	$CRC2_4$	$CRC2_3$	$CRC2_2$	$CRC2_1$	$CRC2_0$

Data Type: Eight-bit number

USAGE: Register 0x0e reports the third byte of the system self test results. Value = 0x31. See Self Test register 0x10.

CRC3 **Address: 0x0f**

Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	$CRC3_7$	$CRC3_6$	$CRC3_5$	$CRC3_4$	$CRC3_3$	$CRC3_2$	$CRC3_1$	$CRC3_0$

Data Type: Eight-bit number

USAGE: Register 0x0f reports the fourth byte of the system self test results. Value = 0x22. See Self Test register 0x10.

Self_Test **Address: 0x10**

Access: Write Reset Value: NA

Bit	7	6	5	4	3	2	1	0
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TESTEN

Data Type: Bit field

USAGE: Set the TESTEN bit in register 0x10 to start the system self-test. The test takes 250ms. During this time, do not write or read through the SPI port. Results are available in the CRC0-3 registers. After self-test, reset the chip to start normal operation.

Field Name	Description
TESTEN	Enable System Self Test **0 = Disable** 1 = Enable

Configuration_bits **Address: 0x11**

Access: Read/Write Reset Value: 0x03

Bit	7	6	5	4	3	2	1	0
	RES	Reserved	$RESTEN_1$	$RESTEN_0$	Reserved	Reserved	Reserved	Reserved

Data Type: Bit field

USAGE: Register 0x11 allows the user to change the configuration of the sensor. Setting the RESTEN bit forces the sensor into Rest mode, as described in the power modes section above. The RES bit allows selection between 400 and 800 cpi resolution.

Note: Forced Rest has a long wakeup time and should not be used for power management during normal mouse motion.

Field Name	Description
$RESTEN_{1-0}$	Puts chip into Rest mode **00 = normal operation** 01 = force Rest1 10 = force Rest2 11 = force Rest3
RES	Sets resolution **0 = 400** 1 = 800

Reserved **Address: 0x12-0x2d**

Observation **Address: 0x2e**

Access: Read/Write Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	$MODE_1$	$MODE_0$	Reserved	Reserved	OBS_3	OBS_2	OBS_1	OBS_0

Data Type: Bit field

USAGE: Register 0x2e provides bits that are set every frame. It can be used during EFTB testing to check that the chip is running correctly. Writing anything to this register will clear the bits.

Field Name	Description
$MODE_{1-0}$	Mode Status: Reports which mode the sensor is in. 00 = Run 01 = Rest1 10 = Rest2 11 = Rest3
OBS_{3-0}	Set every frame

Reserved **Address: 0x2f-0x39**

POWER_UP_RESET **Address: 0x3a**

Access: Write Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
	RST_7	RST_6	RST_5	RST_4	RST_3	RST_2	RST_1	RST_0

Data Type: 8-bit integer

USAGE: Write 0x5A to this register to reset the chip. All settings will revert to default values.

Inverse_Revision_ID **Address: 0x3e**

Access: Read Reset Value: 0xFD

Bit	7	6	5	4	3	2	1	0
	$NRID_7$	$NRID_6$	$NRID_5$	$NRID_4$	$NRID_3$	$NRID_2$	$NRID_1$	$NRID_0$

Data Type: Inverse 8-Bit unsigned integer

USAGE: This value is the inverse of the Revision_ID. It can be used to test the SPI port.

Inverse_Product_ID **Address: 0x3f**

Access: Read Reset Value: 0xF2

Bit	7	6	5	4	3	2	1	0
	$NPID_7$	$NPID_6$	$NPID_5$	$NPID_4$	$NPID_3$	$NPID_2$	$NPID_1$	$NPID_0$

Data Type: Inverse 8-Bit unsigned integer

USAGE: This value is the inverse of the Product_ID. It can be used to test the SPI port.

Motion_Burst **Address: 0x42**

Access: Read Reset Value: Any

Bit	7	6	5	4	3	2	1	0
	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0

Data Type: Various.

USAGE: Read from this register to activate burst mode. The sensor will return the data in the Motion register, Delta_Y, Delta_X, Squal, Shutter_Upper, Shutter_Lower, and Maximum_Pixel. A minimum of 3 bytes should be read during a burst read. Reading the first 3 bytes clears the motion data.

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