LM10520 Single-Phase Buck Controller for AVS Systems

Check for Samples: LM10520

FEATURES

- **Typical Power Savings with AVS: 20 to 50%**
- **PWI 2.0 Interface**
- **7-Bit AVS Control for One Output (Typical Range of 0.6V to 1.2V)**
- **Precision Enable**
- **Integrated, Non-Overlapping NFET Drivers**
- **Switching Frequency Over 50 kHz to 1MHz**
- **Switching Frequency Synchronize Range from 250 kHz to 1MHz**
- **Startup into Pre-Biased Output**
- **Power Stage Input from 1V to 14V**
- **Control stage Input from 3V to 6V**
- **Power Good Flag and Shutdown**
- **Output Over-Voltage and Under-Voltage Detection**
- **Low-Side Adjustable Current Sensing**
- **Adjustable Soft Start**
- **Tracking and Sequencing with Shutdown and Soft-Start Pins**
- **TSSOP-28 Package**

APPLICATIONS

- **AVS-Enabled FPGAs**
- **AVS-Enabled ASICs**

DESCRIPTION

The LM10520 is a single-phase Energy Management Unit (EMU) that actively reduces system-level power consumption by utilizing a continuous, real-time, closed-loop Adaptive Voltage Scaling (AVS) scheme. The AVS technology enables optimum energy management delivery to the load in order to maximize system-level energy savings.

The LM10520 operates cooperatively with PowerWise™ AVS-compatible ASICs, SoCs, and processors to optimize supply voltages adaptively over process and temperature variations. The device is controlled via the high-speed serial PWI 2.0 open-standard interface. It also supports Dynamic Voltage Scaling (DVS) using frequency-voltage pairs from pre-characterized lookup tables.

The LM10520 features a fixed-frequency voltage-mode PWM control architecture which is adjustable from 50 kHz to 1MHz with one external resistor. In addition, the LM10520 allows the switching frequency to be synchronized to an external clock signal over the range of 250 kHz to 1MHz. This wide range of switching frequency gives the power supply designer the flexibility to make better tradeoffs between component size, cost and efficiency.

Features include the ability to startup with a pre-biased load on the output, soft-start, input under-voltage lockout (UVLO) and Power good (based on both under-voltage and over-voltage detection). In addition, the soft-start pin can be used for implementing precise tracking, for the purpose of sequencing with respect to an external rail.

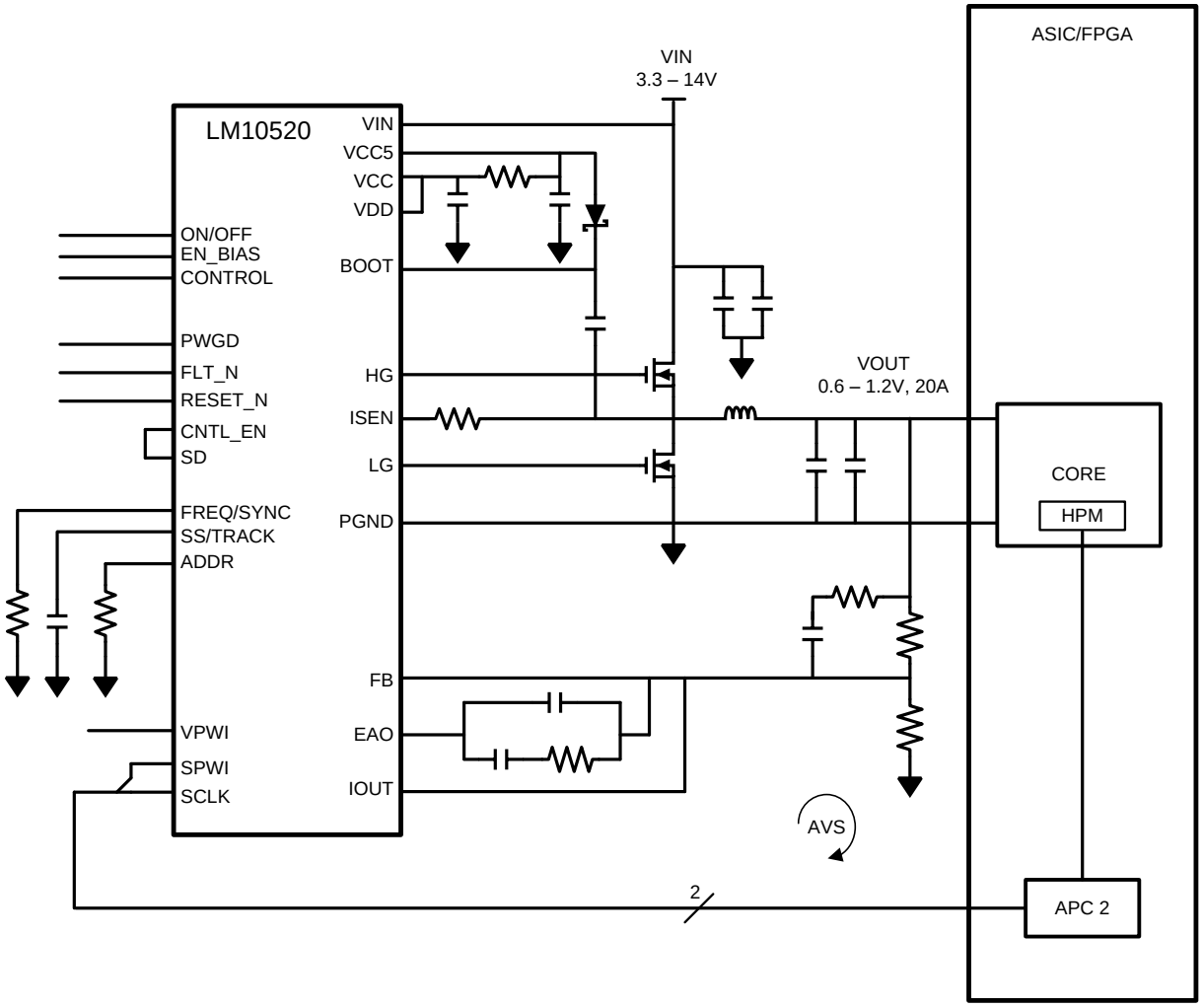
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Typical Application Circuit



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Connection Diagram

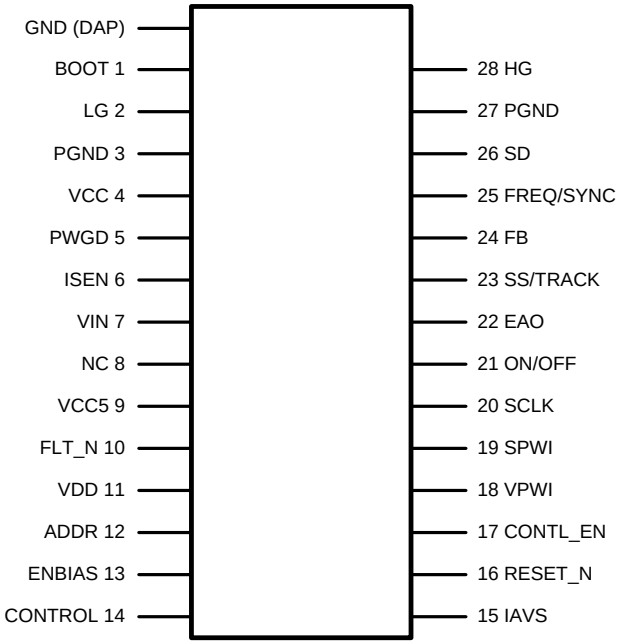


Figure 1. 28-Lead Plastic TSSOP
Package Number PW0028A

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PIN DESCRIPTIONS

Number	Pad Name	Type	Pad Description
	DAP	GND	Connect Die Attach Pad to ground
1	BOOT	Analog	Boot cap voltage. Connect boot capacitor to this pin.
2	LG	Output	Low Side MOSFET gate drive.
3	PGND	GND	Power ground.
4	VCC	Power	5V bias input
5	PWGD	GND	Power good signal
6	ISEN	Analog	Current limit sense
7	VIN	Power	High voltage bias input
8	NC		No Connect
9	VCC5	Power	5V bias output
10	FLT_N	I/O	External fault input, active low. Causes output to be disabled and resets R0 (output voltage register)
11	VDD	Power	Digital circuitry bias
12	ADDR	Analog	Connect a resistor from this to ground to set the PWI address
13	ENBIAS	Input	Enable for digital circuitry
14	CONTROL	Input	Enable for output voltage
15	IOUT1	Analog	Connect this pin the FB pin
16	RESET_N	Input	Digital circuitry reset, active low
17	CNTL_EN	Output	Digital circuitry output which control Vout enable/disable
18	VPWI	Power	PWI I/O bias input
19	SPWI	I/O	PWI signal
20	SCLK	Output	PWI clock
21	ON/OFF	Input	Enable for internal 5V LDO
22	EAO	Analog	Error amp output
23	SS/TRACK	Analog	Connecting a capacitor to ground will set the softstart time. Optionally, if this pin is driven externally the output will track the voltage at this pin
24	FB		Feedback connection
25	FREQ/SYNC	Analog	Connecting a resistor from this pin to ground will set the switching frequency. Alternatively, a clock source can drive this pin, and the LM10520 will synchronize to the clock frequency.
26	SD	Input	Shutdown for the analog circuitry
27	PGND	GND	Power ground
28	HG	Analog	High side MOSFET drive

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

ON/OFF, VIN		-0.3V to 16V
VCC		-0.3V to 6V
LG, PGND, SGND, PWGD, HG, SD, FB, SS/TRACK, EAO, FREQ/SYNC		-0.3V to VCC + 0.3V
BOOT		-0.3V to 18V
ISEN		-0.3V to 14V
VPWI		-0.2V to VDD
SPWI, SCLK		-0.2 to VPWI
All other pins		-0.2V to 6V
Junction Temperature		150°C
Storage Temperature		-45°C to 150°C
ESD Tolerance (3)	Human Body Model	1.5 kV
Soldering Information See product folder at www.ti.com and literature number SNOA549		

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device operates correctly. Operating Ratings do not imply ensured performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) ESD using the human body model which is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

OPERATING RATINGS

VIN	3.5V to 16V
VCC, VDD	3V to 5.5V
VPWI(1)	1.6V to 3.6V
BOOT Voltage	1V to 17V
Junction Temperature	-40°C to 125°C

(1) Note: VPWI cannot be higher than VDD

THERMAL PROPERTIES

Junction-to-Ambient Thermal Resistance	26°C/W

ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V unless otherwise indicated. Typicals and limits appearing in plain type apply for T_A= T_J= 25°C. Limits appearing in boldface type apply over full Operating Temperature Range. Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	FB Pin Voltage	V_{CC} = 3V to 6V	**0.591**	0.6	**0.609**	V
V_{ON}	UVLO Thresholds	V_{CC} Rising V_{CC} Falling		2.79 2.42		V
I_Q	Operating V_{CC}/V_{DD} Current	V_{CC} = 3.3V, V_{SD} = 3.3V f_{SW} = 600 kHz, V_{CC} connected to V_{DD}		2.15	**2.71**	mA
		V_{CC} = V_{DD} = 5V, V_{SD} = 5V f_{SW} = 600 kHz		2.315	**3.01**	
	Shutdown V_{CC}/V_{DD} Current	V_{CC} = V_{DD} = 3.3V, V_{SD} = EN_BIAS= 0V		2.5	**13**	µA
	Shutdown VIN Current	ON/OFF = 0V		0.05	**2**	
t_{PWGD1}	PWGD Pin Response Time	V_{FB} Rising		10		µs
t_{PWGD2}	PWGD Pin Response Time	V_{FB} Falling		10		µs
I_{SS-ON}	SS Pin Source Current	V_{SS} = 0V	**7**	10	**14**	µA

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.3V unless otherwise indicated. Typicals and limits appearing in plain type apply for T_A= T_J= 25°C. Limits appearing in boldface type apply over full Operating Temperature Range. Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{SS-OC}	SS Pin Sink Current During Over Current	V_{SS} = 2.0V		90		µA
I_{SEN-TH}	I_{SEN} Pin Source Current Trip Point		**25**	40	**55**	µA
I_{FB}	FB Pin Current	Sourcing		20		nA
I_{ADDR}	Address pin source current			7.8		µA
IAVS						
LSB	DAC Step size	$I_{DAC-MAX}$ / 2^n (1 ≤ n ≤ 7)		470		nA
	Resolution		7			Bits
FS	Full Scale			56.69		µA
INL	Integral Non-Linearity		−2		2	LSB
DNL	Differential Non-Linearity		−0.5		0.5	
ZE	Zero Code Error/Offset Error			57		nA
ERROR AMPLIFIER						
GBW	Error Amplifier Unity Gain Bandwidth			9		MHz
G	Error Amplifier DC Gain			118		dB
SR	Error Amplifier Slew Rate			2		V/µs
I_{EAO}	EAO Pin Current Sourcing and Sinking Capability			14 16		mA
V_{EAO}	Error Amplifier Output Voltage	Minimum		1		V
		Maximum		2.2		V
GATE DRIVE						
I_{Q-BOOT}	BOOT Pin Quiescent Current	V_{BOOT} = 12V, V_{SD} = 0		18	**90**	µA
R_{HG_UP}	High-Side MOSFET Driver Pull-Up ON resistance	V_{BOOT} = 5V @ 350 mA Sourcing		2.7		Ω
R_{HG_DN}	High-Side MOSFET Driver Pull-Down ON resistance	350 mA Sinking		0.8		Ω
R_{LG_UP}	Low-Side MOSFET Driver Pull-Up ON resistance	V_{BOOT} = 5V @ 350 mA Sourcing		2.7		Ω
R_{LG_DN}	Low-Side MOSFET Driver Pull-Down ON resistance	350 mA Sinking		0.8		Ω
OSCILLATOR						
f_{SW}	PWM Frequency	R_{FADJ} = 750 kΩ		50		kHz
		R_{FADJ} = 100 kΩ		300		
		R_{FADJ} = 42.2 kΩ	**475**	600	**725**	
		R_{FADJ} = 18.7 kΩ		1000		
	LM10520 External Synchronizing Signal Frequency	Voltage Swing = 0V to V_{CC}	250		1000	
$SYNC_L$	LM10520 Synchronization Signal Low Threshold	f_{SW} = 250 kHz to 1 MHz			1	V
$SYNC_H$	LM10520 Synchronization Signal High Threshold	f_{SW} = 250 kHz to 1 MHz	2			V
D_{MAX}	Max High-Side Duty Cycle	f_{SW} = 300 kHz f_{SW} = 600 kHz f_{SW} = 1 MHz		86 78 67		%

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.3V unless otherwise indicated. Typicals and limits appearing in plain type apply for T_A= T_J= 25°C. Limits appearing in boldface type apply over full Operating Temperature Range. Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LOGIC AND CONTROL INPUTS						
EN_BIAS_{TH}	Precision enable threshold	Rising		1.32	**1.4**	V
		Falling	**1.09**	1.19		
I_{IL}	Input Current Low	FLT_N, RESET_N	**−10**			µA
		ENBIAS, CONTROL	**−1**			
		SPWI, SCLK	**−1**			
I_{IH}	Input Current High	FLT_N, RESET_N			**1**	µA
		ENBIAS, CONTROL			**10**	
		SPWI, SCLK			**5**	
V_{IL}	Input Low Voltage	CONTROL, FLT_N, RESET_N			**0.5**	V
V_{IH}	Input High Voltage	CONTROL, FLT_N, RESET_N	**1.1**			
$V_{IL\ PWI}$	Input Low Voltage, PWI	SPWI, SCLK, 1.5 < VPWI < 3.3			**30**	% of VPWI
$V_{IH\ PWI}$	Input High Voltage, PWI	SPWI, SCLK, 1.5 < VPWI < 3.3	**70**			
f_{SCLK}	PWI2 SCLK	**DC useful for testing/debug	0		15M	Hz
$V_{STBY-IH}$	Standby High Trip Point	V_{FB} = 0.575V, V_{BOOT} = 3.3V V_{SD} Rising			**1.1**	V
$V_{STBY-IL}$	Standby Low Trip Point	V_{FB} = 0.575V, V_{BOOT} = 3.3V V_{SD} Falling	**0.232**			V
V_{SD-IH}	$\overline{SD}$ Pin Logic High Trip Point	V_{SD} Rising			**1.3**	V
V_{SD-IL}	$\overline{SD}$ Pin Logic Low Trip Point	V_{SD} Falling	**0.8**			V
LOGIC AND CONTROL OUTPUTS						
V_{OL}	Output Low Level	CNTL_EN, I_{SINK} ≤ 1mA			0.4	V
V_{OH}	Output High Level	CNTL_EN, I_{SINK} ≤ 1mA	VDD - 0.4			
$V_{OH\ PWI}$	Output High Level, PWI	SPWI, I_{SOURCE} ≤ 1mA	VPWI - 0.4			
$V_{PWGD-TH-LO}$	PWGD Pin Trip Points	V_{FB} Falling	**0.408**	0.434	**0.457**	V
$V_{PWGD-TH-HI}$	PWGD Pin Trip Points	V_{FB} Rising	**0.677**	0.710	**0.742**	V
$V_{PWGD-HYS}$	PWGD Hysteresis	V_{FB} Falling V_{FB} Rising		60 90		mV

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TYPICAL PERFORMANCE CHARACTERISTICS

Internal Reference Voltage vs Temperature

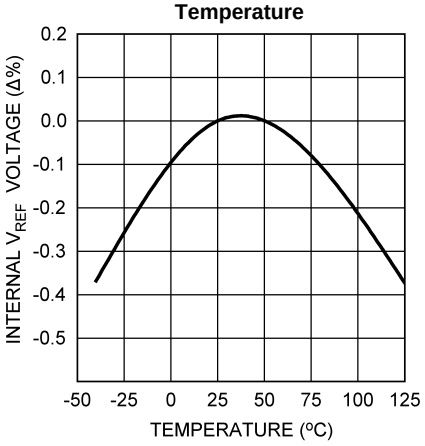


Figure 2.

Frequency vs Temperature

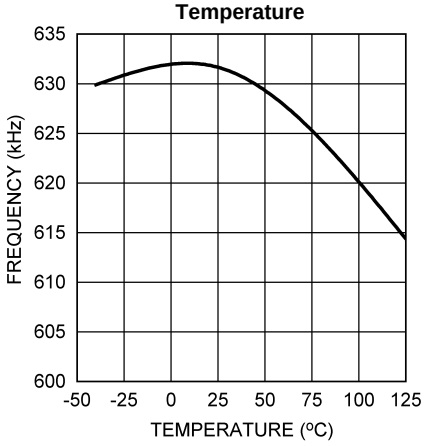


Figure 3.

Output Voltage vs Output Current

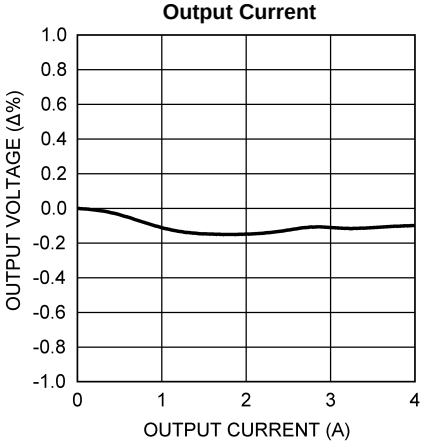


Figure 4.

Switch Waveforms
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 3A, C_{SS} = 12 nF, f_{SW} = 1MHz

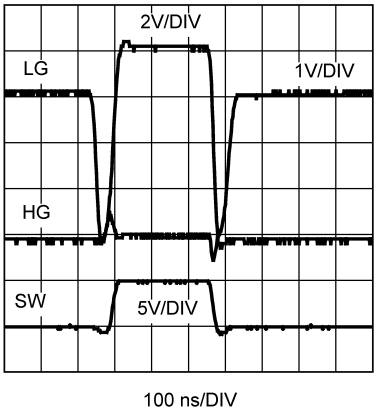


Figure 5.

Start-Up (Full-Load)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 3A, C_{SS} = 12 nF, f_{SW} = 1MHz

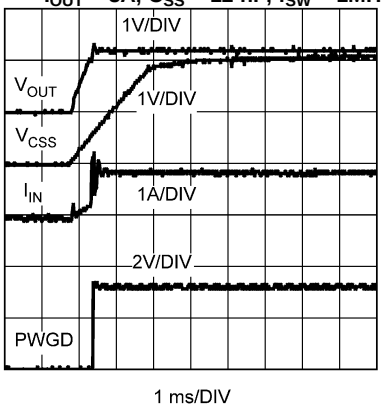


Figure 6.

Start-Up (No-Load)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
C_{SS} = 12 nF, f_{SW} = 1MHz

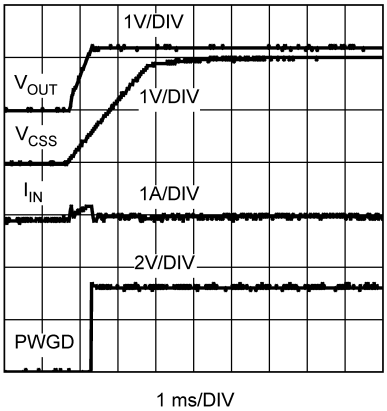


Figure 7.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Shutdown (Full-Load)
V_{CC} = 3.3V, V_{IN} = 5V, V_{OUT} = 1.2V
I_{OUT} = 3A, C_{SS} = 12 nF, f_{SW} = 1MHz

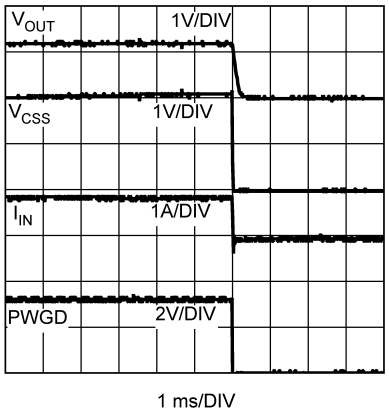


Figure 8.

Load Transient Response
PVIN = 12V, AVIN = 4.5V,
V_{OUT} = 1.2V, FSW = 300 kHz

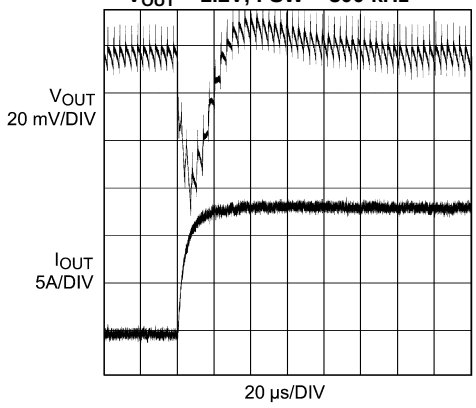


Figure 9.

Line Transient Response (V_{IN} = 3V to 9V)
V_{CC} = 3.3V, V_{OUT} = 1.2V
I_{OUT} = 2A, f_{SW} = 1 MHz

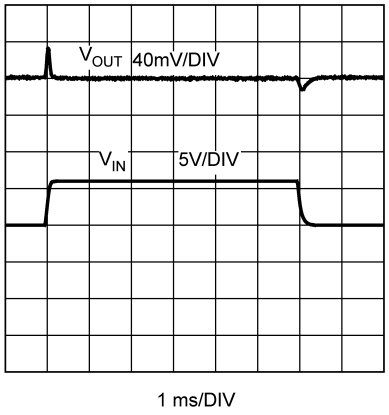


Figure 10.

Frequency
vs.
Frequency Adjust Resistor

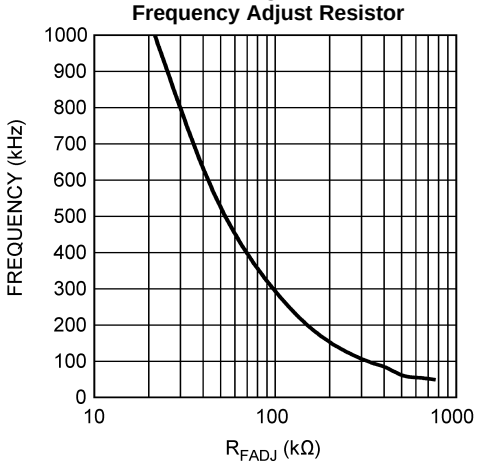


Figure 11.

Maximum Duty Cycle
vs
Frequency
V_{CC} = 3.3V

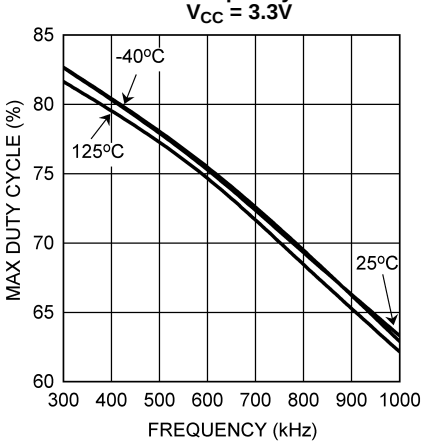


Figure 12.

Maximum Duty Cycle
vs
V_{CC}
f_{SW} = 600 kHz

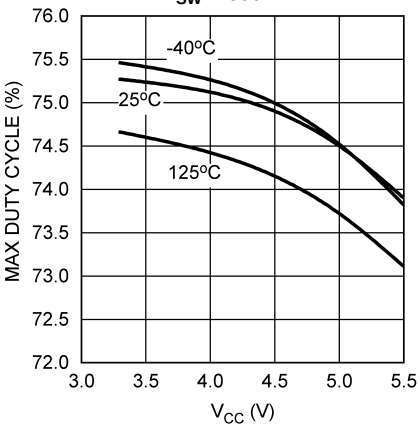


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

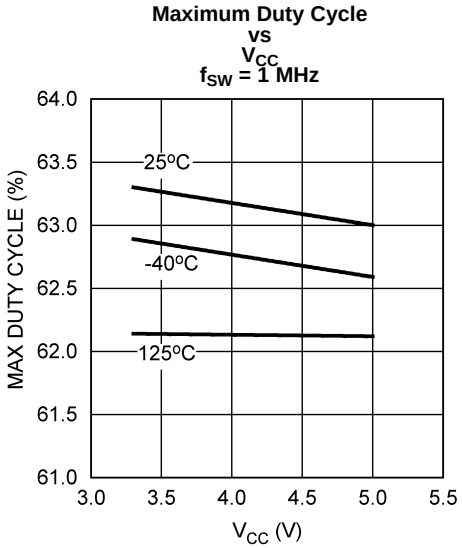
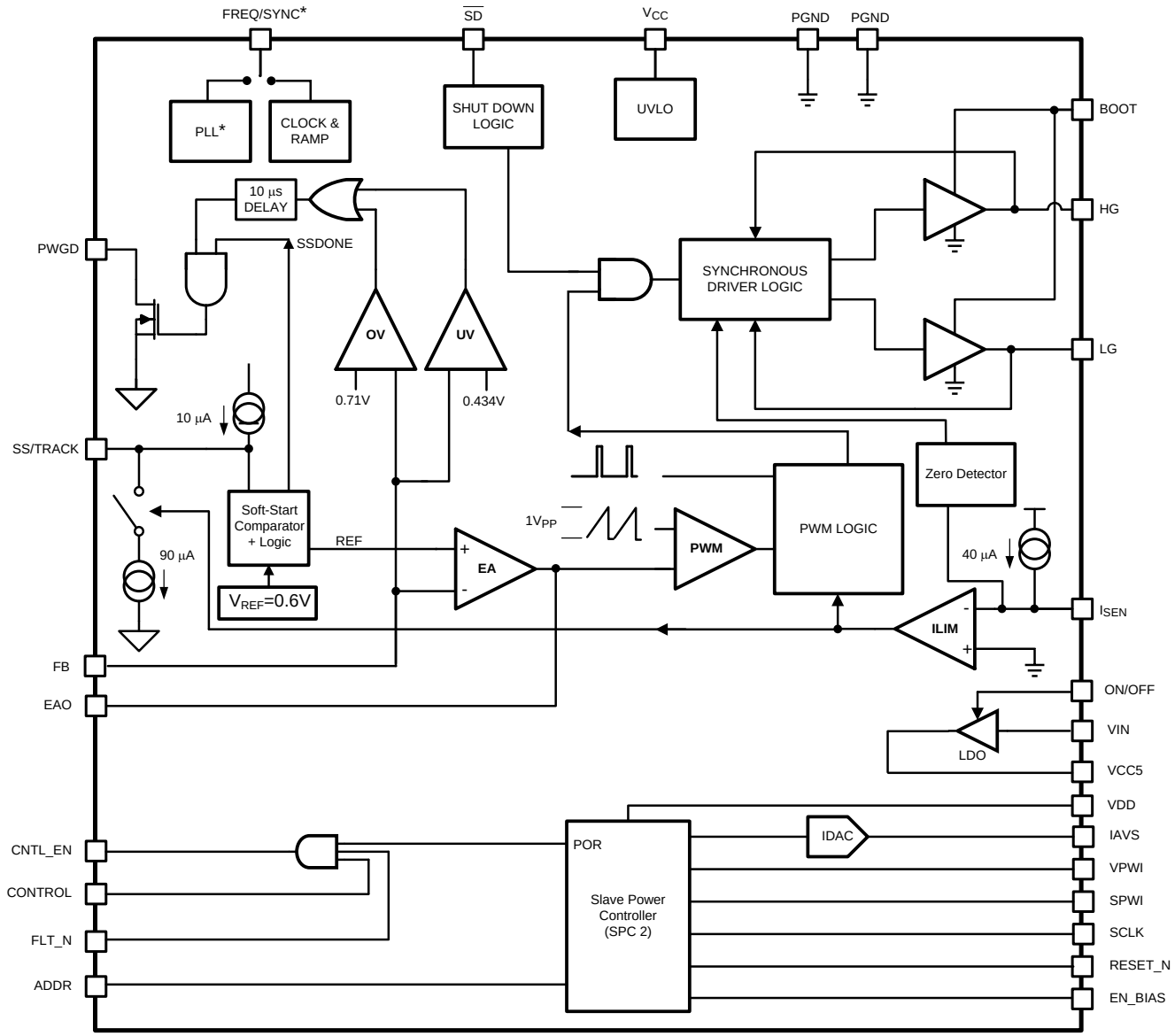


Figure 14.

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BLOCK DIAGRAM



LM10520 PWI REGISTER MAP

The PWI 2.0 standard defines 32 8-bit base registers, and up to 256 8-bit extended registers, on each PWI slave. The table below summarizes these registers and shows default register bit values after reset, as programmed by the factory. The following sub-sections provide additional details on the use of each individual register.

Table 1. SUMMARY

Base Registers											
Register Address	**Register Name**	**Register Usage**	**Type**	**Reset Default Value**							
				7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	R0	IAVS	R/W	0*(1)	Configured by R9						
0x03	R3		R/O	0	0	0	0	1	1	1	FLT_N
0x04	R4	Device Capability	R/O	0	0	0	0	0	0	1	0
0x09	R9	IAVS Default	R/W	I AVS Default Code							
0x0A	R10	Ramp Control	R/W	1	0	0	1	1	1	0	0
0x0F	R15	Revision ID	N/A	0	0	0	0	0	0	0	0
0x1F	R31	Reserved **Do not write to**	R/W	-	-	-	-	-	-	-	-

(1) Note: A bit with an asterisk (*) denotes a register bit that is always read as a fixed value. Writes to these bits will be ignored. A bit with a hyphen (-) denotes a bit in an unimplemented register location. A write into unimplemented register(s) will be ignored. A read of an unimplemented register(s) will produce a “No response frame”. Please refer to PWI specification version 2.0 for further information.

Table 2. R0 - IAVS
AVS Feedback Current Injection

Address	0x00
Type	R/W
Reset Default	8h'7F

Bit	**Field Name**	**Description or Comment**	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:0	IAVS Sourcing Current	Programmed voltage value. Default value is in **bold.**	
		Current Data Code [6:0]	Current (µA)
		7h'00	60
		7h'xx	Linear Scaling
		7h'7F	**0 (default)**

Table 3. R3 - Status
LM10520 Status

Address	0x03
Type	R/O
Reset Default	–

Bit	**Field Name**	**Description or Comment**
7:4	Not Used	Always read back 0
3:1	Not Used	Always read back 1
0	FLT_N	1: FLT_N is high (no fault) 0: FLT_N is low (fault)

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Table 4. R4 - Device Capability Register

Address	0x04
Type	R/O
Reset Default	8h'02

Bit	Field Name	Description or Comment
7:3		Always read back 0
2:0		Always read back 010, specifying PWI 2.0

Table 5. R9 - IAVS Default Register

Address	0x09
Type	R/W
Reset Default	8h'7F

Bit	Field Name	Description or Comment	
7	Sign	Always read back 0.	
6:0	IAVS Default	Current Data Code [6:0]	Current (µA)
		7h'00	60
		7h'xx	Linear Scaling
		7h'7F	**0 (default)**

Table 6. R10 - Ramp Control

Address	0x0A
Type	R/W
Reset Default	8h'9C

Bit	Field Name	Description or Comment				
7	Ramp Control Enable	**1: Enabled** 0: Disabled				
6	Not Used	Always read 0				
5:3	Ramp Time Step Control	Ramp Time Step Control			Ramp Time Step (µs)	
		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	1 2 3 4 6 8 12 16	
2:0	Ramp Code Step Control	Ramp Code Step			Rising Step (LSB)	Falling Step (LSB)
		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	1 2 3 4 6 8 12 16	1 1 2 3 4 5 6 8

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Table 7. R15 - Revision ID Register

Address	0x7F
Type	R/O
Reset Default	8h'00

Bit	Field Name	Description or Comment
7:0		Always read back 0

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APPLICATION INFORMATION

The device is a PowerWise Interface (PWI) compliant energy management unit (EMU). It operates cooperatively with processors using Texas Instruments' Advanced Power Controller (APC) to provide Adaptive or Dynamic Voltage Scaling (AVS, DVS) which drastically improves processor efficiencies compared to conventional power delivery methods. The device consists of PWI registers, logic, and a switching DC/DC buck controller to supply the AVS or DVS voltage domain.

VOLTAGE SCALING

The device is designed to be used in a voltage scaling system to lower the power dissipation of SoC or ASICs. By scaling the supply voltage with the clock frequency and process variations, dramatic power savings can be achieved. Two types of voltage scaling are supported, dynamic voltage scaling (DVS) and adaptive voltage scaling (AVS). DVS systems switch between pre-characterized voltages which are paired to clock frequencies used for frequency scaling in the ASIC. AVS systems track the ASIC's performance and optimizes the supply voltage to the required performance. AVS is a closed loop system that provides process and temperature compensation such that for any given process, temperature, or clock frequency, the minimum supply voltage is delivered.

DIGITALLY ASSISTED VOLTAGE SCALING

The device delivers fast, controlled voltage scaling transients with the help of a digital state machine. The state machine automatically optimizes the slew rate of the output to provide large signal transients with minimal over- and undershoot. This is an important characteristic for voltage scaling systems that rely on minimal over- and undershoot to set voltages as low as possible and save energy.

POWERWISE INTERFACE

The device is programmable via the low-power, 2-wire PowerWise Interface (PWI). This serial interface controls the various voltages and states of the regulator in the device. The output voltage is programmable with 7-bit resolution and an adjustable range, set by the feedback resistors, from 0.6V – Vin*Dmax (see ELECTRICAL CHARACTERISTICS for Dmax). This high resolution voltage control affords accurate temperature and process compensation in AVS. The device supports the full command set as described in PWI 1.0/2.0 specification:

- Core Voltage Adjust
- Reset
- Sleep
- Shutdown
- Wakeup
- Register Read
- Register Write
- Authenticate
- Synchronize

The output voltage of the switching regulator is programmed via the Core Voltage Adjust command.

PWI ADDRESS

A resistor from the ADDR pin to ground sets the device's PWI address. The device senses the resistance as it is initializing from the shutdown state. The device will not update the address until it cycles through shutdown again. Use the table below to choose the appropriate resistor to place form ADDR pin to ground.

PWI Address	Resistance (± 1% tolerance)
0	≤ 40.2 kΩ
1	60.4 kΩ
2	80.6 kΩ
3	100 kΩ
4	120 kΩ
5	140 kΩ

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PWI Address	Resistance (± 1% tolerance)
6	160 kΩ
7	180 kΩ

INPUTS: ON/OFF, ENBIAS, CONTROL, FLT_N, RESET_N, SCLK, SPWI

- ON/OFF:
  - The ON/OFF logic input enables the internal LDO (VCC5 output pin).
- ENBIAS:
  - The ENBIAS logic input enables the internal logic of the LM10520. The LM10520 goes through an initialization procedure upon the rising edge of ENBIAS. Initialization is complete within 100 µsec, after which the device is ready to be used. If at any point ENBIAS goes low, the device enters a low Iq shutdown state.
  - The ENBIAS input is buffered internally by a Schmitt trigger with precision thresholds to allow accurate output voltage sequencing off of the input rail.
- CONTROL:
  - The CONTROL logic input allows control of the CNTL_EN output without incurring delays associated with initialization. This signal is effectively ANDed with the internal 'ready' signal, which is high once initialization is complete.
  - The CONTROL pin level toggles the device between Active and Sleep states, and will reset the R0 register.
- FLT_N:
  - The FLT_N logic input resets and holds the R0 register when its input signal is low. It has no effect on CNTL_EN. This provides a convenient way to support automatic fault recovery modes in the slave power regulator. When connected to a standard PWGD pin of a DC/DC regulator, FLT_N will reset and hold R0 as long as PWGD is low, allowing the slave regulator to recover from the fault by returning to the default voltage. Once FLT_N returns high, R0 can be written to.
- RESET_N:
  - The RESET_N provides a separate, level controlled logic reset.
- SCLK and SPWI:
  - SCLK and SPWI provide serial PWI communication.
- CNTL_EN:
  - The CNTL_EN output connects to the SD# pin. CNTL_EN allows power state control via the PWI interface or ENBIAS/CONTROL logic inputs. LM10520 will drive CNTL_EN to the VDD voltage to enable the buck controller circuitry, and to 0 V to disable the circuitry.

IAVS OUTPUT CURRENT: CONTROLLING THE OUTPUT VOLTAGE

The LM10520 uses a 7-bit current DAC to control the output voltage. Since it is a current output, IAVS can be connected directly to the feedback node. IAVS has a range of 0 – 60 µA with 7 bits of resolution, or a 0.469 µA LSB.

IAVS should be connected to the feedback node of LM10520 as shown in Figure 15. The output voltage VOUT is expressed as:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) - I_{AVS} \times R_{FB1} \quad (1)$$

where

- VFB = the regulated feedback voltage of the slave regulator

This equation is valid for V_{OUT} > VFB.

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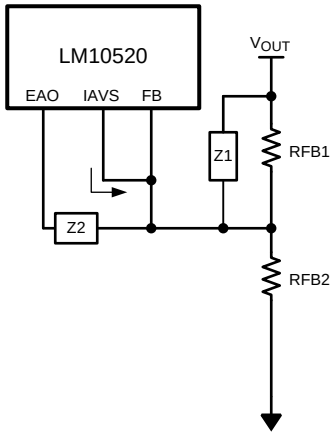


Figure 15. Connecting IAVS to the Feedback Node

Using Register R9 to Change the Default Output Voltage

The LM10520 default IAVS current is set by R9. R9 is trimmed to 0x7F, so that IAVS = 0µA when power is applied to LM10520. Between power cycling, R9 can be changed so that IAVS defaults to values between 0 - 60 µA. This can be useful for software trim of the default output voltage of the LM10520 controlled regulator. In order to do this, the system must take care to write to R9 before enabling the output. (The output can be enabled/disabled while keeping the LM10520 logic on via the CONTROL input.) Therefore, R9 must be written to by some system controller that is on a different power domain than that provided by LM10520. In addition, the "INITIAL_VDD" register in the Advanced Power Controller (APC) must have the same value as R9 so that the APC and LM10520 default to the same voltage code.

Digital Slew Rate Control

The IAVS and IAVS Mirror outputs have an adjustable, digital slew rate control. The slew rate control is programmed in register R10.

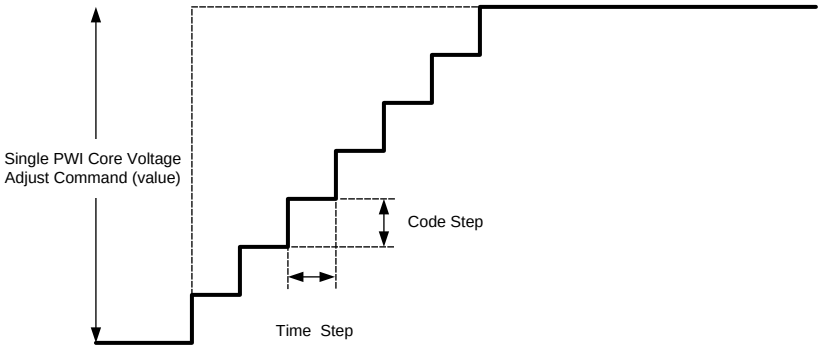


Figure 16. Digital Slew Rate Control

LM10520 effectively overrides the internal reference of the slave regulator to allow it to operate in an AVS system. The amount of current drawn from the AVS enabled power supply when scaling voltage depends on several factors determined by the well known equation for current in a capacitor:

$I^C = Cdv/dt$

where

- C is the total output capacitance seen by the power supply
- dv is the voltage step
- dt is the step time (2)

The digital slew rate control of LM10520 allows independent manipulation of the dv and dt terms to accommodate a wide range of output capacitances.

STATES

Startup

During the startupt state, the LM10520 initializes all its registers and enables its bandgap. This process typically takes 1.116 msec. CNTL_EN is low during startup.

Active

During the active state, CNTL_EN is is high, the IAVS DACs are enabled, and PWI registers can be accessed.

Sleep

During the sleep state, CNTL_EN is low, the IAVS DACs are disabled, and PWI registers can be accessed.

Fault

During the fault state, the IAVS current register (R0) is reset, after which the LM10520 automatically returns to its previous state.

Shutdown

During the shutdown state, CNTL_EN is low, the IAVS DACs are disabled, and most internal circuitry is disabled. Only the PWI state machine is biased to allow register access.

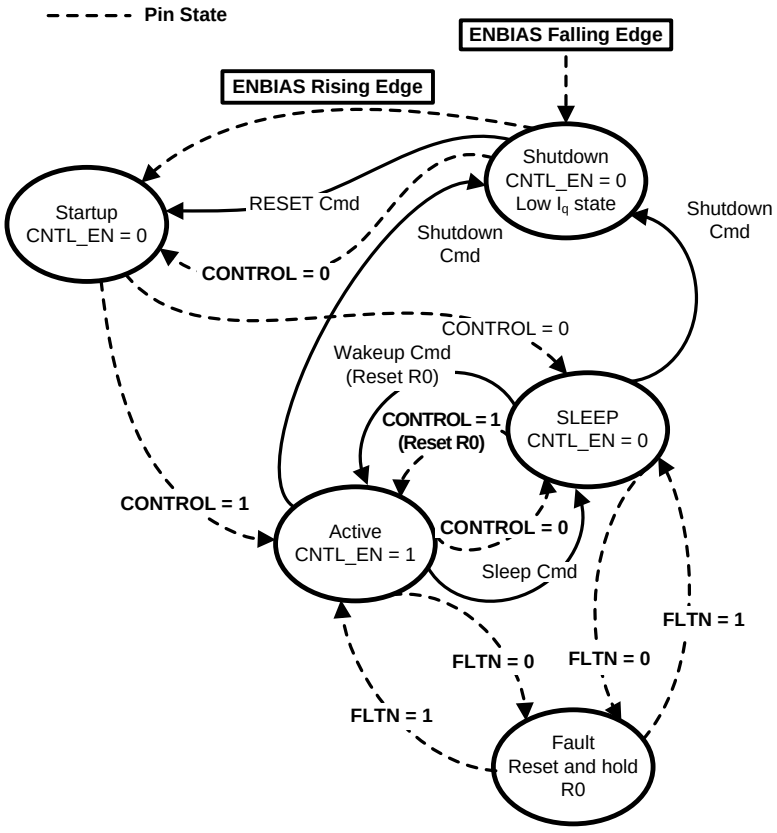


Figure 17. LM10520 State Diagram

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VOLTAGE MODE CONTROLLER

The LM10520 incorporates control circuitry and drivers for synchronous buck PWM regulation. It uses voltage mode control to achieve the low duty cycles necessary for the low conversion ratios in an AVS system. It has flexible input enable controls to allow logic level control of output voltage enable, bias enable, and internal LDO enable. In addition, an active low fault input can be used for system fault response sequencing. These inputs allow simple, system level control of the device state. The LM10520 also includes input under-voltage lock-out (UVLO) and a power good (PWGD) flag (based on over-voltage and under-voltage detection). The over-voltage and under-voltage signals are OR-gated to drive the power good signal and provide a logic signal to the system if the output voltage goes out of regulation. Current limit is achieved by sensing the voltage VDS across the low side MOSFET. The LM10520 is also able to stat-up with the output pre-biased with a load. The LM10520 also allows the switching frequency to be a synchronized with an external clock source.

START UP/SOFT-START

When V_{CC} exceeds 2.79V and the shutdown pin ($\overline{SD}$) sees a logic high, the soft-start period begins. Then an internal, fixed 10 µA source begins charging the soft-start capacitor. During soft-start the voltage on the soft-start capacitor C_{SS} is connected internally to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the LM10520 reference voltage of 0.6V. At this point the reference voltage takes over at the non-inverting error amplifier input. The capacitance of C_{SS} determines the length of the soft-start period, and can be approximated by:

$$C_{SS} = \frac{t_{SS}}{60} \quad (3)$$

where

- C_{SS} is in µF
- t_{SS} is in ms

During soft start the Power Good flag is forced low and it is released when the FB pin voltage reaches 70% of 0.6V. At this point the chip enters normal operation mode, and the output overvoltage and undervoltage monitoring starts.

SETTING THE DEFAULT AND PROGRAMMABILITY RANGE OF THE OUTPUT VOLTAGE

The LM10520 has a flexible output voltage range control. When the system is starting up, the output voltage exits soft-start and AVS has not been enabled by the load (the load is the AVS enabled processor, and is booting up). This is the default voltage of the LM10520, and is set by the feedback resistor divider ratio. Once the automatic AVS authentication process has successfully completed, the AVS loop is engaged and the LM10520 automatically reduces the voltage. A 7-bit current source is injected into the feedback resistor node to achieve voltage scaling. Therefore, the range and resolution of the device is adjustable via the top feedback resistor.

SETTING THE SWITCHING FREQUENCY

During fixed-frequency mode of operation the PWM frequency is adjustable between 50 kHz and 1 MHz and is set by an external resistor, R_{FADJ}, between the FREQ/SYNC pin and ground. The resistance needed for a desired frequency is approximated by the curve Frequency vs. Frequency Adjust Resistor in the Typical Performance Characteristics.

When it is desired to synchronize the switching frequency with an external clock source, the LM10520 has the unique ability to synchronize from this external source within the range of 250 kHz to 1MHz. The external clock signal should be AC coupled to the FREQ/SYNC pin as shown below in Figure 18, where the R_{FADJ} is chosen so that the fixed frequency is approximately within ±30% of the external synchronizing clock frequency. An internal protection diode clamps the low level of the synchronizing signal to approximately -0.5V. The internal clock sychronizes to the rising edge of the external clock.

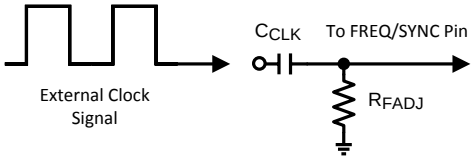


Figure 18. AC Coupled Clock

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It is recommended to choose an AC coupling capacitance in the range of 50 pF to 100 pF. Exceeding the recommended capacitance may inject excessive energy through the internal clamping diode structure present on the FREQ/SYNC pin.

The typical trip level of the synchronization pin is 1.5V. To ensure proper synchronization and to avoid damaging the IC, the peak-to-peak value (amplitude) should be between 2.5V and V_{CC}. The minimum width of this pulse must be greater than 100 ns, and it's maximum width must be 100 ns less than the period of the switching cycle.

The external clock synchronization process begins once the LM10520 is enabled and an external clock signal is detected. During the external clock synchronization process the internal clock initially switches at approximately 1.5 MHz and decreases until it has matched the external clock's frequency. The lock-in period is approximately 30 µs if the external clock is switching at 1MHz, and about 100 µs if the external clock is at 200 kHz. When there is no clock signal present, the LM10520 enters into fixed-frequency mode and begins switching at the frequency set by the R_{FADJ} resistor. If the external clock signal is removed after frequency synchronization, the LM10520 will enter fixed-frequency mode within two clock cycles. If the external clock is removed within the 30 µs lock-in period, the LM10520 will re-enter fixed-frequency mode within two internal clock cycles after the lock-in period.

OUTPUT PRE-BIAS STARTUP

If there is a pre-biased load on the output of the LM10520 during startup, the IC will disable switching of the low-side MOSFET and monitor the SW node voltage during the off-time of the high-side MOSFET. There is no load current sensing while in pre-bias mode because the low-side MOSFET never turns on. The IC will remain in this pre-bias mode until it sees the SW node stays below 0V during the entire high-side MOSFET's off-time. Once it is determined that the SW node remained below 0V during the high-side off-time, the low-side MOSFET begins switching during the next switching cycle. Figure 19 shows the SW node, HG, and LG signals during pre-bias startup. The pre-biased output voltage should not exceed V_{CC} + V_{GS} of the external High-Side MOSFET to ensure that the High-Side MOSFET will be able to switch during startup.

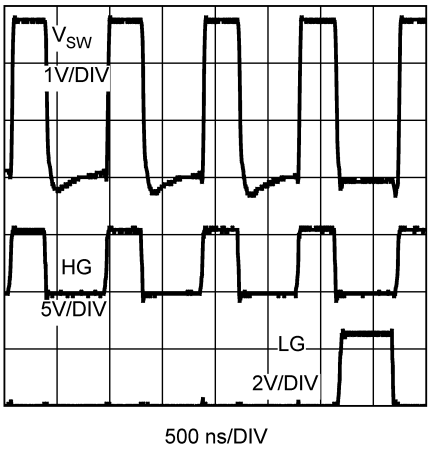


Figure 19. Output Pre-Bias Mode Waveforms

TRACKING A VOLTAGE LEVEL

The LM10520 can track the output of a master power supply during soft-start by connecting a resistor divider to the SS/TRACK pin. In this way, the output voltage slew rate of the LM10520 will be controlled by the master supply for loads that require precise sequencing. When the tracking function is used no soft-start capacitor should be connected to the SS/TRACK pin. However in all other cases, a C_{SS} value of at least 1nF between the soft-start pin and ground should be used.

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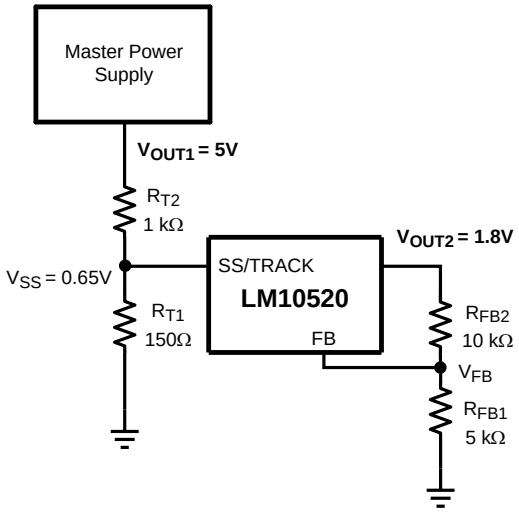


Figure 20. Tracking Circuit

One way to use the tracking feature is to design the tracking resistor divider so that the master supply's output voltage (V_{OUT1}) and the LM10520's output voltage (represented symbolically in Figure 20 as V_{OUT2}, i.e. without explicitly showing the power components) both rise together and reach their target values at the same time. For this case, the equation governing the values of the tracking divider resistors R_{T1} and R_{T2} is:

$$0.65 = V_{OUT1} \frac{R_{T1}}{R_{T1}+R_{T2}} \tag{4}$$

The current through R_{T1} should be about 4mA for precise tracking. The final voltage of the SS/TRACK pin should be set higher than the feedback voltage of 0.6V (say about 0.65V as in the above equation). If the master supply voltage was 5V and the LM10520 output voltage was 1.8V, for example, then the value of R_{T1} needed to give the two supplies identical soft-start times would be 150Ω. A timing diagram for the equal soft-start time case is shown in Figure 21.

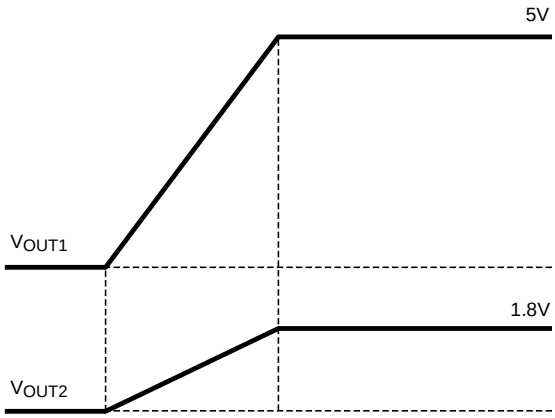


Figure 21. Tracking with Equal Soft-Start Time

TRACKING A VOLTAGE SLEW RATE

The tracking feature can alternatively be used not to make both rails reach regulation at the same time but rather to have similar rise rates (in terms of output dV/dt). This method ensures that the output voltage of the LM10520 always reaches regulation before the output voltage of the master supply. In this case, the tracking resistors can be determined based on the following equation:

$$0.65 = V_{OUT2} \frac{R_{T1}}{R_{T1} + R_{T2}} \quad (5)$$

For the example case of V_{OUT1} = 5V and V_{OUT2} = 1.8V, with R_{T1} set to 150Ω as before, R_{T2} is calculated from the above equation to be 265Ω. A timing diagram for the case of equal slew rates is shown in Figure 22.

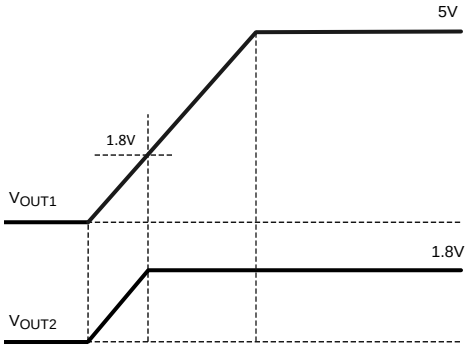


Figure 22. Tracking with Equal Slew Rates

MOSFET GATE DRIVERS

The LM10520 has two gate drivers designed for driving N-channel MOSFETs in a synchronous mode. Note that unlike most other synchronous controllers, the bootstrap capacitor of the LM10520 provides power not only to the driver of the upper MOSFET, but the lower MOSFET driver too (both drivers are ground referenced, i.e. no floating driver).

Two things must be kept in mind here. First, the BOOT pin has an absolute maximum rating of 18V. This must never be exceeded, even momentarily. Since the bootstrap capacitor is connected to the SW node, the peak voltage impressed on the BOOT pin is the sum of the input voltage (V_{IN}) plus the voltage across the bootstrap capacitor (ignoring any forward drop across the bootstrap diode). The bootstrap capacitor is charged up by a given rail (called V_{BOOT_DC} here) whenever the upper MOSFET turns off. This rail can be the same as V_{CC} or it can be any external ground-referenced DC rail. But care has to be exercised when choosing this bootstrap DC rail that the BOOT pin is not damaged. For example, if the desired maximum V_{IN} is 14V, and V_{BOOT_DC} is chosen to be the same as V_{CC}, then clearly if the V_{CC} rail is 6V, the peak voltage on the BOOT pin is 14V + 6V = 20V. This is unacceptable, as it is in excess of the rating of the BOOT pin. A V_{CC} of 3V would be acceptable in this case. Or the V_{IN} range must be reduced accordingly. There is also the option of deriving the bootstrap DC rail from another 3V external rail, independent of V_{CC}.

The second thing to be kept in mind here is that the output of the low-side driver swings between the bootstrap DC rail level of V_{BOOT_DC} and Ground, whereas the output of the high-side driver swings between V_{IN}+ V_{BOOT_DC} and Ground. To keep the high-side MOSFET fully on when desired, the Gate pin voltage of the MOSFET must be higher than its instantaneous Source pin voltage by an amount equal to the 'Miller plateau'. It can be shown that this plateau is equal to the threshold voltage of the chosen MOSFET plus a small amount equal to Io/g. Here Io is the maximum load current of the application, and g is the transconductance of this MOSFET (typically about 100 for logic-level devices). That means we must choose V_{BOOT_DC} to at least exceed the Miller plateau level. This may therefore affect the choice of the threshold voltage of the external MOSFETs, and that in turn may depend on the chosen V_{BOOT_DC} rail.

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So far, in the discussion above, the forward drop across the bootstrap diode has been ignored. But since that does affect the output of the driver somewhat, it is a good idea to include this drop in the following examples. Looking at the Typical Application schematic, this means that the difference voltage V_{CC} - V_{D1}, which is the voltage the bootstrap capacitor charges up to, must always be greater than the maximum tolerance limit of the threshold voltage of the upper MOSFET. Here V_{D1} is the forward voltage drop across the bootstrap diode D1. This may place restrictions on the minimum input voltage and/or type of MOSFET used.

A basic bootstrap circuit can be built using one Schottky diode and a small capacitor, as shown in Figure 23. The capacitor C_{BOOT} serves to maintain enough voltage between the top MOSFET gate and source to control the device even when the top MOSFET is on and its source has risen up to the input voltage level. The charge pump circuitry is fed from V_{CC}, which can operate over a range from 3.0V to 6.0V. Using this basic method the voltage applied to the gates of both high-side and low-side MOSFETs is V_{CC} - V_D. This method works well when V_{CC} is 5V±10%, because the gate drives will get at least 4.0V of drive voltage during the worst case of V_{CC-MIN} = 4.5V and V_{D-MAX} = 0.5V. Logic level MOSFETs generally specify their on-resistance at V_{GS} = 4.5V. When V_{CC} = 3.3V±10%, the gate drive at worst case could go as low as 2.5V. Logic level MOSFETs are not ensured to turn on, or may have much higher on-resistance at 2.5V. Sub-logic level MOSFETs, usually specified at V_{GS} = 2.5V, will work, but are more expensive, and tend to have higher on-resistance. The circuit in Figure 23 works well for input voltages ranging from 1V up to 14V and V_{CC} = 5V±10%, because the drive voltage depends only on V_{CC}.

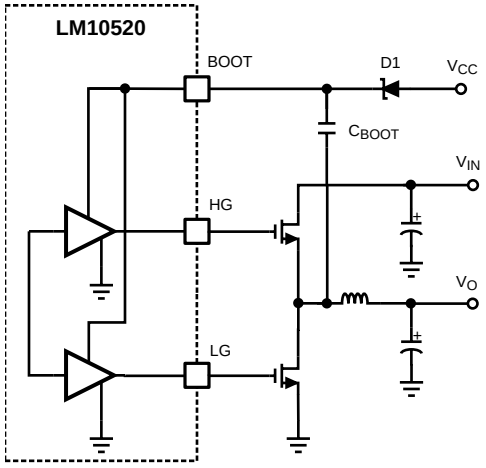


Figure 23. Basic Charge Pump (Bootstrap)

Note that the LM10520 can be paired with a low cost linear regulator like the LM78L05 to run from a single input rail between 6.0 and 14V. The 5V output of the linear regulator powers both the V_{CC} and the bootstrap circuit, providing efficient drive for logic level MOSFETs. An example of this circuit is shown in Figure 24.

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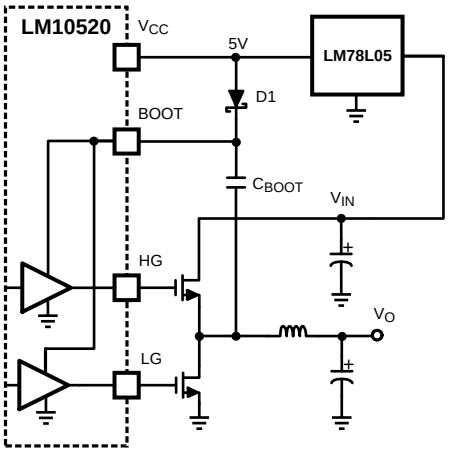


Figure 24. LM78L05 Feeding Basic Charge Pump

Figure 25 shows a second possibility for bootstrapping the MOSFET drives using a doubler. This circuit provides an equal voltage drive of V_{CC} - $3V_D$ + V_{IN} to both the high-side and low-side MOSFET drives. This method should only be used in circuits that use 3.3V for both V_{CC} and V_{IN}. Even with V_{IN} = V_{CC} = 3.0V (10% lower tolerance on 3.3V) and V_D = 0.5V both high-side and low-side gates will have at least 4.5V of drive. The power dissipation of the gate drive circuitry is directly proportional to gate drive voltage, hence the thermal limits of the LM10520 IC will quickly be reached if this circuit is used with V_{CC} or V_{IN} voltages over 5V.

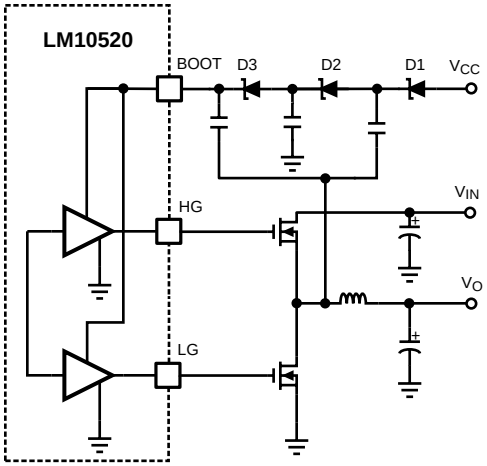


Figure 25. Charge Pump with Added Gate Drive

All the gate drive circuits shown in the above figures typically use 100 nF ceramic capacitors in the bootstrap locations.

POWER GOOD SIGNAL

The open drain output on the Power Good pin needs a pull-up resistor to a low voltage source. The pull-up resistor should be chosen so that the current going into the Power Good pin is less than 1mA. A 100 kΩ resistor is recommended for most applications.

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The Power Good signal is an OR-gated flag which takes into account both output over-voltage and under-voltage conditions. If the feedback pin (FB) voltage is 18% above its nominal value (118% x V_{FB} = 0.708V) or falls 28% below that value (72% x V_{FB} = 0.42V) the Power Good flag goes low. The Power Good flag can be used to signal other circuits that the output voltage has fallen out of regulation, however the switching of the LM10520 continues regardless of the state of the Power Good signal. The Power Good flag will return to logic high whenever the feedback pin voltage is between 72% and 118% of 0.6V.

CURRENT LIMIT

Current limit is realized by sensing the voltage across the low-side MOSFET while it is on. The R_{DSON} of the MOSFET is a known value; hence the current through the MOSFET can be determined as:

$$V_{DS} = I_{OUT} \times R_{DSON} \quad (6)$$

The current through the low-side MOSFET while it is on is also the falling portion of the inductor current. The current limit threshold is determined by an external resistor, R_{CS}, connected between the switching node and the I_{SEN} pin. A constant current (I_{SEN-TH}) of 40 µA typical is forced through R_{CS}, causing a fixed voltage drop. This fixed voltage is compared against V_{DS} and if the latter is higher, the current limit of the chip has been reached. To obtain a more accurate value for R_{CS} you must consider the operating values of R_{DSON} and I_{SEN-TH} at their operating temperatures in your application and the effect of slight parameter differences from part to part. R_{CS} can be found by using the following equation using the R_{DSON} value of the low side MOSFET at it's expected hot temperature and the absolute minimum value expected over the full temperature range for the for the I_{SEN-TH} which is 25 µA:

$$R_{CS} = R_{DSON-HOT} \times I_{LIM} / I_{SEN-TH} \quad (7)$$

For example, a conservative 15A current limit in a 10A design with a $R_{DSON-HOT}$ of 10 mΩ would require a 6kΩ resistor. The minimum value for R_{CS} in any application is 1kΩ. Because current sensing is done across the low-side MOSFET, no minimum high-side on-time is necessary. The LM10520 enters current limit mode if the inductor current exceeds the current limit threshold at the point where the high-side MOSFET turns off and the low-side MOSFET turns on. (The point of peak inductor current, see Figure 26). Note that in normal operation mode the high-side MOSFET always turns on at the beginning of a clock cycle. In current limit mode, by contrast, the high-side MOSFET on-pulse is skipped. This causes inductor current to fall. Unlike a normal operation switching cycle, however, in a current limit mode switching cycle the high-side MOSFET will turn on as soon as inductor current has fallen to the current limit threshold. The LM10520 will continue to skip high-side MOSFET pulses until the inductor current peak is below the current limit threshold, at which point the system resumes normal operation.

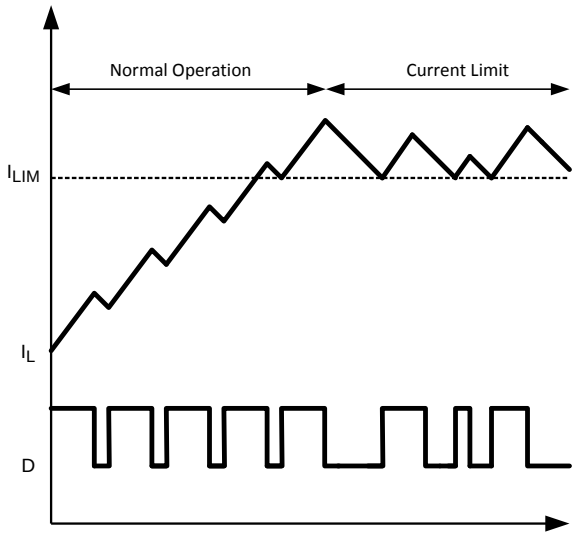


Figure 26. Current Limit Threshold

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Unlike a high-side MOSFET current sensing scheme, which limits the peaks of inductor current, low-side current sensing is only allowed to limit the current during the converter off-time, when inductor current is falling. Therefore in a typical current limit plot the valleys are normally well defined, but the peaks are variable, according to the duty cycle. The PWM error amplifier and comparator control the off-pulse of the high-side MOSFET, even during current limit mode, meaning that peak inductor current can exceed the current limit threshold. Assuming that the output inductor does not saturate, the maximum peak inductor current during current limit mode can be calculated with the following equation:

$$R_{LIM}(T_j) = \frac{I_{CL} \times R_{DS(ON)max}}{I_{LIM\text{-}TH}(T_j)}$$

where

- T_{SW} is the inverse of switching frequency f_{SW} (8)

The 200 ns term represents the minimum off-time of the duty cycle, which ensures enough time for correct operation of the current sensing circuitry.

In order to minimize the time period in which peak inductor current exceeds the current limit threshold, the IC also discharges the soft-start capacitor through a fixed 90 µA sink. The output of the LM10520 internal error amplifier is limited by the voltage on the soft-start capacitor. Hence, discharging the soft-start capacitor reduces the maximum duty cycle D of the controller. During severe current limit this reduction in duty cycle will reduce the output voltage if the current limit conditions last for an extended time. Output inductor current will be reduced in turn to a flat level equal to the current limit threshold. The third benefit of the soft-start capacitor discharge is a smooth, controlled ramp of output voltage when the current limit condition is cleared.

DESIGN CONSIDERATIONS

The following is a design procedure for all the components needed to create the Typical Application Circuit shown on the front page. This design converts 3.3V (V_{IN}) to 1.2V (V_{OUT}) at a maximum load of 4A with an efficiency of 89% and a switching frequency of 300 kHz. The same procedures can be followed to create many other designs with varying input voltages, output voltages, and load currents.

Input Capacitor

The input capacitors in a Buck converter are subjected to high stress due to the input current trapezoidal waveform. Input capacitors are selected for their ripple current capability and their ability to withstand the heat generated since that ripple current passes through their ESR. Input rms ripple current is approximately:

$$I_{RMS_RIP} = I_{OUT} \times \sqrt{D(1 - D)}$$

where

- duty cycle $D = V_{OUT}/V_{IN}$ (9)

The power dissipated by each input capacitor is:

$$P_{CAP} = \frac{(I_{RMS_RIP})^2 \times ESR}{n^2}$$

where

- n is the number of paralleled capacitors
- ESR is the equivalent series resistance of each capacitor (10)

The equation above indicates that power loss in each capacitor decreases rapidly as the number of input capacitors increases. The worst-case ripple for a Buck converter occurs during full load and when the duty cycle (D) is 0.5. For this 3.3V to 1.2V design the duty cycle is 0.364. For a 4A maximum load the ripple current is 1.92A.

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Output Inductor

The output inductor forms the first half of the power stage in a Buck converter. It is responsible for smoothing the square wave created by the switching action and for controlling the output current ripple (ΔI_{OUT}). The inductance is chosen by selecting between tradeoffs in efficiency and response time. The smaller the output inductor, the more quickly the converter can respond to transients in the load current. However, as shown in the efficiency calculations, a smaller inductor requires a higher switching frequency to maintain the same level of output current ripple. An increase in frequency can mean increasing loss in the MOSFETs due to the charging and discharging of the gates. Generally the switching frequency is chosen so that conduction loss outweighs switching loss. The equation for output inductor selection is:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_{OUT} \times f_{SW}} \times D$$

$$L = \frac{3.3V - 1.2V}{0.4 \times 4A \times 300\ kHz} \times \frac{1.2V}{3.3V}$$

$$L = 1.6\ \mu H \quad (11)$$

Here we have plugged in the values for output current ripple, input voltage, output voltage, switching frequency, and assumed a 40% peak-to-peak output current ripple. This yields an inductance of 1.6 µH. The output inductor must be rated to handle the peak current (also equal to the peak switch current), which is (I_{OUT} + (0.5 x ΔI_{OUT})) = 4.8A, for a 4A design.

The Coilcraft DO3316P-222P is 2.2 µH, is rated to 7.4A peak, and has a direct current resistance (DCR) of 12 mΩ. After selecting the Coilcraft DO3316P-222P for the output inductor, actual inductor current ripple should be re-calculated with the selected inductance value, as this information is needed to select the output capacitor. Re-arranging the equation used to select inductance yields the following:

$$\Delta I_{OUT} = \frac{V_{IN(MAX)} - V_O}{f_{SW} \times L_{ACTUAL}} \times D$$

where

- $V_{IN(MAX)}$ is assumed to be 10% above the steady state input voltage, or 3.6V at V_{IN} = 3.3V (12)

The re-calculated current ripple will then be 1.2A. This gives a peak inductor/switch current will be 4.6A.

Output Capacitor

The output capacitor forms the second half of the power stage of a Buck switching converter. It is used to control the output voltage ripple (ΔV_{OUT}) and to supply load current during fast load transients.

In this example the output current is 4A and the expected type of capacitor is an aluminum electrolytic, as with the input capacitors. Other possibilities include ceramic, tantalum, and solid electrolyte capacitors, however the ceramic type often do not have the large capacitance needed to supply current for load transients, and tantalums tend to be more expensive than aluminum electrolytic. Aluminum capacitors tend to have very high capacitance and fairly low ESR, meaning that the ESR zero, which affects system stability, will be much lower than the switching frequency. The large capacitance means that at the switching frequency, the ESR is dominant, hence the type and number of output capacitors is selected on the basis of ESR. One simple formula to find the maximum ESR based on the desired output voltage ripple, ΔV_{OUT} and the designed output current ripple, ΔI_{OUT}, is:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \quad (13)$$

In this example, in order to maintain a 2% peak-to-peak output voltage ripple and a 40% peak-to-peak inductor current ripple, the required maximum ESR is 20 mΩ. The Sanyo 4SP560M electrolytic capacitor will give an equivalent ESR of 14 mΩ. The capacitance of 560 µF is enough to supply energy even to meet severe load transient demands.

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MOSFETs

Selection of the power MOSFETs is governed by a trade-off between cost, size, and efficiency. One method is to determine the maximum cost that can be endured, and then select the most efficient device that fits that price. Breaking down the losses in the high-side and low-side MOSFETs and then creating spreadsheets is one way to determine relative efficiencies between different MOSFETs. Good correlation between the prediction and the bench result is not ensured, however. Single-channel buck regulators that use a controller IC and discrete MOSFETs tend to be most efficient for output currents of 2 to 10A.

Losses in the high-side MOSFET can be broken down into conduction loss, gate charging loss, and switching loss. Conduction, or I^2R loss, is approximately:

$$P_C = D\ (I_O^2 \times R_{DSON\text{-}HI} \times 1.3) \text{ (High-Side MOSFET)} \quad (14)$$

$$P_C = (1 - D) \times (I_O^2 \times R_{DSON\text{-}LO} \times 1.3) \text{ (Low-Side MOSFET)} \quad (15)$$

In the above equations the factor 1.3 accounts for the increase in MOSFET R_{DSON} due to heating. Alternatively, the 1.3 can be ignored and the R_{DSON} of the MOSFET estimated using the R_{DSON} Vs. Temperature curves in the MOSFET datasheets.

Gate charging loss results from the current driving the gate capacitance of the power MOSFETs, and is approximated as:

$$P_{GC} = n \times (V_{DD}) \times Q_G \times f_{SW}$$

where

- 'n' is the number of MOSFETs (if multiple devices have been placed in parallel)
- V_{DD} is the driving voltage (see MOSFET GATE DRIVERS)
- Q_{GS} is the gate charge of the MOSFET (16)

If different types of MOSFETs are used, the 'n' term can be ignored and their gate charges simply summed to form a cumulative Q_G. Gate charge loss differs from conduction and switching losses in that the actual dissipation occurs in the LM10520, and not in the MOSFET itself.

Switching loss occurs during the brief transition period as the high-side MOSFET turns on and off, during which both current and voltage are present in the channel of the MOSFET. It can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_O \times (t_r + t_f) \times f_{SW}$$

where

- t_r and t_f are the rise and fall times of the MOSFET (17)

Switching loss occurs in the high-side MOSFET only.

For this example, the maximum drain-to-source voltage applied to either MOSFET is 3.6V. The maximum drive voltage at the gate of the high-side MOSFET is 3.1V, and the maximum drive voltage for the low-side MOSFET is 3.3V. Due to the low drive voltages in this example, a MOSFET that turns on fully with 3.1V of gate drive is needed. For designs of 5A and under, dual MOSFETs in SO-8 provide a good trade-off between size, cost, and efficiency.

Support Components

$C_{IN}2$ - A small (0.1 to 1 µF) ceramic capacitor should be placed as close as possible to the drain of the high-side MOSFET and source of the low-side MOSFET (dual MOSFETs make this easy). This capacitor should be X5R type dielectric or better.

R_{CC}, C_{CC}- These are standard filter components designed to ensure smooth DC voltage for the chip supply. R_{CC} should be 1 to 10Ω. C_{CC} should 1µF, X5R type or better.

C_{BOOT}- Bootstrap capacitor, typically 100 nF.

$R_{PULL\text{-}UP}$ – This is a standard pull-up resistor for the open-drain power good signal (PWGD). The recommended value is 100 kΩ connected to V_{CC}. If this feature is not necessary, the resistor can be omitted.

D_1 - A small Schottky diode should be used for the bootstrap. It allows for a minimum drop for both high and low-side drivers. The MBR0520 or BAT54 work well in most designs.

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R_{CS} - Resistor used to set the current limit. Since the design calls for a peak current magnitude (I_{OUT} + (0.5 x ΔI_{OUT})) of 4.8A, a safe setting would be 6A. (This is below the saturation current of the output inductor, which is 7A.) Following the equation from the Current Limit section, a 1.3 kΩ resistor should be used.

R_{FADJ} - This resistor is used to set the switching frequency of the chip. The resistor value is approximated from the Frequency vs. Frequency Adjust Resistor curve in the Typical Performance Characteristics. For 300 kHz operation, a 100 kΩ resistor should be used.

C_{SS} - The soft-start capacitor depends on the user requirements and is calculated based on the equation given in the section titled START UP/SOFT-START. Therefore, for a 7 ms delay, a 12 nF capacitor is suitable.

Control Loop Compensation

The LM10520 uses voltage-mode ('VM') PWM control to correct changes in output voltage due to line and load transients. VM requires careful small signal compensation of the control loop for achieving high bandwidth and good phase margin.

The control loop is comprised of two parts. The first is the power stage, which consists of the duty cycle modulator, output inductor, output capacitor, and load. The second part is the error amplifier, which for the LM10520 is a 9MHz op-amp used in the classic inverting configuration. Figure 27 shows the regulator and control loop components.

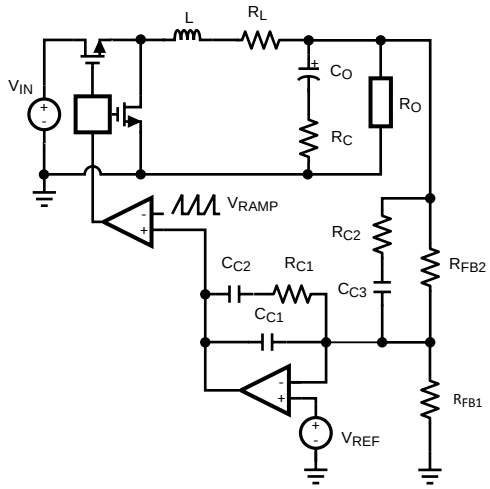


Figure 27. Power Stage and Error Amp

One popular method for selecting the compensation components is to create Bode plots of gain and phase for the power stage and error amplifier. Combined, they make the overall bandwidth and phase margin of the regulator easy to see. Software tools such as Excel, MathCAD, and Matlab are useful for showing how changes in compensation or the power stage affect system gain and phase.

The power stage modulator provides a DC gain A_{DC} that is equal to the input voltage divided by the peak-to-peak value of the PWM ramp. This ramp is $1.0V_{pk\text{-}pk}$ for the LM10520. The inductor and output capacitor create a double pole at frequency f_{DP}, and the capacitor ESR and capacitance create a single zero at frequency f_{ESR}. For this example, with V_{IN} = 3.3V, these quantities are:

$$A_{DC} = \frac{V_{IN}}{V_{RAMP}} = \frac{3.3}{1.0} = 10.4 \text{ dB} \tag{18}$$

$$f_{DP} = \frac{1}{2\pi}\sqrt{\frac{R_O + R_L}{LC_O(R_O + ESR)}} = 4.5 \text{ kHz} \tag{19}$$

$$f_{ESR} = \frac{1}{2\pi C_O ESR} = 20.3 \text{ kHz} \tag{20}$$

In the equation for f_{DP}, the variable R_L is the power stage resistance, and represents the inductor DCR plus the on resistance of the top power MOSFET. R_O is the output voltage divided by output current. The power stage transfer function G_{PS} is given by the following equation, and Figure 28 shows Bode plots of the phase and gain in this example.

$$G_{PS} = \frac{V_{IN} \times R_O}{V_{RAMP}} \times \frac{sC_OR_C + 1}{as^2 + bs + c}$$

where

- $a = LC_O(R_O + R_C)$
- $b = L + C_O(R_OR_L + R_OR_C + R_CR_L)$
- $c = R_O + R_L$

(21)

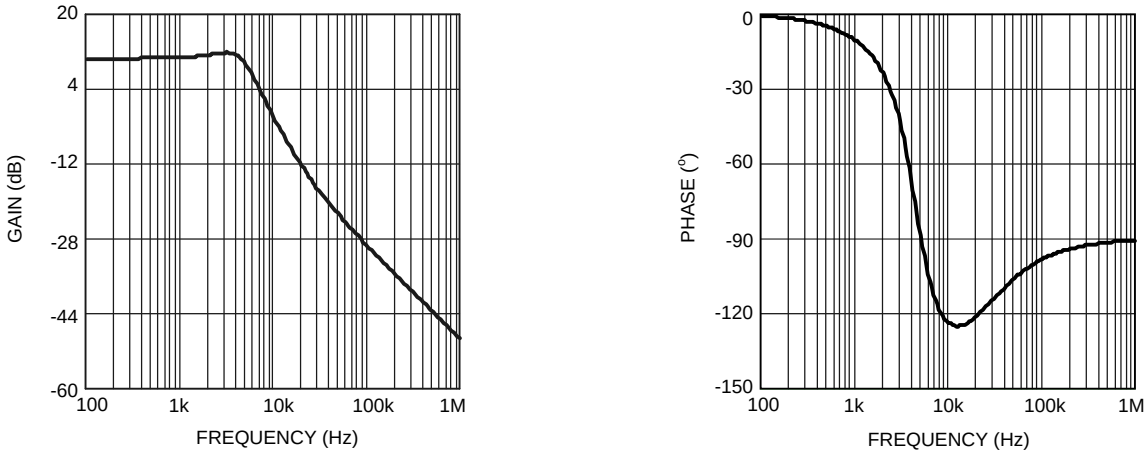


Figure 28. Power Stage Gain and Phase

The double pole at 4.5 kHz causes the phase to drop to approximately -130° at around 10 kHz. The ESR zero, at 20.3 kHz, provides a +90° boost that prevents the phase from dropping to -180°. If this loop were left uncompensated, the bandwidth would be approximately 10 kHz and the phase margin 53°. In theory, the loop would be stable, but would suffer from poor DC regulation (due to the low DC gain) and would be slow to respond to load transients (due to the low bandwidth.) In practice, the loop could easily become unstable due to tolerances in the output inductor, capacitor, or changes in output current, or input voltage. Therefore, the loop is compensated using the error amplifier and a few passive components.

For this example, a Type III, or three-pole-two-zero approach gives optimal bandwidth and phase.

In most voltage mode compensation schemes, including Type III, a single pole is placed at the origin to boost DC gain as high as possible. Two zeroes f_{Z1} and f_{Z2} are placed at the double pole frequency to cancel the double pole phase lag. Then, a pole, f_{P1} is placed at the frequency of the ESR zero. A final pole f_{P2} is placed at one-half of the switching frequency. The gain of the error amplifier transfer function is selected to give the best bandwidth possible without violating the Nyquist stability criteria. In practice, a good crossover point is one-fifth of the switching frequency, or 60 kHz for this example. The generic equation for the error amplifier transfer function is:

$$G_{EA} = A_{EA} \times \frac{\left(\frac{s}{2\pi f_{Z1}} + 1\right)\left(\frac{s}{2\pi f_{Z2}} + 1\right)}{s\left(\frac{s}{2\pi f_{P1}} + 1\right)\left(\frac{s}{2\pi f_{P2}} + 1\right)}$$

(22)

In this equation the variable A_{EA} is a ratio of the values of the capacitance and resistance of the compensation components, arranged as shown in Figure 27. A_{EA} is selected to provide the desired bandwidth. A starting value of 80,000 for A_{EA} should give a conservative bandwidth. Increasing the value will increase the bandwidth, but will also decrease phase margin. Designs with 45-60° are usually best because they represent a good trade-off between bandwidth and phase margin. In general, phase margin is lowest and gain highest (worst-case) for maximum input voltage and minimum output current. One method to select A_{EA} is to use an iterative process beginning with these worst-case conditions.

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1. Increase A_{EA}
2. Check overall bandwidth and phase margin
3. Change V_{IN} to minimum and recheck overall bandwidth and phase margin
4. Change I_O to maximum and recheck overall bandwidth and phase margin

The process ends when the both bandwidth and the phase margin are sufficiently high. For this example input voltage can vary from 3.0 to 3.6V and output current can vary from 0 to 4A, and after a few iterations a moderate gain factor of 101 dB is used.

The error amplifier of the LM10520 has a unity-gain bandwidth of 9 MHz. In order to model the effect of this limitation, the open-loop gain can be calculated as:

$$OPG = \frac{2\pi \times 9\ MHz}{s} \tag{23}$$

The new error amplifier transfer function that takes into account unity-gain bandwidth is:

$$H_{EA} = \frac{G_{EA} \times OPG}{1 + G_{EA} + OPG} \tag{24}$$

The gain and phase of the error amplifier are shown in Figure 29.

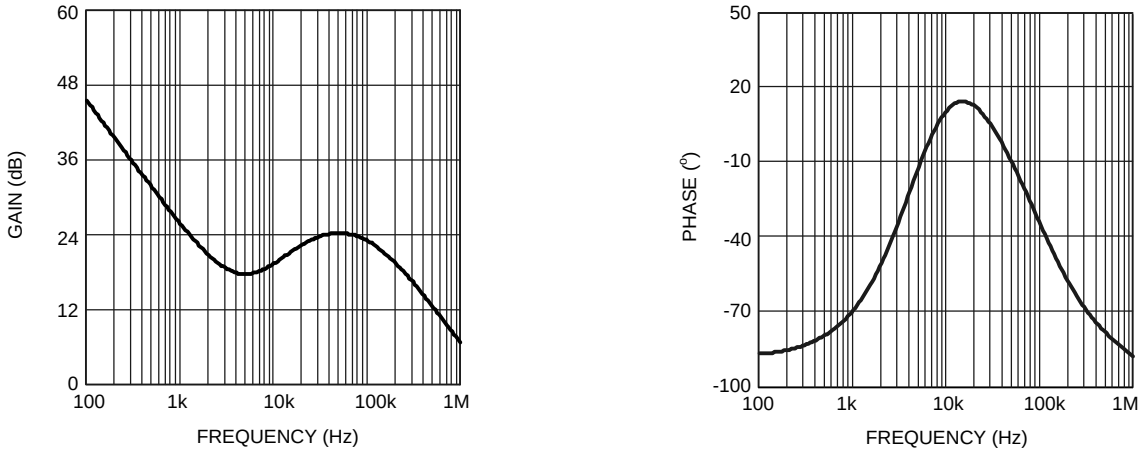


Figure 29. Error Amp. Gain and Phase

In VM regulators, the top feedback resistor R_{FB2} forms a part of the compensation. Setting R_{FB2} to 10 kΩ±1%, usually gives values for the other compensation resistors and capacitors that fall within a reasonable range. (Capacitances > 1pF, resistances < 1MΩ) C_{C1}, C_{C2}, C_{C3}, R_{C1}, and R_{C2} are selected to provide the poles and zeroes at the desired frequencies, using the following equations:

$$C_{C1} = \frac{f_{Z1}}{A_{EA} \times 10{,}000 \times f_{P2}} = 27\ pF \tag{25}$$

$$C_{C2} = \frac{1}{A_{EA} \times 10{,}000} - C_{C1} = 882\ pF \tag{26}$$

$$C_{C3} = \frac{1}{2\pi \times 10{,}000} \times \left(\frac{1}{f_{Z2}} - \frac{1}{f_{P1}}\right) = 2.73\ nF \tag{27}$$

$$R_{C1} = \frac{1}{2\pi \times C_{C2} \times f_{Z1}} = 39.8\ k\Omega \tag{28}$$

$$R_{C2} = \frac{1}{2\pi \times C_{C3} \times f_{P1}} = 2.55\ k\Omega \tag{29}$$

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In practice, a good tradeoff between phase margin and bandwidth can be obtained by selecting the closest ±10% capacitor values above what are suggested for C_{C1} and C_{C2}, the closest ±10% capacitor value below the suggestion for C_{C3}, and the closest ±1% resistor values below the suggestions for R_{C1}, R_{C2}. Note that if the suggested value for R_{C2} is less than 100Ω, it should be replaced by a short circuit. Following this guideline, the compensation components will be:

C_{C1} = 27 pF±10%, C_{C2} = 820 pF±10%

C_{C3} = 2.7 nF±10%, R_{C1} = 39.2 kΩ±1%

R_{C2} = 2.55 kΩ±1%

The transfer function of the compensation block can be derived by considering the compensation components as impedance blocks Z_F and Z_I around an inverting op-amp:

$$G_{EA\text{-}ACTUAL} = \frac{Z_F}{Z_I} \tag{30}$$

$$Z_F = \frac{\frac{1}{sC_{C1}} \times \left(10{,}000 + \frac{1}{sC_{C2}}\right)}{10{,}000 + \frac{1}{sC_{C1}} + \frac{1}{sC_{C2}}} \tag{31}$$

$$Z_I = \frac{R_{C1}\left(R_{C2} + \frac{1}{sC_{C3}}\right)}{R_{C1} + R_{C2} + \frac{1}{sC_{C3}}} \tag{32}$$

As with the generic equation, $G_{EA\text{-}ACTUAL}$ must be modified to take into account the limited bandwidth of the error amplifier. The result is:

$$H_{EA} = \frac{G_{EA\text{-}ACTUAL} \times OPG}{1 + G_{EA\text{-}ACTUAL} + OPG} \tag{33}$$

The total control loop transfer function H is equal to the power stage transfer function multiplied by the error amplifier transfer function.

$$H = G_{PS} \times H_{EA} \tag{34}$$

The bandwidth and phase margin can be read graphically from Bode plots of H_{EA} as shown in Figure 30.

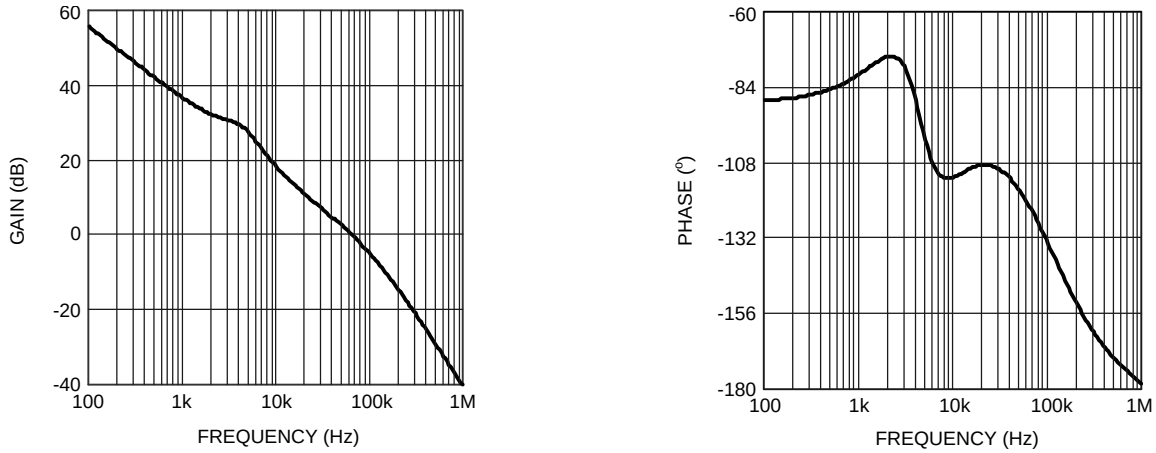


Figure 30. Overall Loop Gain and Phase

The bandwidth of this example circuit is 59 kHz, with a phase margin of 60°.

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EFFICIENCY CALCULATIONS

The following is a sample calculation.

A reasonable estimation of the efficiency of a switching buck controller can be obtained by adding together the Output Power (P_{OUT}) loss and the Total Power (P_{TOTAL}) loss:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{TOTAL}} \times 100\% \quad (35)$$

The Output Power (P_{OUT}) for the Typical Application Circuit design is (1.2V x 4A) = 4.8W. The Total Power (P_{TOTAL}), with an efficiency calculation to complement the design, is shown below.

The majority of the power losses are due to the low side and high side MOSFET's losses. The losses in any MOSFET are group of switching (P_{SW}) and conduction losses (P_{CND}).

$P_{FET} = P_{SW} + P_{CND} = 61.38\ mW + 270.42\ mW$

$P_{FET} = 331.8\ mW$ (36)

FET Switching Loss (P_{SW})

$P_{SW} = P_{SW(ON)} + P_{SW(OFF)}$

$P_{SW} = 0.5 \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}$

$P_{SW} = 0.5 \times 3.3V \times 4A \times 300\ kHz \times 31\ ns$

$P_{SW} = 61.38\ mW$ (37)

The FDS6898A has a typical turn-on rise time t_r and turn-off fall time t_f of 15 ns and 16 ns, respectively. The switching losses for this type of dual N-Channel MOSFETs are 0.061W.

FET Conduction Loss (P_{CND})

$P_{CND} = P_{CND1} + P_{CND2}$

$P_{CND1} = I^2_{OUT} \times R_{DS(ON)} \times k \times D$

$P_{CND2} = I^2_{OUT} \times R_{DS(ON)} \times k \times (1\text{-}D)$

$R_{DS(ON)}$ = 13 mΩ and the factor is a constant value (k = 1.3) to account for the increasing $R_{DS(ON)}$ of a FET due to heating.

$P_{CND1} = (4A)^2 \times 13\ m\Omega \times 1.3 \times 0.364$

$P_{CND2} = (4A)^2 \times 13\ m\Omega \times 1.3 \times (1 - 0.364)$

$P_{CND} = 98.42\ mW + 172\ mW = 270.42\ mW$ (38)

There are few additional losses that are taken into account:

IC Operating Loss (P_{IC})

$P_{IC} = I_{Q_VCC} \times V_{CC}$

where

- $I_{Q\text{-}VCC}$ is the typical operating V_{CC} current

P_{IC}= 1.7 mA x 3.3V = 5.61 mW (39)

FET Gate Charging Loss (P_{GATE})

$P_{GATE} = n \times V_{CC} \times Q_{GS} \times f_{SW}$

$P_{GATE} = 2 \times 3.3V \times 3\ nC \times 300\ kHz$

$P_{GATE} = 5.94\ mW$ (40)

The value n is the total number of FETs used and Q_{GS} is the typical gate-source charge value, which is 3 nC. For the FDS6898A the gate charging loss is 5.94 mW.

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Input Capacitor Loss (P_{CAP})

$$P_{CAP} = \frac{(I_{RMS_RIP})^2 \times ESR}{n^2}$$

where

- $I_{RMS_RIP} = I_{OUT} \times \sqrt{D(1 - D)}$ (41)

Here n is the number of paralleled capacitors, ESR is the equivalent series resistance of each, and P_{CAP} is the dissipation in each. So for example if we use only one input capacitor of 24 mΩ.

$$P_{CAP} = \frac{(1.924A)^2 \times 24\ m\Omega}{1^2}$$

$$P_{CAP} = 88.8\ mW \quad (42)$$

Output Inductor Loss (P_{IND})

$$P_{IND} = I^2_{OUT} \times DCR$$

where

- DCR is the DC resistance

Therefore, for example

$$P_{IND} = (4A)^2 \times 11\ m\Omega$$

$$P_{IND} = 176\ mW \quad (43)$$

Total System Efficiency

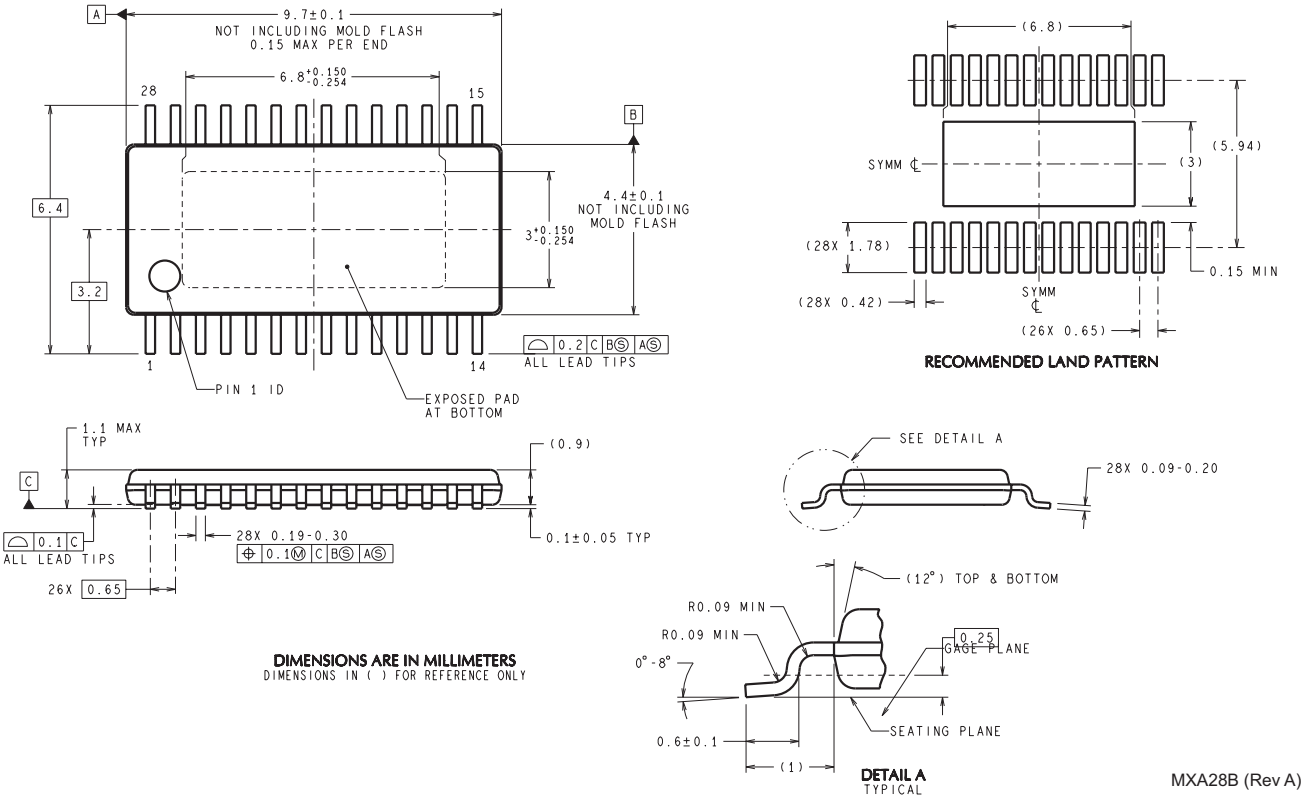
$$P_{TOTAL} = P_{FET} + P_{IC} + P_{GATE} + P_{CAP} + P_{IND} \quad (44)$$

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{TOTAL}} \times 100\% \quad (45)$$

$$V_{OUT} = V_{FB} \times \frac{(R_{FB1} + R_{FB2})}{R_{FB1}} \quad (46)$$

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PWP0028B



MXA28B (Rev A)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10520MH/NOPB	NRND	HTSSOP	PWP	28	48	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 125	LM10520	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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