Noritake itron

RoHS 2002/95/EC

VACUUM FLUORESCENT DISPLAY

MODULE

SPECIFICATION

MODEL : CU20049-UW2J

REVISION : F-1

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This specification is subject to change without prior notice.

This product complies with RoHS Directive 2002/95/EC

1. General Description

1.1 Application: Readout of computer, micro-computer, communication terminal and automatic instruments.

1.2 Construction: Single board display module consists of 80 characters (4 x 20) VFD, a controller which includes character generator ROM, and RAM, and a DC/DC converter.

1.3 Scope: Interface level is TTL-8/4 bit parallel and CMOS synchronous serial.
+5V single power supply is required.

1.4 Weight: About 155 g

2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Power Supply Voltage	V_{CC}	0	—	5.5	V_{DC}	—
Logic Input Voltage	V_I	0	—	V_{CC}+0.3	V_{DC}	—

3. Electrical Ratings
Measuring Conditions : TA (Ambient temperature)=25 degree

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Input Voltage DB0-DB7, RS, R/$\overline{W}$($\overline{WR}$), E($\overline{RD}$), SCK, STB	"H"	V_{IH1}	2.0	–	V_{CC}	V_{DC}	V_{CC} – V_{SS} = 5.0V
	"L"	V_{IL1}	V_{SS}	–	0.8		
Logic Input Voltage SI/SO	"H"	V_{IH2}	0.7V_{CC}	–	V_{CC}	V_{DC}	V_{CC} – V_{SS} = 5.0V
	"L"	V_{IL2}	V_{SS}	–	0.3V_{CC}		
Power supply Voltage		V_{CC}-V_{SS}	4.75	5.00	5.25	V_{DC}	–

4. Electrical Characteristics
Measuring Conditions: TA (Ambient temperature)=25degree, V_{CC}=5.0V_{DC}

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Output Voltage	"H"	V_{OH}	V_{CC}-0.8	_	–	V_{DC}	I_{OH} = -4 mA
	"L"	V_{OL}	–	_	0.6		I_{OL} = 4 mA
	"H"	V_{OH}	V_{CC}-0.5	_	–	V_{DC}	I_{OH} = -2 mA
	"L"	V_{OL}	–	_	0.5		I_{OL} = 2 mA
Power Supply Current 1		I_{CC1}	–	650	850	mA	Display ON
Power Supply Current 2		I_{CC2}	–	8	15	mA	Display OFF
Power Consumption			–	3.25	4.25	W	Display ON

Note: I_{CC1} shows the current, when all dots are turned on.
Slow rise up power supply may cause a failure of Power-on reset which is explained in "8.2 Power-on reset". Less than 50 ms power rising time is recommended.
I_{CC} might be anticipated twice as usual at power on rush.

5. Optical Specifications

Number of characters	:	80 (4 lines x 20 chars)
Matrix format	:	5 x 8 dot
Display area	:	99.6 x 37.6 mm (X x Y)
Character size	:	3.65 x 8.8 mm (X x Y)
Character pitch	:	5.05 x 9.6 mm (X x Y)
Dot size	:	0.57 x 0.84 mm (X x Y)
Dot pitch	:	0.77 x 1.14 mm (X x Y)
Luminance	:	Min. 350 cd/m^2
Color of illumination	:	Green (Blue-green)

6. Environmental Specifications

Operating temperature	:	-40 to +85 degree
Storage temperature	:	-50 to +85 degree
Operating humidity	:	20 to 80 % RH (Non condensation)
Vibration (Non operation)	:	10 to 55 to 10 Hz (Frequency) 1.0 mm (Total Amplitude) 30 min. (Duration) X, Y, Z each direction
Shock (Non operation)	:	539 m/S^2, 10mS

7. Functional Descriptions

7.1. Instruction table

Instruction	CODE										Time	Description
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display clear	0	0	0	0	0	0	0	0	0	1	100 μs MAX.	Clears all display and Sets DD RAM address 0 in the address counter.
Cursor Home	0	0	0	0	0	0	0	0	1	*	666 ns	Sets DD RAM address 0 in the address counter. Also returns the display being shifted to the original position. DD RAM contents remain unchanged.
Entry Mode set	0	0	0	0	0	0	0	1	I/D	S	666 ns	Sets the cursor direction and specifies display shift. These operations are performed during writing/reading data.
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	666 ns	Sets all display ON/OFF (D), cursor ON/OFF (C), cursor blink of character position (B).
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	666 ns	Shifts display or cursor, keeping DDRAM contents.
Function Set	0	0	0	0	1	IF	*	*	*	*	666 ns	Sets data length (IF).
Brightness control	1	0	*	*	*	*	*	*	BR1	BR0	666 ns	Accepts 1 byte data of just after “Function set” as brightness control data.

Instruction	CODE										Time	Description
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
CG RAM address setting	0	0	0	1	ACG						666 ns	Sets the CG RAM address.
DD RAM address Setting	0	0	1	ADD							666 ns	Sets the DD RAM address.
Busy flag & address reading	0	1	BF	ACC							666 ns	Reads busy flag (BF) and address counter.
Data writing to CG or DD RAM	1	0	Data writing								666 ns	Writes data into CG RAM or DD RAM.
Data reading from CG or DD RAM	1	1	Data reading								666 ns	Reads data from CG RAM or DD RAM.
	I/D = 1 : Increment I/D = 0 : Decrement S = 1 : Display shift enabled S = 0 : Cursor shift enabled S/C = 1 : Display shift S/C = 0 : Cursor move R/L = 1 : Shift to the right R/L = 0 : Shift to the left BR1,BR0 = 00 : 100% 01 : 75% 10 : 50% 11 : 25%						IF = 1 : 8-bits IF = 0 : 4-bits BF = 1 : Busy BF = 0 : Not busy					DD RAM: Display data RAM CG RAM: Character generator RAM ACG: CG RAM address ADD: DD RAM address ACC: Address Counter

Note:

* : Don’t care.

7.2. Display Clear

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	01H

RS = 0

This instruction

1. Fills all location in the display data (DD) RAM with 20H (Blank character).
2. Clears the contents of the address counter to 0H.
3. Sets the display for zero character shift.
4. Sets the address counter to point to the DD RAM.
5. If the cursor is displayed, moves the cursor to the left most character in the top line (Line 1).
6. Sets the address counter to increment on each access of DD RAM or CG RAM.

7.3. Cursor Home

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	1	*	02H to 03H

RS = 0

*: Don't care

This instruction
1. Clears the contents of the address counter to 0H.
2. Sets the address counter to point to the DD RAM.
3. Sets the display for zero character shift.
4. If the cursor is displayed, moves the left most character in the top line. (Line 1).

7.4. Entry Mode Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	1	I/D	S	04H to 07H

RS = 0

The I/D bit selects the way in which the contents of the address counter are modified after every access to DD RAM or CG RAM.
I/D = 1: The address counter is incremented.
I/D = 0: The address counter is decremented.

The S bit enables display shift, instead of cursor shift, after each write or read to the DD RAM.
S = 1 : Display shift enabled.
S = 0 : Cursor shift enabled.

The direction in which the display is shifted is opposite in sense to that of the cursor. For example if S=0 and I/D=1, the cursor would shift one character to the right after a CPU writes to DD RAM. However if S=1 and I/D=1, the display would shift one character to the left and the cursor would maintain its position on the panel.

The cursor will already be shifted in the direction selected by I/D during reads of the DD RAM, irrespective of the value of S. Similarly reading and writing the CG RAM always shifts the cursor. Also both lines are shifted simultaneously.

I/D	S	After writing DD RAM data	After reading DD RAM data
0	0	The cursor moves one character to the left.	The cursor moves one character to the left.
1	0	The cursor moves one character to the right.	The cursor moves one character to the right.
0	1	The display shifts one character to the right without cursor's move.	The cursor moves one character to the left.
1	1	The display shifts one character to the left without cursor's move.	The cursor moves one character to the right.

7.5. Display ON/OFF

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	D	C	B	08H to 0FH

RS = 0

This instruction controls various features of the display.
The D bit turns the entire display on or off.
D = 1 : Display on
D = 0 : Display off
Note : When display is turned off, power converter is also inhibited and reduces power consumption.

The C bit turns the cursor on or off.
C = 1 : Cursor on
C = 0 : Cursor off

The B bit enables blinking of the character the cursor coincides with.
B = 1 : Blinking on
B = 0 : Blinking off

Blinking is achieved by alternating between a normal and all on display of a character.
The cursor blinks with a frequency of about 1 Hz and DUTY 50%.

7.6. Cursor/Display shift

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	S/C	R/L	*	*	10H to 1FH

RS = 0

*: Don’t care

This instruction shifts the display and/or moves the cursor, on character to the left or right, without reading nor writing DD RAM.
The S/C bit selects movement of the cursor or movement of both the cursor and the display.
S/C = 1 : Shift both cursor and display.
S/C = 0 : Shift cursor only.
The R/L bit selects leftward or rightward movement of the display and/or cursor.
R/L = 1 : Shift one character right.
R/L = 0 : Shift one character left.

Cursor move and Display shift by the “Cursor/Display Shift”.

S/C	R/L	Cursor shift	Display shift
0	0	Move one character to the left	No shift
0	1	Move one character to the right	No shift
1	0	Shift one character to the left with display	Shift one character to the left
1	1	Shift one character to the right with display	Shift one character to the right

7.7. Function Set

This command sets width of data bus line by itself, and sets screen brightness by following one byte data.

7.7.1. Function Set Command

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	IF	*	*	*	*	20H to 3FH

RS = 0

*: Don't care

This instruction initializes the system, and must be the first instruction executed after power-on.
The IF bit selects between an 8-bit or a 4-bit bus width interface.

IF = 1 : 8-bit CPU interface using DB7 to DB0
IF = 0 : 4-bit CPU interface using DB7 to DB4

When serial interface is selected, IF=1.

7.7.2. Brightness Control

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
*	*	*	*	*	*	BR1	BR0	00H to 03H

RS = 1

*: Don't care

One byte data (RS = 1) which follows the "Function Set Command" is considered as brightness data. When a command (RS = 0) is written after the "Function Set Command", the brightness control function is not initiated. Screen brightness is as follows;

BR1	BR0	Brightness
0	0	100 % (Default)
0	1	75 %
1	0	50 %
1	1	25 %

7.8. Set CG RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	ACG						40H to 7FH

RS = 0

This instruction
1. Loads a new 6-bit address into the address counter.
2. Sets the address counter to address CG RAM.

Once the "Sets CG RAM Address" has been executed, the contents of the address counter will be automatically modified after every access of CG RAM, as determined by the "7.4 Entry Mode Set" instruction. The active width of the address counter, when it is addressing CG

RAM, is 6-bits so the counter will wrap around to 00H from 3FH if more than 64 bytes of data are written to CG RAM.

7.9. Set DD RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	ADD						

RS = 0

80H to 93H (1 line), C0H to D3H (2 line), 94H to A7H (3 line), D4H to E7H (4 line)

This instruction
1. Loads a new 7-bit address into the address counter.
2. Sets the address counter to point to the DD RAM.

Once the “Set DD RAM Address” instruction has been executed, the contents of the address counter will be automatically modified after each access of DD RAM, as selected by the “7.4 Entry Mode Set” instruction.

Valid DD RAM Address Ranges

	Number of Characters	Address
1st line	20	00H to 13H
2nd line	20	40H to 53H
3rd line	20	14H to 27H
4th line	20	54H to 67H

7.10. Write Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
DATA WRITE								00H to FFH

RS = 1

This instruction writes the data in DB7 to DB0 into either the CG RAM or the DD RAM.
The RAM space (CG or DD), and the address in that space, that is accessed depends on whether a “Set CG RAM Address” or “Set DD RAM Address” instruction was last executed, and on the parameters of that instruction. The contents of the address counter will be automatically modified after each “Write Data”, as determined by the “7.4 Entry Mode Set”. When data is written to the CG RAM, the DB7, DB6 and DB5 bits are not displayed as characters.

7.11. Read Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DATA READ							

RS = 1

This instruction reads data from either CG RAM or DD RAM, depending on the type of “Set RAM Address” instructions last sent. The address in that space depends on the “Set RAM Address” instruction parameters. Immediately before executing “Read Data”, “Set CG RAM Address” or “Set DD RAM Address” must be executed. The contents of the address counter are modified after each “Read Data”, as determined by the “7.4 Entry Mode Set”. Display shift is not executed, as described at of the “7.4 Entry Mode Set”.

7.12. Read Busy Flag/Address Counter

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BF	ACC						

RS = 0

Reading the instruction register yields the current value of the address counter and the busy flag. This instruction must be executed prior to any other instructions. ACC, the address counter value, will point to a location in either CG RAM or DD RAM, depending on the type of “Set RAM Address” instruction last sent.
In “Busy Flag Check” immediately after executing “Write Data” instruction, a valid address counter value can be ready as soon as BF goes low. The BF bit shows the status of the busy flag.

BF = 1 : busy.
BF = 0 : ready for next instruction, command receivable.

8. Other features

8.1. CG RAM

The display module has CG RAM of 320 bit = (5x8 bit /char) x 8 chars which is for user definable character fonts. The character fonts consists of 5x7 dots with underline. The number 1-36 corresponds to character fonts.

Character code	CG RAM address						CG RAM data (character pattern)							
	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
00H or (08H)	0	0	0	0	0	0	*	*	*	1	2	3	4	5
	0	0	0	0	0	1	*	*	*	6	7	8	9	10
	0	0	0	0	1	0	*	*	*	11	12	13	14	15
	0	0	0	0	1	1	*	*	*	16	17	18	19	20
	0	0	0	1	0	0	*	*	*	21	22	23	24	25
	0	0	0	1	0	1	*	*	*	26	27	28	29	30
	0	0	0	1	1	0	*	*	*	31	32	33	34	35
	0	0	0	1	1	1	*	*	*	0	0	36	0	0
01H or (09H)	0	0	1	0	0	0	*	*	*	1	2	3	4	5
	0	0	1	0	0	1	*	*	*	6	7	8	9	10
	0	0	1	0	1	0	*	*	*	11	12	13	14	15
	0	0	1	0	1	1	*	*	*	16	17	18	19	20
	0	0	1	1	0	0	*	*	*	21	22	23	24	25
	0	0	1	1	0	1	*	*	*	26	27	28	29	30
	0	0	1	1	1	0	*	*	*	31	32	33	34	35
	0	0	1	1	1	1	*	*	*	0	0	36	0	0

REMARKS; " * ": Don't care " 0 ": Turned off " 1 ": Turned on

Dot assignment

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25
26	27	28	29	30
31	32	33	34	35
		36		

Remarks: The 36th dot is five.
Use those dots as underline.

8.2. Power-on reset

Internal status of the module is initialized, when the controller detects the rising of power supply up. The status are as follows:

1. Display clear
   Fills the DD RAM with 20Hex (Space code).
   During executing of " Display Clear " (Max 100 μs), the busy flag (BF) is "1".

2. Sets the address counter to 0H.
   Sets the address counter to point the DD RAM.

3. Display ON/OFF
   D = 0 : display OFF
   C = 0 : Cursor OFF
   B = 0 : Blink OFF

4. Entry Mode Set
   I/D = 1 : Increment (+1)
   S = 0 : No display shift

5. Function Set
   IF = 1 : 8-bit interface

6. Brightness Control
   BR0 = BR1 =0 : 100%

·Remarks
   There is a possibility that reset doesn't work by slow start power supply.
   Therefore the initializing by commands needs.

8.3. CPU interface

The display module is capable to select some interfaces such as parallel (i80 or M68, 8-bit or 4-bit) or serial.

8.3.1. Select CPU

The module is able to select to parallel or serial data transfer by setting JP7 jumper, and to connect to bus of i80 type or M68 type CPU by setting JP2 jumper. Refer to " 8.4 Jumper" for detail.

8.3.2. 4-bit CPU interface

If 4-bit interface is used, the 8-bit instruction are written nibble by nibble: the high-order nibble being written first, followed by low-order nibble. It is not necessary to check the busy flag between writing separate nibbles of individual instructions.

See " 7.7.1 Function Set Command " for more information.

8.3.3 Serial data transfer

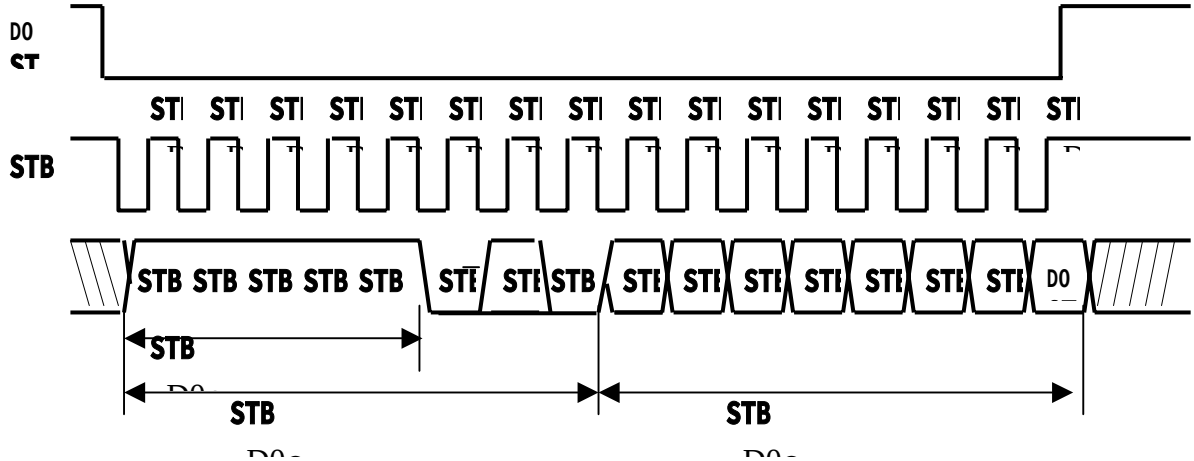
Serial data can be inputted when the Strobe goes to “0”.

Serial data consists of 2 bytes. The first byte (Start Byte) consists of a total of 8 bits: the Synchronous bits (bit1-bit5), R/$\overline{W}$ (bit6), RS (bit7) and bit8. The register is selected (Instruction Register or Data Register) by the RS (bit7). RS is “0” in Instruction Register, and it is “1” in Data Register. The data write or read is selected by R/W (bit6). R/$\overline{W}$ is “0” when the data is written, and it is “1” when the data is read.

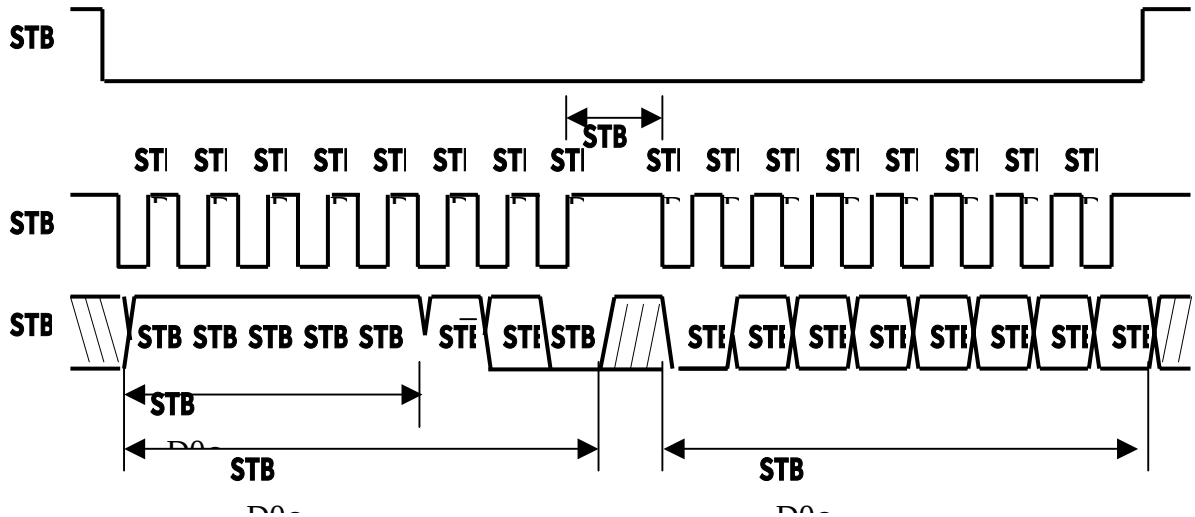
	0	1
R/$\overline{W}$	Data Write	Data Read
RS	Instruction Register	Data Register

In “Data Write”, the second byte (8-bit Instruction / Data Byte) is written after the Start Byte. On the other hand, the second byte is the read data in “Data Read”, such as the Busy Flag + Address Counter or the data written in the DD RAM or CG RAM. The read data is outputted at the falling edge of the shift clock.

<Data Write>



<Data Read>



8.4. Jumper

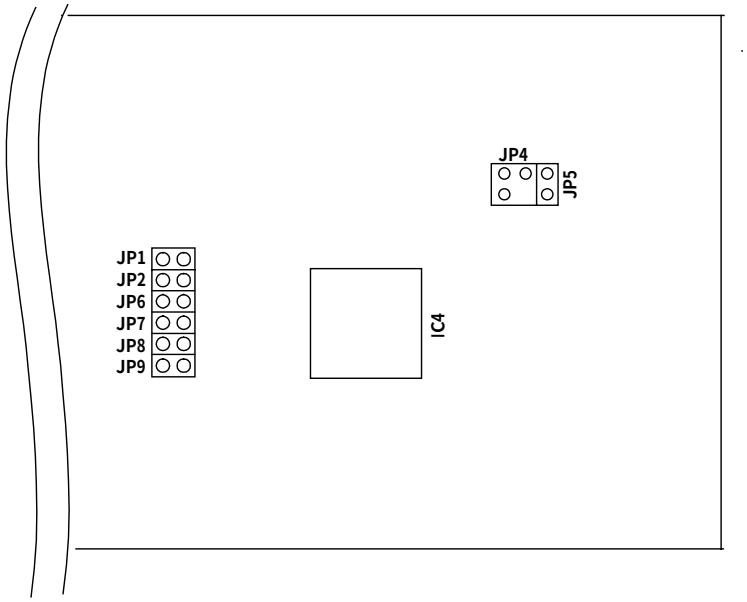
Some jumpers are prepared on the PCB board, to set operating mode of the display module. A soldering iron is required to short jumper.

No2 and No3 of jumper 'JP4' is used to reset of module.

You can reset the module by shorting No2 and No3 of the jumper 'JP4' for some interval which is longer than 10us.

The following figure shows the location of each jumper.

Location:



The following table shows the function of No 1 and No 2 of JP4, JP2, JP7.

CU20049-UW2J is no reset inputs and M68 CPU bus parallel interface at default setting. Reset input signal is active when it is low.

Table of No 1 and No 2 of JP4 setting

No 1 and No 2 of JP4	No 3 of CN1 and No 6 of CN3
open	NC
short	$\overline{\text{RESET}}$

NC: no connection

Table of JP7 setting

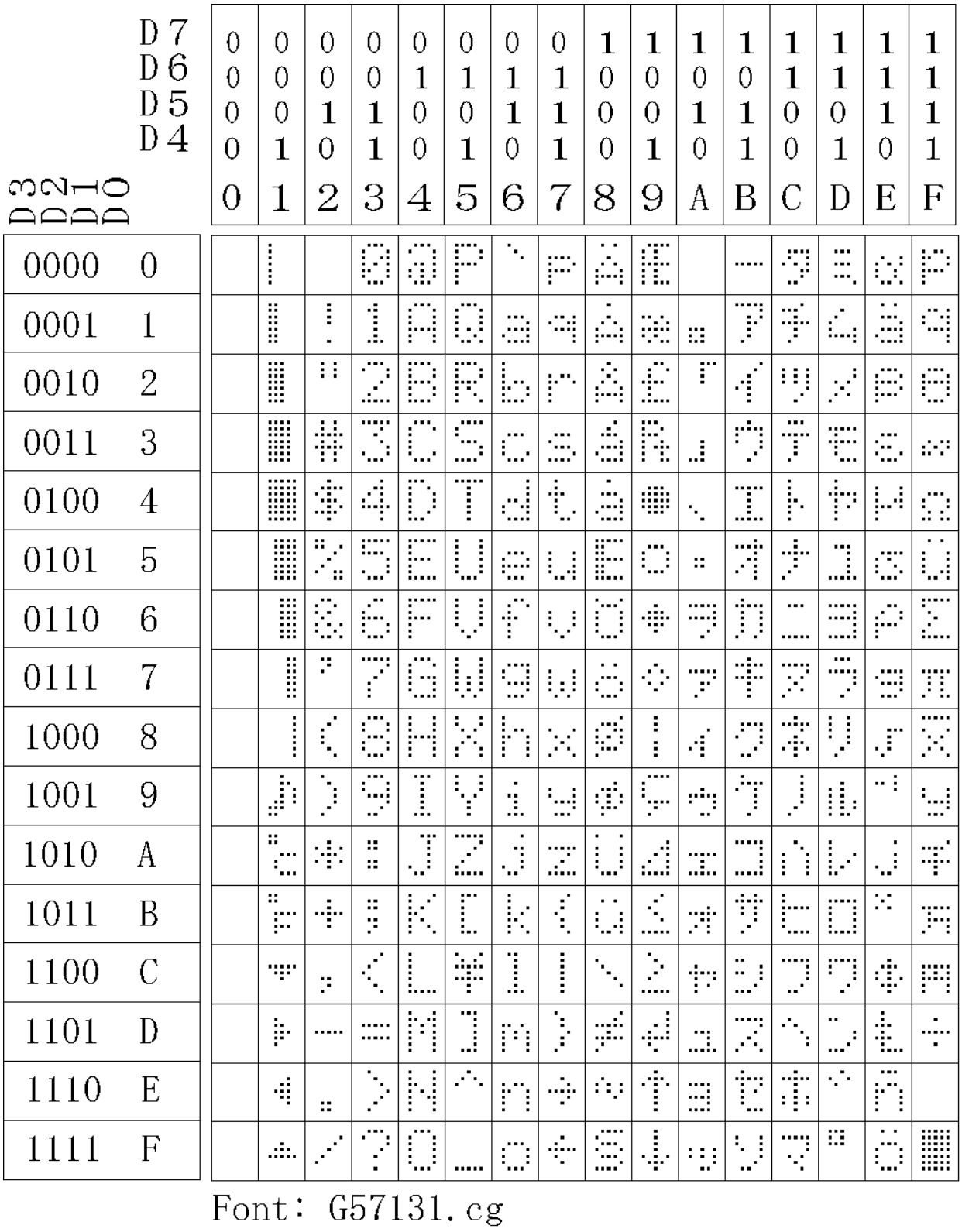
JP7	Interface
Open	Parallel interface
Short	Serial interface

Table of JP2 setting

JP2	CPU bus mode	Control signals
open	M68 type	E,R/$\overline{\text{W}}$
short	i80 type	$\overline{\text{WR}}$, $\overline{\text{RD}}$

JP1, JP3,JP5,JP6,JP8 and JP9 are factory use only.

9. Character Font

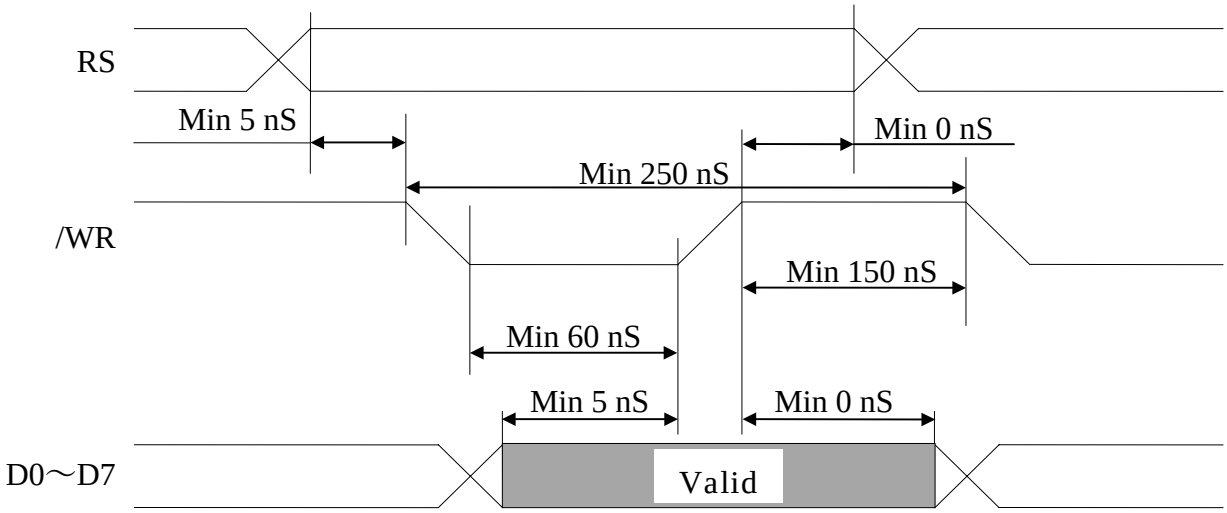


Note: Font number 00-07Hex (08-0FHex) is User Definable Character Fonts.

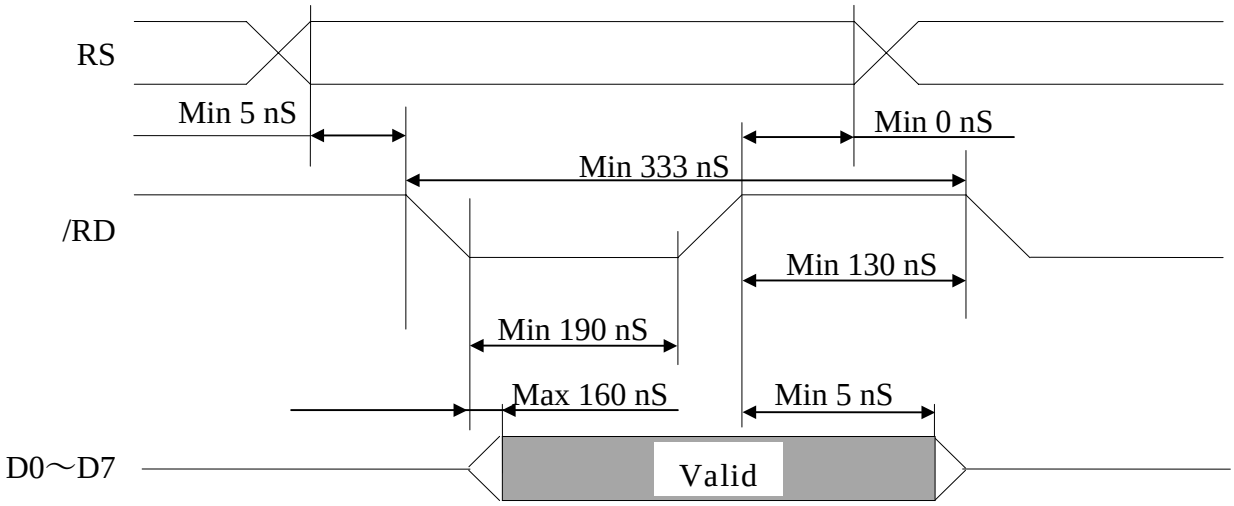
10. Timing

Input signal rise time and fall time < 15 ns.

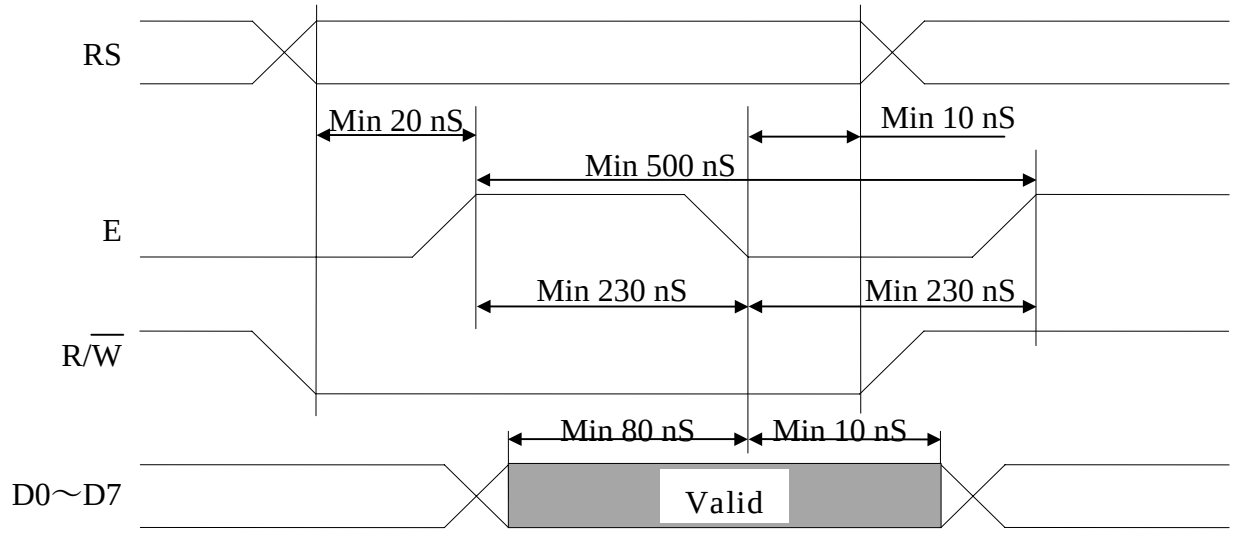
10.1. CPU bus write timing (Parallel interface i80 type)



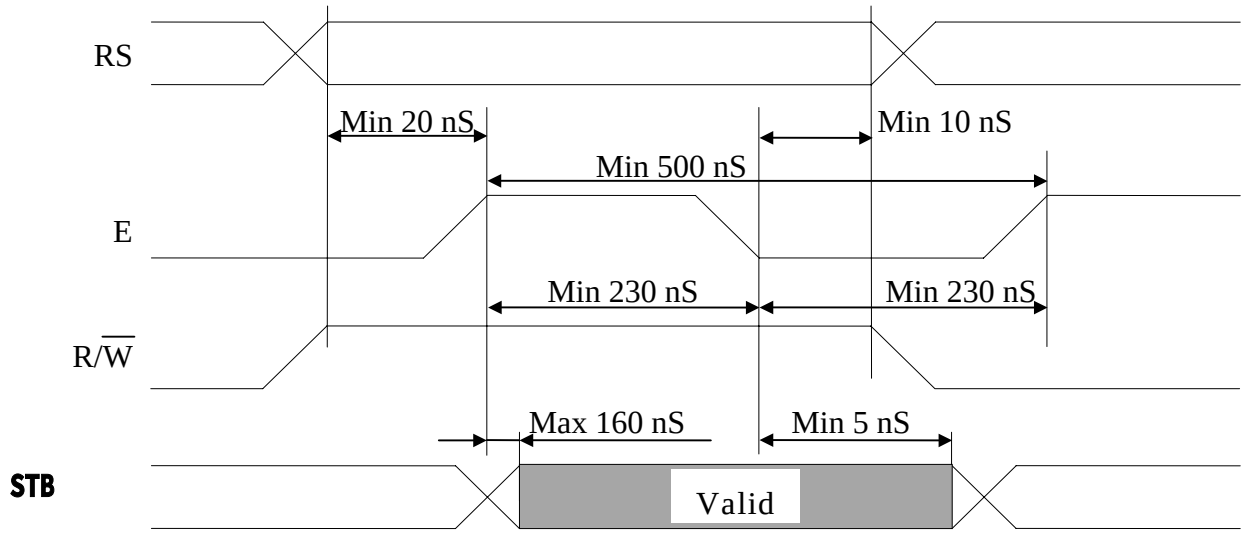
10.2. CPU bus read timing (Parallel interface i80 type)



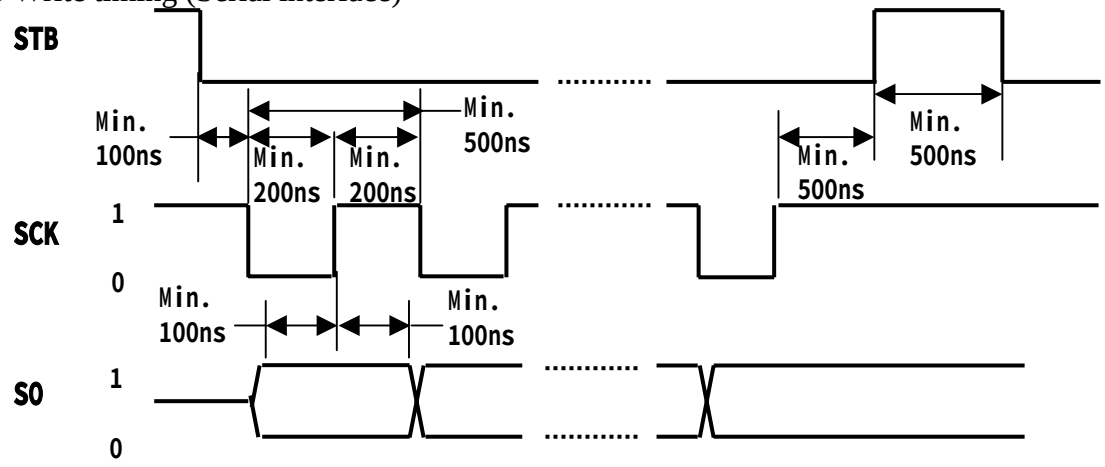
10.3. CPU bus write timing (Parallel interface M68 type)



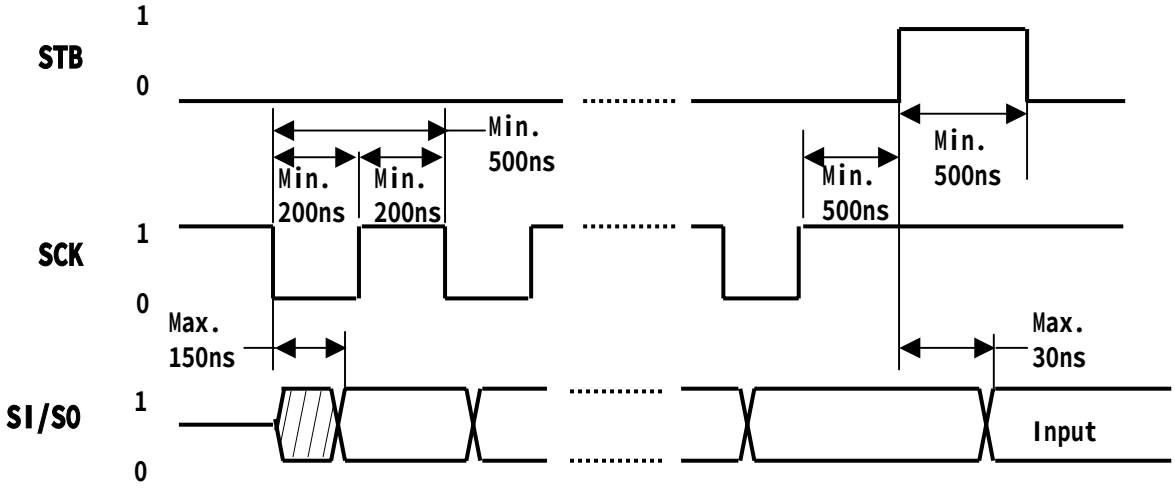
10.4. CPU bus read timing (Parallel interface M68 type)



10.5 Write timing (Serial interface)



10.6 Read timing (Serial interface)



11. Connector Pin assignment

The through holes are prepared for power supply and data communications.
A connector or pins may be able to solder to the holes.

Diameter of holes is 1.0mm.

11.1. 14pin Connector (CN1) for parallel interface

Pin No.	Signal name	Function	Direction
1	GND	Ground	Input
2	VCC	Power supply	Input
3	NC	Non connection	-
4	RS	Switch signal	Input
5	R/$\overline{W}$($\overline{WR}$)	Data transfer select (Write enable)	Input
6	E($\overline{RD}$)	Write enable (Read enable)	Input
7	DB0	Data input	Input/Output
8	DB1	Data input	Input/Output
9	DB2	Data input	Input/Output
10	DB3	Data input	Input/Output
11	DB4	Data input	Input/Output
12	DB5	Data input	Input/Output
13	DB6	Data input	Input/Output
14	DB7	Data input	Input/Output

NC: no connection

The third through hole is for reset input when No 1 and No 2 of JP4 are short.

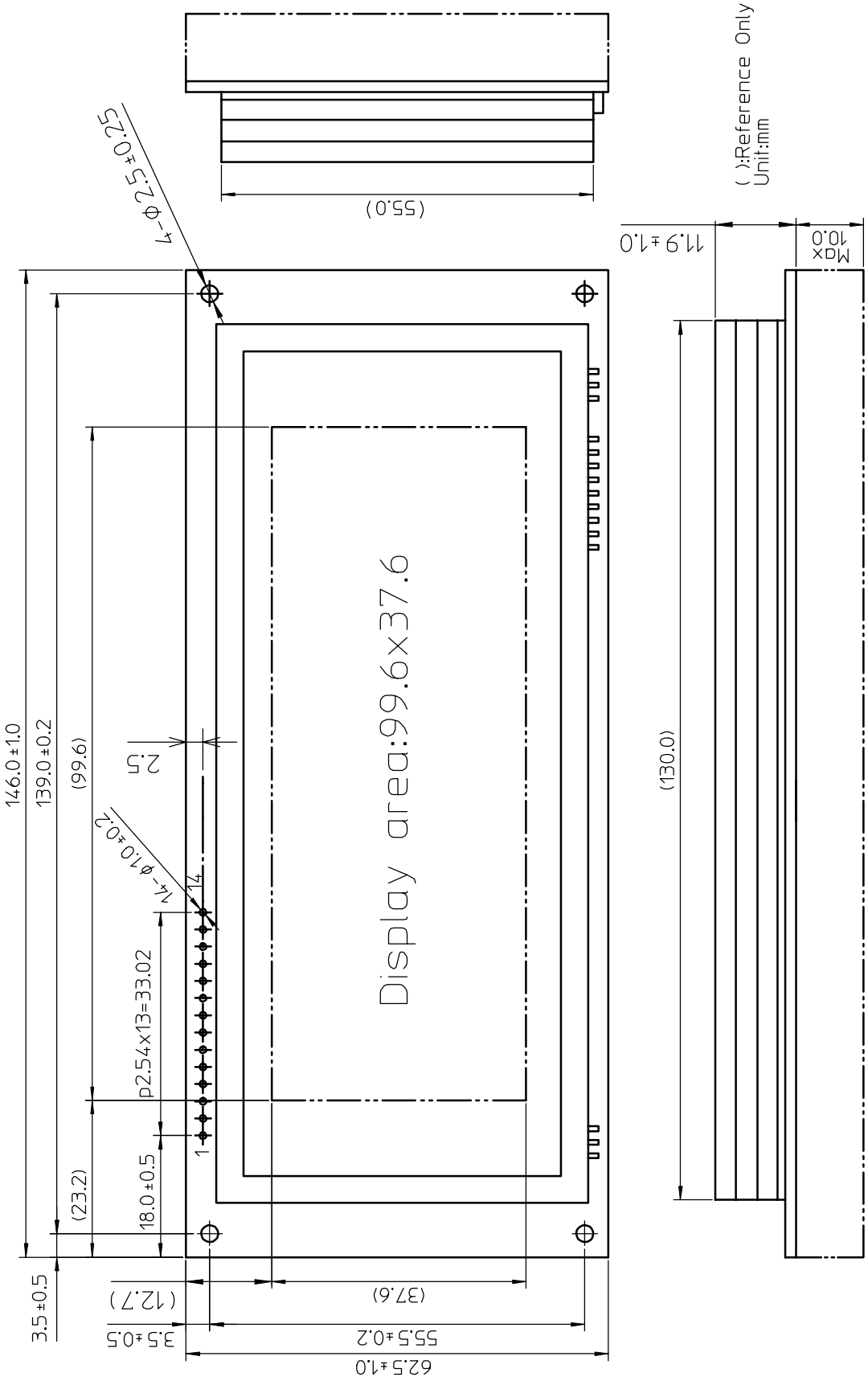
11.2 6pin Connector (CN3) for serial interface

Pin No.	Signal name	Function	Direction
1	VCC	Power supply	Input
2	SI/SO	Data input/output	Input/Output
3	GND	Ground	Input
4	STB	Strobe	Input
5	SCK	Display clock	Input
6	NC	Non connection	-

NC: no connection

The 6th through hole is for reset input when No 1 and No 2 of JP4 are short.

12.Outline dimension



Notice for the Cautious Handling VFD Modules

Handling and Usage Precautions:
Please carefully follow the appropriate product application notes for proper usage, safety handling, and operation standards for maximum performance.

[VFD tubes are made of glass]
- Because the edges of the VFD glass-envelop are not smooth, it is necessary to handle carefully to avoid injuries to your hands
- Please avoid breaking the VFD glass-envelop to prevent injury from sharp glass particles.
- The tip of the exhaust pipe is fragile so avoid shock from impact.
- It is recommended to allow sufficient open space surrounding the exhaust pipe to avoid possible damage.
- Please design the PCB for the VFD-module within 0.3 mm warping tolerance to avoid any forces that may damage the display due to PCB distortion causing a breakdown of the electrical circuit leading to VFD failure.

[High voltage]
- Avoid touching conductive electrical parts, because the VFD-module uses high voltage exceeding 30～100 volts.
- Even when electric power is turned off, it may take more than one minute for the electrical current to discharge.

[Cable connection]
- Do not unplug the power and/or data cables of VFD-modules during operating condition because unrecoverable damage may result.
- Sending input signals to the VFD-module during a power off condition sometimes causes I/O port damage.
- It is recommended to use a 30 cm or shorter signal cable to prevent functional failures.

[Electrostatic charge]
- VFD-modules needs electrostatic free packaging and protection from electrostatic charges during handling and usage.

[Structure]
- During operation, VFD and VFD-modules generate heat. Please consider sufficient heat radiation dissipation using heat sink solutions.
- We prefer to use UL grade materials or components in conjunction with VFD-modules.
- Wrap and twist motion causes stress and may break VFDs & VFD modules. Please adhere to allowances within 0.3mm at the point of attachment.

[Power]
- Apply regulated power to the VFD-module within specified voltages to protect from failures.
- Because some VFD-modules may consume in rush current equal to twice the typical current at power-on timing, we recommend using a sufficient power capability and quick starting of the power regulator.
- VFD-module needs a specified voltage at the point of connection. Please use an adequate power cable to avoid a decrease in voltage. We also recommend inserting a power fuse for extra protection.

[Operating consideration]
- Illuminating phosphor will decrease in brightness during extended operation. If a fixed pattern illuminates for an extended period,(several hours), the phosphor efficiency will decrease compared to the non operating phosphor causing a non uniform brightness among pixels. Please consider programming the display patterns to use all phosphor segments evenly. Scrolling may be a consideration for a period of time to refresh the phosphor condition and improve even illumination to the pixels.
- We recommend using a signal cable 30cm or less to avoid some possible disturbances to the signal.

[Storage and operating environment]
- Please use VFD-modules under the recommended specified environmental conditions. Salty, sulfur and dusty environments may damage the VFD-module even during storage.

[Discard]
- Some VFDs contain a small amount of cadmium in the phosphor and lead in the solder. When discarding VFDs or VFD-modules, please adhere to governmental related laws or regulations.

[Others]
- Although the VFD-module is designed to be protected from electrical noise, please plan your circuitry to exclude as much noise as possible.
- Do not reconstruct or repair the VFD-module without our authorization. We cannot assure the quality or reliability of unauthorized reconstructed VFD-modules.

Notice:
・We do not authorize the use of any patents that may be inherent in these specifications.
・Neither whole nor partial copying of these specifications are permitted without our approval.
If necessary , please ask for assistance from our sales consultant.
・This product is not designed for military, aerospace, medical or other life-critical applications. If you choose to use this product for these applications, please ask us for prior consultation or we cannot take responsibility for problems that may occur.