Product Specification

PE42359

SPDT UltraCMOS® RF Switch
10 MHz–3 GHz

Features

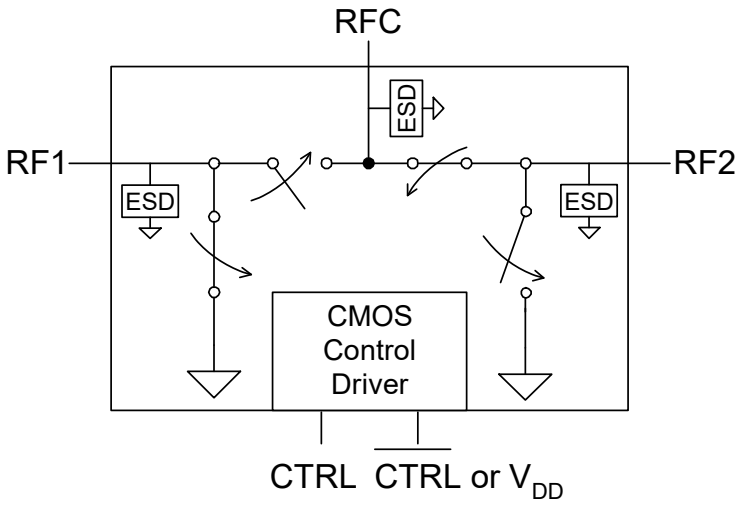
- AEC-Q100 Grade 2 certified
- Supports operating temperature up to +105 °C
- Single-pin or complementary CMOS logic control inputs
- Low insertion loss
  - 0.35 dB @ 1000 MHz
  - 0.50 dB @ 2000 MHz
- Isolation of 30 dB @ 1000 MHz
- High ESD tolerance of 2 kV HBM
- Typical input 1 dB compression point of +33.5 dBm
- 1.8V minimum power supply voltage

Product Description

The PE42359 UltraCMOS® RF switch is designed to cover a broad range of applications from 10 MHz through 3 GHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface, and can be controlled using either single-pin or complementary control inputs. Using a nominal +3-volt power supply voltage, a typical input 1 dB compression point of +33.5 dBm can be achieved. PE42359 also meets the quality and performance standards for automotive applications and has received AEC-Q100 Grade 2 certification.

The PE42359 is manufactured on pSemi's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration

Figure 1. Functional Diagram



DOC-02109

Figure 2. Package Type
6-lead SC-70



©2012-2023 pSemi Corporation All rights reserved.

Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3.0V (Z_S = Z_L = 50Ω)

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency[1]		10		3000	MHz
Insertion loss[2]	10–1000 MHz 1000–2000 MHz 2000–3000 MHz[2]		0.35 0.50 1.1	0.45 0.60 1.3	dB dB dB
Isolation (RFX–RFX)	10–1000 MHz 1000–2000 MHz 2000–3000 MHz	32 20 13	35 21 14		dB dB dB
Isolation (RFC–RFX)	10–1000 MHz 1000–2000 MHz 2000–3000 MHz	28 19 12	29 20 13		dB dB dB
Return loss (RFX–RFC)[2]	10–1000 MHz 1000–2000 MHz 2000–3000 MHz[2]	21 15 9	25 18 11		dB dB dB
Switching time	50% CTRL to 90% or 10% RF		2		µs
Video feedthrough[3]			15		mV_{pp}
Input 1 dB compression point	1000 MHz @ 2.3–3.3V 1000 MHz @ 1.8–2.3V 2500 MHz @ 2.3–3.3V 2500 MHz @ 1.8–2.3V	31.5 29.5 28.5 28	33.5 30.5 30.5 29		dBm
Input IP3	2500 MHz, 20 dBm input power		55		dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.
2. High frequency performance can be improved by external matching (see *Figure 20–Figure 25* and *Figure 28*).
3. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50Ω test set-up, measured with 1 ns rise time pulses and 500 MHz bandwidth.

Table 1A. Electrical Specifications @ –40 °C to +105 °C, V_{DD} = 3.0V (Z_S = Z_L = 50Ω)

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency		10		3000	MHz
Insertion loss	10–1000 MHz 1000–2000 MHz 2000–3000 MHz		0.35 0.5 1.1	0.6 0.75 1.4	dB dB dB
Isolation (RFX–RFX)	10–1000 MHz 1000–2000 MHz 2000–3000 MHz	31 19 12	35 21 14		dB dB dB
Isolation (RFC–RFX)	10–1000 MHz 1000–2000 MHz 2000–3000 MHz	27 18 11	29 20 13		dB dB dB
Return loss (RFX–RFC)	10–1000 MHz 1000–2000 MHz 2000–3000 MHz	20 14 9	25 18 11		dB dB dB
Switching time	50% CTRL to 90% or 10% RF		3.6		µs
Video feedthrough			15		mV_{pp}
Input 1 dB compression point	1000 MHz @ 2.3–3.3V 1000 MHz @ 1.8–2.3V 2500 MHz @ 2.3–3.3V 2500 MHz @ 1.8–2.3V	30.5 28.5 27.5 27	33.5 30.5 30.5 29		dBm
Input IP3	2500 MHz, 20 dBm input power		54		dBm

©2012-2023 pSemi Corporation. All rights reserved.

Figure 3. Pin Configuration (Top View)

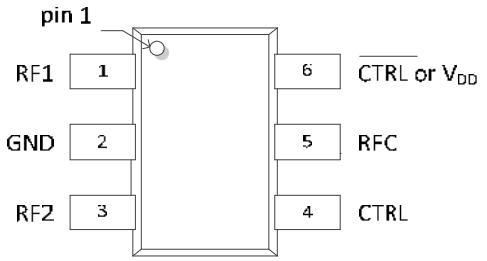


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	RF1*	RF port 1
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF2*	RF port 2
4	CTRL	Switch control input, CMOS logic level.
5	RFC*	RF common
6	$\overline{\text{CTRL}}$ or V_{DD}	This pin supports two interface options: *Single-pin control mode.* A nominal 3-volt supply connection is required. *Complementary-pin control mode.* A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode.

Note*: All RF pins must be DC blocked with an external series capacitor or held at 0 VDC.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Unit
Power supply voltage, V_{DD}	1.8	3.0	3.3	V
Power supply current, I_{DD} (+25 °C only)		9	20	µA
Control voltage high	0.7× V_{DD}			V
Control voltage low			0.3× V_{DD}	V

Moisture Sensitivity Level

The moisture sensitivity level rating for the

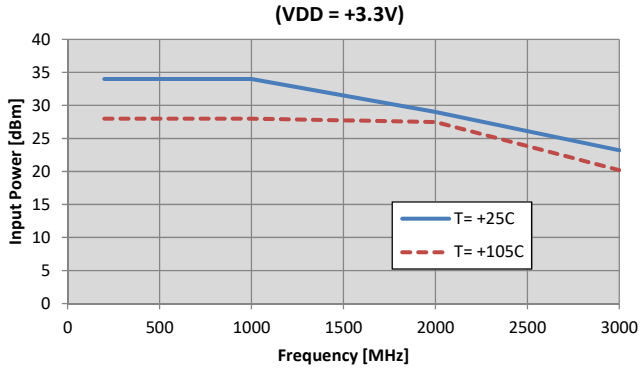
Table 4. Absolute Maximum Ratings

Parameter/Condition	Min	Max	Unit
Power supply voltage, V_{DD}	–0.3	4.0	V
Voltage on any DC input, V_I	–0.3	V_{DD}+ 0.3	V
Storage temperature range, T_{ST}	–65	150	°C
Operating temperature range, T_{OP}	–40	105	°C
Input power (50Ω), P_{IN}[1]		see *Figure 4*	
ESD voltage HBM[2], $V_{ESD,HBM}$, all pins		2000	V
ESD voltage CDM[3], $V_{ESD,CDM}$, all pins		1000	V

Notes: 1. To maintain optimum device performance, do not exceed max P_{IN} at desired operating frequency (see *Figure 4*).
2. Human body model (MIL–STD 883 Method 3015).
3. Charged device model (JEDEC JESD22–C101).

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended

Figure 4. Maximum Power Handling



Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

©2012-2023 pSemi Corporation. All rights reserved.

Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = High	RFC to RF1
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 ($\overline{CTRL}$ or V_{DD}) = Low Pin 4 (CTRL) = High	RFC to RF1
Pin 6 ($\overline{CTRL}$ or V_{DD}) = High Pin 4 (CTRL) = Low	RFC to RF2

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Switching Frequency

The PE42359 has a maximum 25 kHz switching rate.

Control Logic Input

The PE42359 is a versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 4) supporting a +3-volt CMOS logic input, and requires a dedicated +3-volt power supply connection on pin 6 (V_{DD}). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS μProcessor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins CTRL and $\overline{CTRL}$ (pins 4 and 6), that can be directly driven by +3-volt CMOS logic or a suitable μProcessor I/O port. This enables the PE42359 to be used as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE42359 operating limits.

©2012-2023 pSemi Corporation. All rights reserved.

Typical Performance Data @ +25 °C, V_{DD} = 3.0V unless otherwise specified.

Figure 5. Insertion Loss (RFX Nominal Condition)*

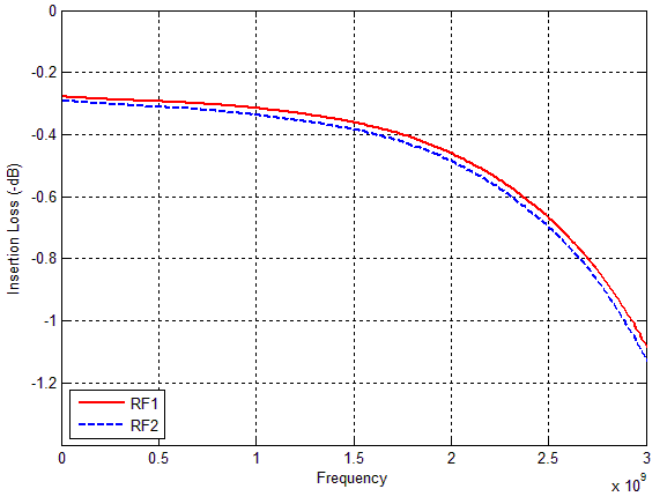


Figure 6. Insertion Loss vs Temp (RF1–RFC)*

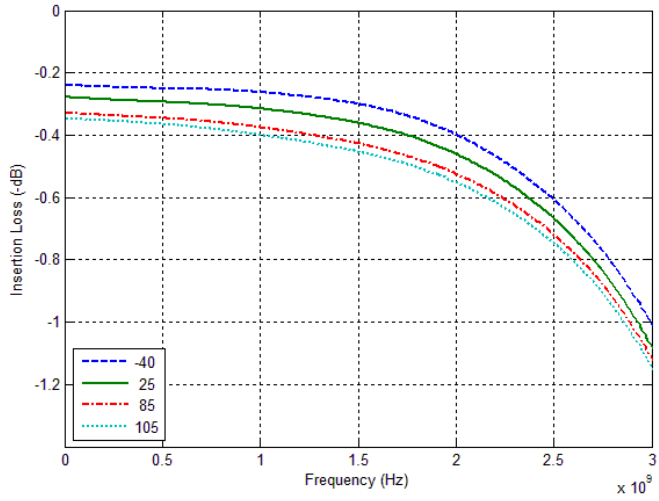
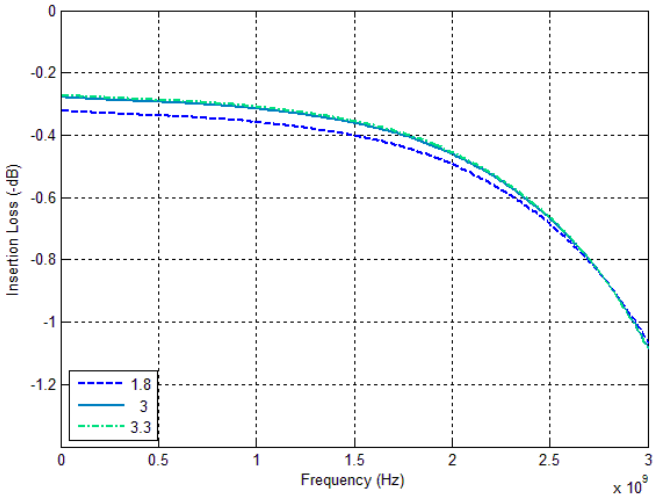


Figure 7. Insertion Loss vs V_{DD} (RF1–RFC)*



Note *: High frequency performance can be improved by external matching (see *Figure 20–Figure 25* and *Figure 28*).

©2012-2023 pSemi Corporation. All rights reserved.

Typical Performance Data @ +25 °C, V_{DD} = 3.0V unless otherwise specified.

Figure 8. RFC–RFX Isolation vs Temp

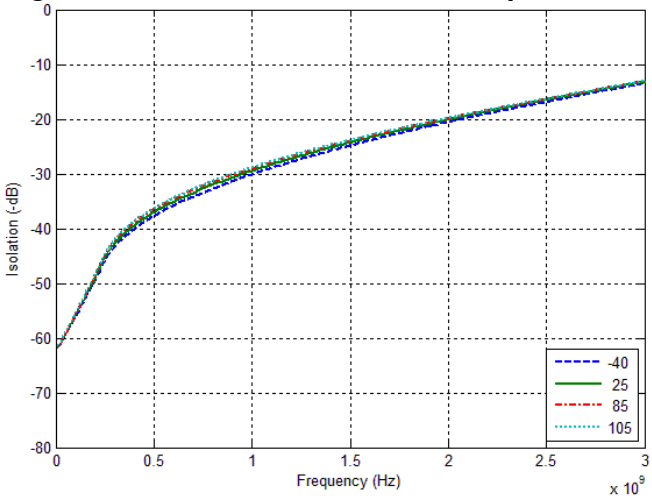


Figure 9. RFC–RFX Isolation vs V_{DD}

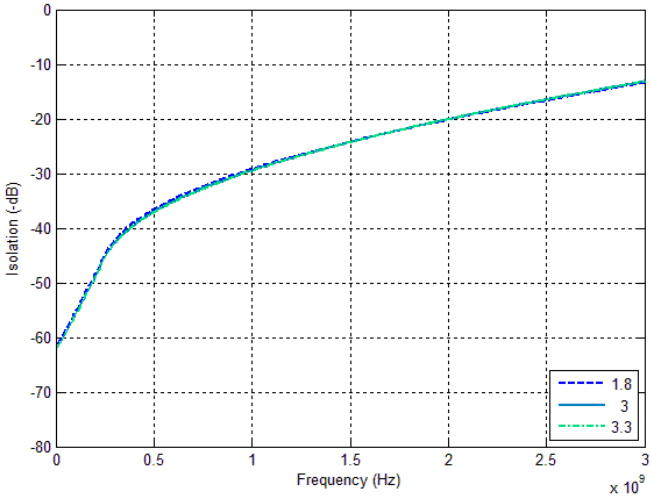


Figure 10. RFX–RFX Isolation vs Temp

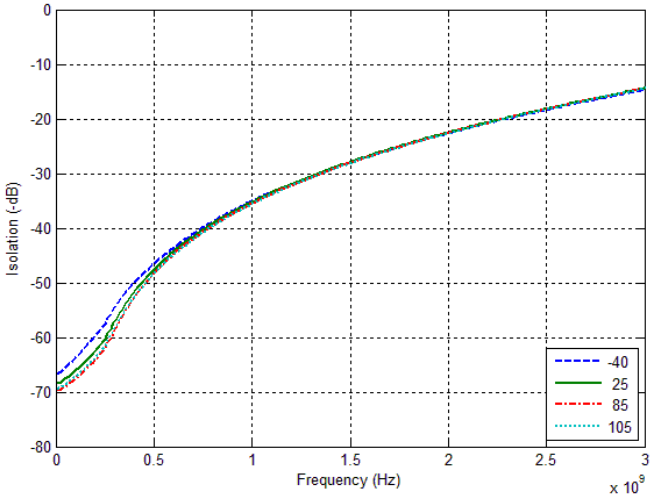
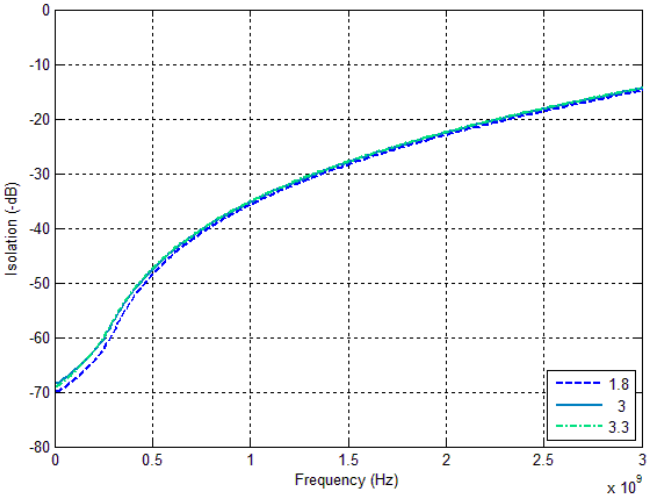


Figure 11. RFX–RFX Isolation vs V_{DD}



©2012-2023 pSemi Corporation. All rights reserved.

Typical Performance Data @ +25 °C, V_{DD} = 3.0V unless otherwise specified.

Figure 12. RFC Port Return Loss vs Temp (RF1 Active)*

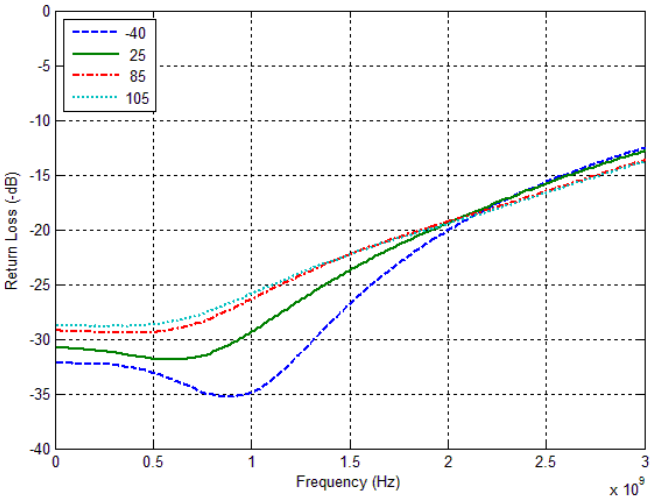


Figure 13. RFC Port Return Loss vs V_{DD} (RF1 Active)*

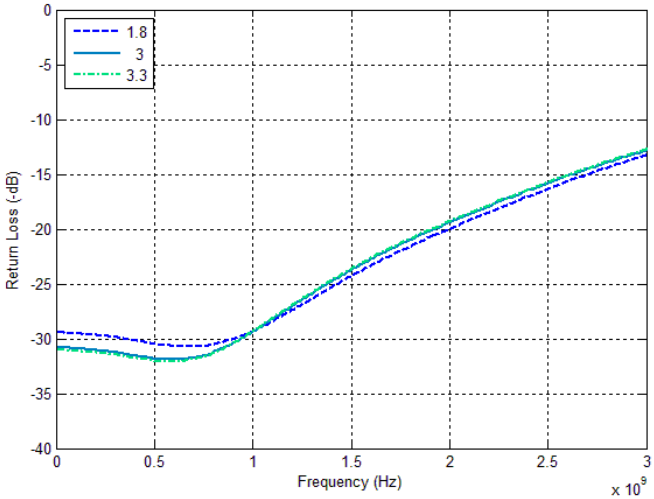


Figure 14. RFC Port Return Loss vs Temp (RF2 Active)*

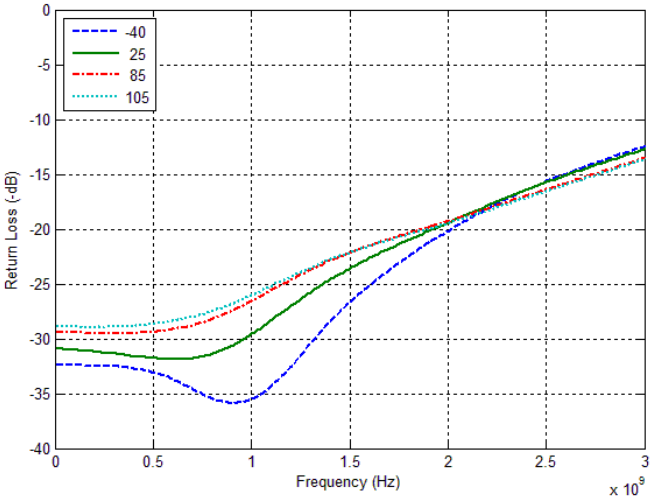
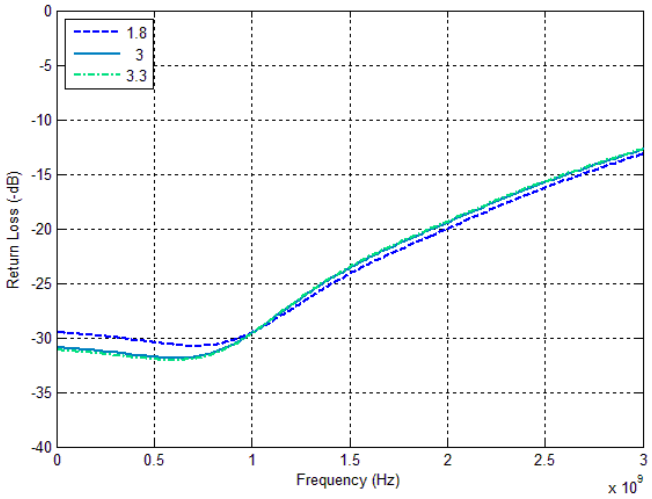


Figure 15. RFC Port Return Loss vs V_{DD} (RF2 Active)*



Note *: High frequency performance can be improved by external matching (see *Figure 20–Figure 25* and *Figure 28*).

©2012-2023 pSemi Corporation. All rights reserved.

Typical Performance Data @ +25 °C, V_{DD} = 3.0V unless otherwise specified.

Figure 16. Active Port Return Loss vs Temp (RF1 Active)*

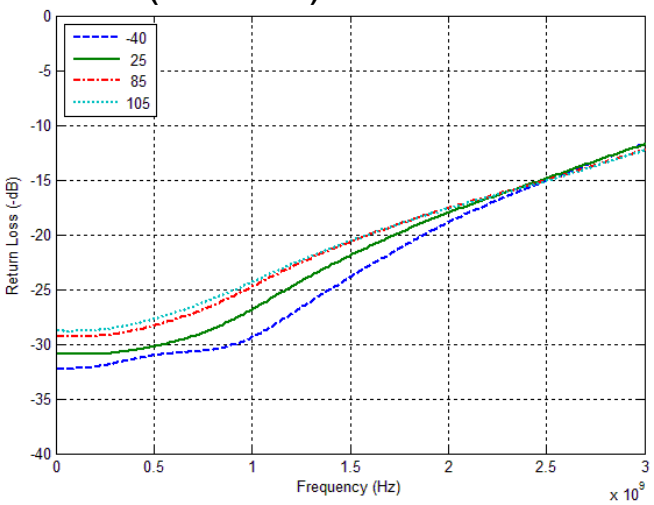


Figure 17. Active Port Return Loss vs V_{DD} (RF1 Active)*

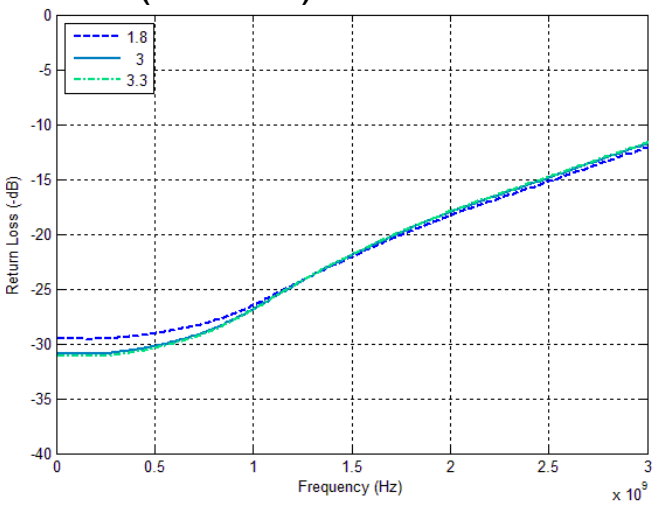


Figure 18. Active Port Return Loss vs Temp (RF2 Active)*

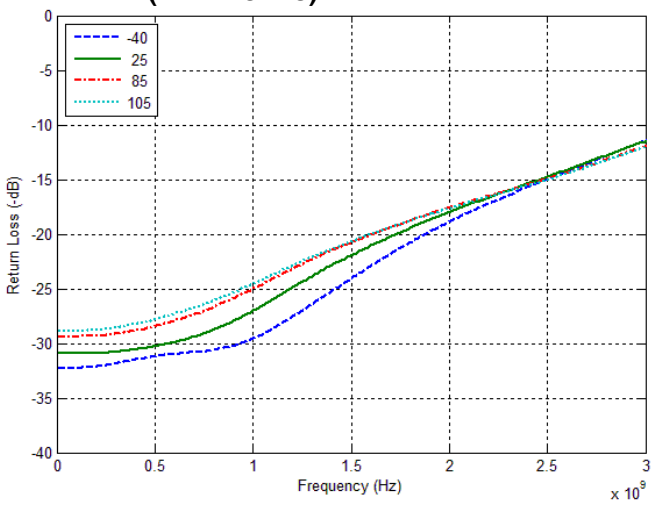
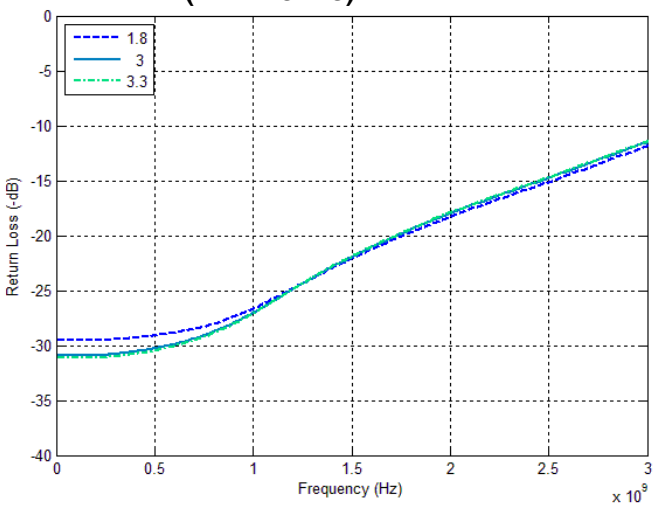


Figure 19. Active Port Return Loss vs V_{DD} (RF2 Active)*



Note *: High frequency performance can be improved by external matching (see *Figure 20–Figure 25* and *Figure 28*).

©2012-2023 pSemi Corporation. All rights reserved.

Performance Comparison @ +25 °C and V_{DD} = 3.0V, with or without matching.

Figure 20. Insertion Loss RF1*

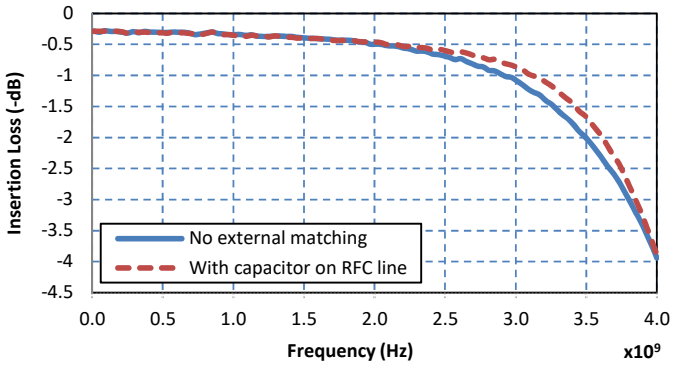


Figure 21. Insertion Loss RF2*

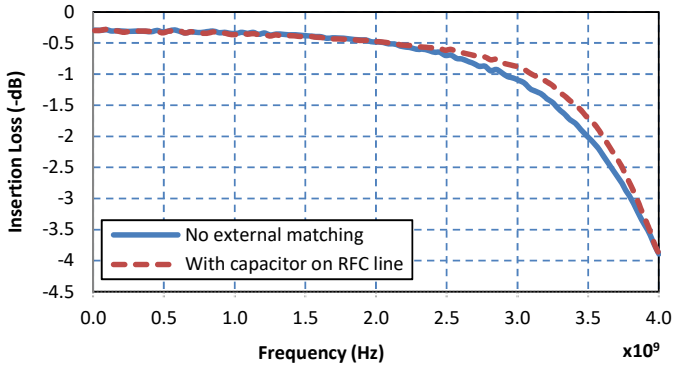


Figure 22. Active Port Return Loss (RF1 Active)*

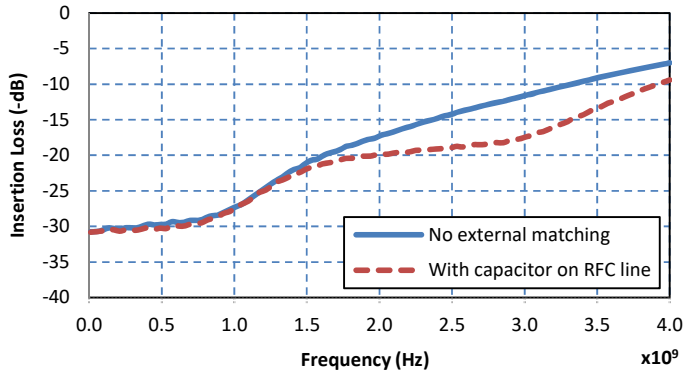


Figure 23. Active Port Return Loss (RF2 Active)*

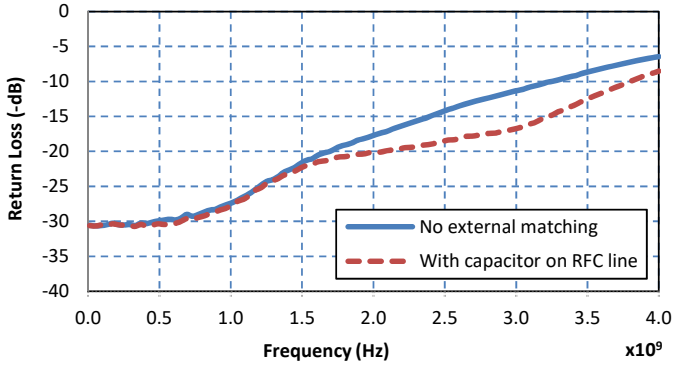


Figure 24. RFC Port Return Loss (RF1 Active)*

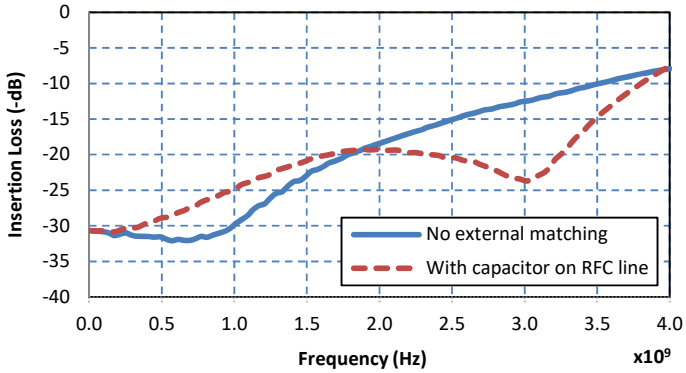
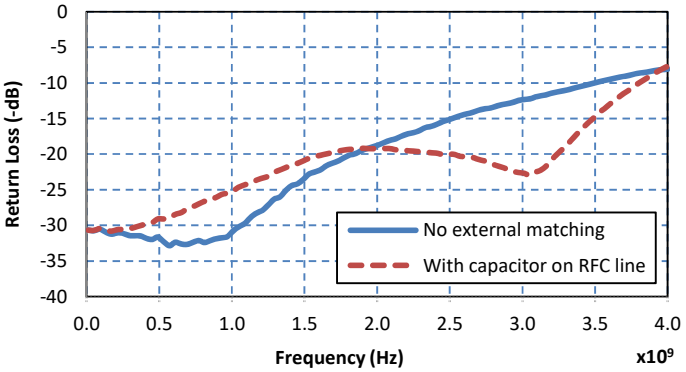


Figure 25. RFC Port Return Loss (RF2 Active)*



Note *: High frequency performance can be improved by external matching (see *Figure 20–Figure 25* and *Figure 28*).

©2012-2023 pSemi Corporation. All rights reserved.

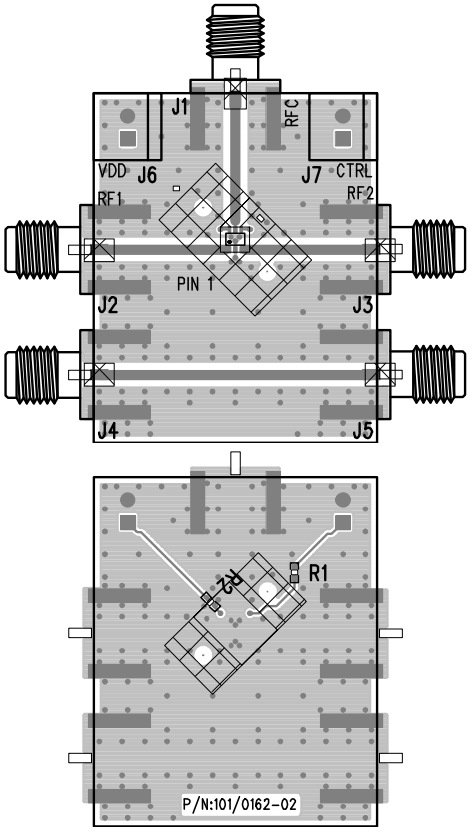
Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of pSemi's PE42359. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50Ω transmission is available via SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two-metal-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 and J7 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device V_{DD} or $\overline{CTRL}$ input. J7-1 is connected to the device CTRL input.

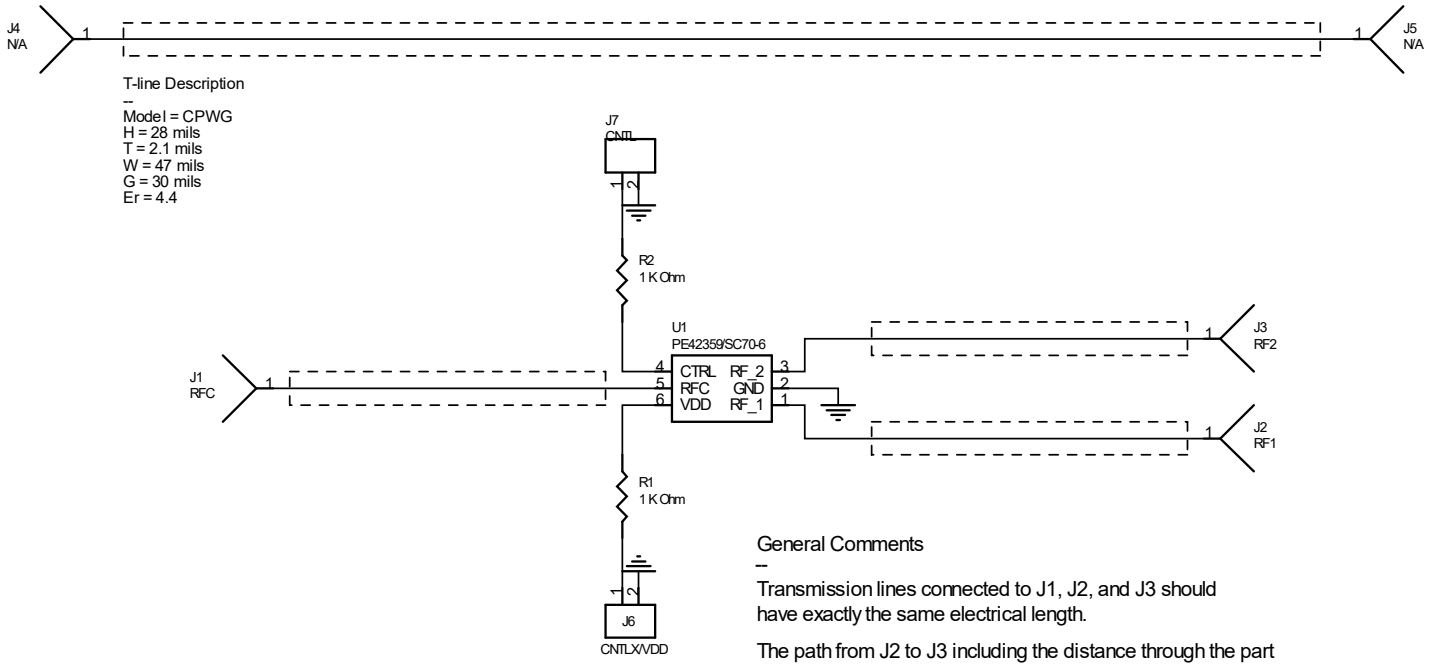
Figure 26. Evaluation Board Layout



PRT-53273

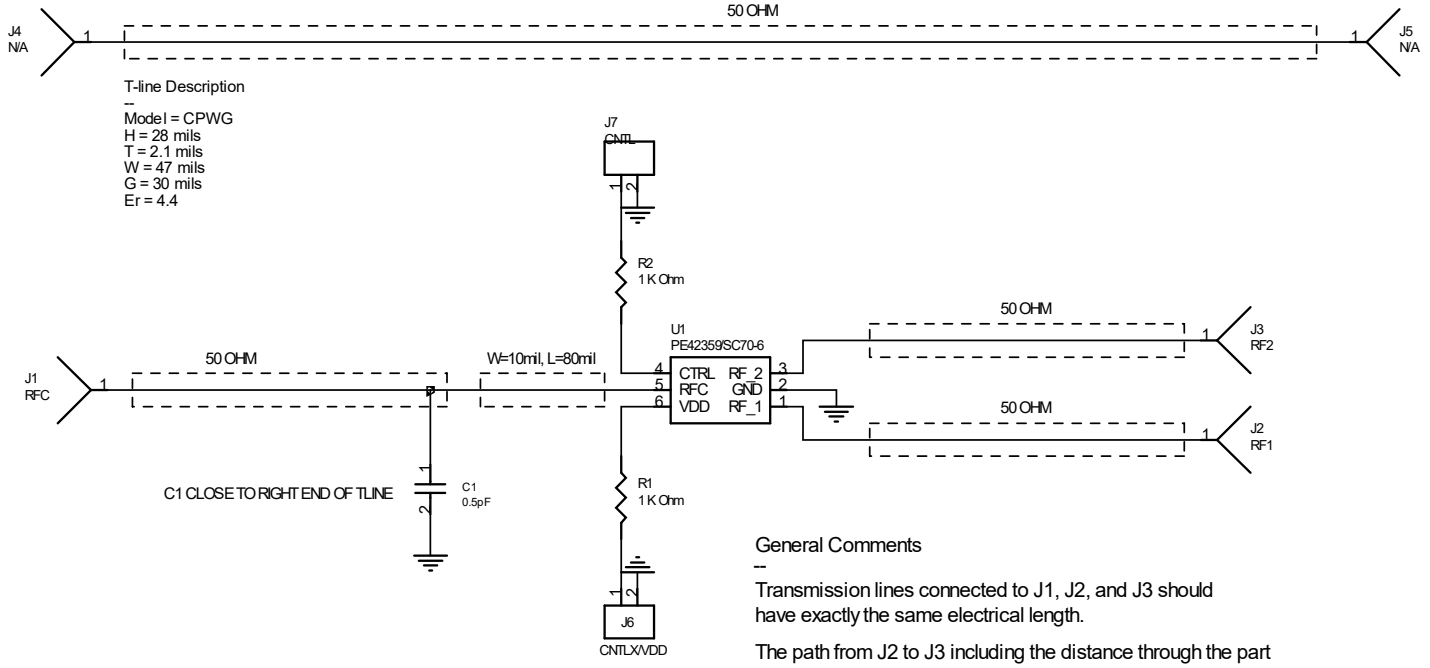
©2012-2023 pSemi Corporation. All rights reserved.

Figure 27. Evaluation Board Schematic



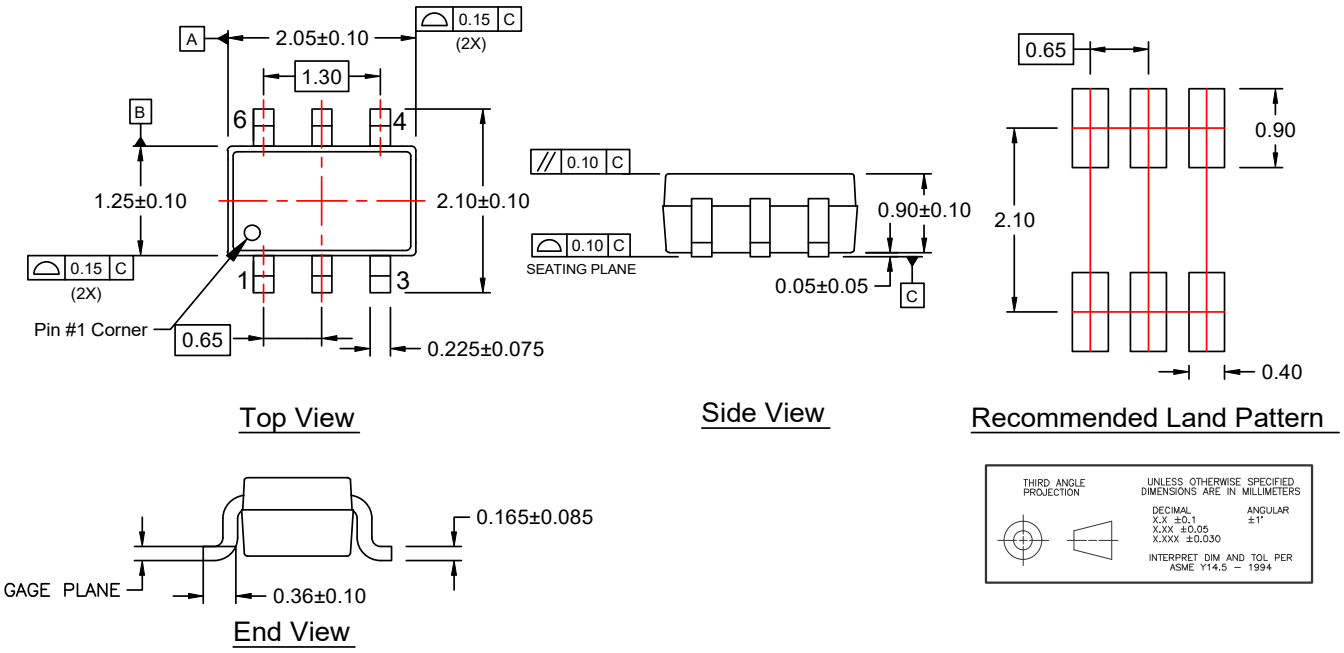
©2012-2023 pSemi Corporation. All rights reserved.

Figure 28. Evaluation Board Schematic with Matching



©2012-2023 pSemi Corporation. All rights reserved.

Figure 29. Package Drawing
6-lead SC-70



DOC-76316

Figure 30. Top Marking Specification

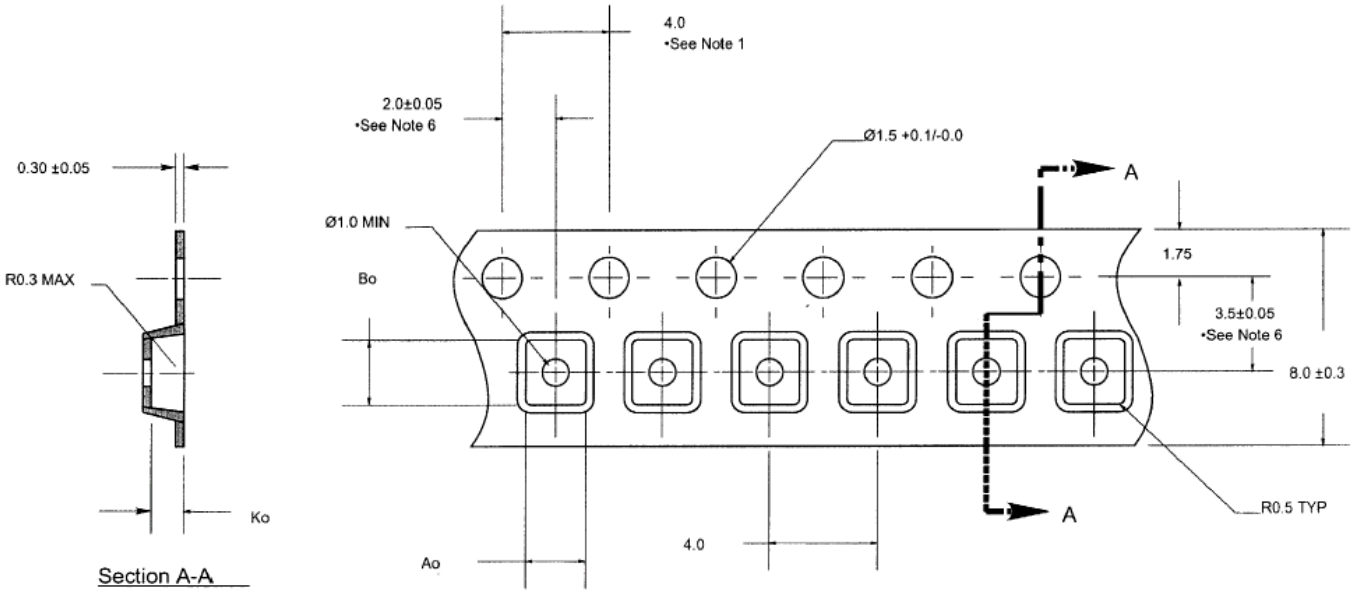


● = Pin 1 Indicator
PPP = Last 3 Digits of Part Number
YWW = Date Code

PRT-50103

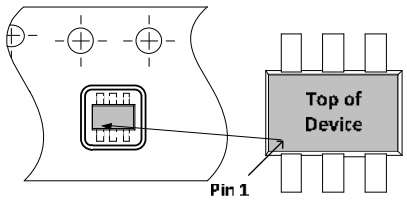
©2012-2023 pSemi Corporation. All rights reserved.

Figure 31. Tape and Reel Specification



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 2.25 mm
Bo = 2.4 mm
Ko = 1.2 mm



Device Orientation in Tape

Table 7. Ordering Information

Order Code	Description	Package	Shipping Method
PE42359SCAA-Z	PE42359 SPDT RF switch	6-lead SC-70	3000 units/T&R
EK42359-01	PE42359 Evaluation kit	Evaluation kit	1/Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification: The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product. ***Product Specification:*** The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).
The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.
The Peregrine Semiconductor name, Peregrine Semiconductor logo and UltraCMOS are registered trademarks and the pSemi name, pSemi logo, HaRP and DuNE are trademarks of pSemi Corporation in the U.S. and other countries.
pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com.

©2012-2023 pSemi Corporation. All rights reserved.