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The S-35391A is a CMOS 2-wire real-time clock IC which operates with the very low current consumption in the wide range of operation voltage. The operation voltage is 1.3 V to 5.5 V so that the S-35391A can be used for various power supplies from main supply to backup battery. Due to the 0.25 μA current consumption and wide range of power supply voltage at time keeping, the S-35391A makes the battery life longer. In the system which operates with a backup battery, the included free registers can be used as the function for user's backup memory. Users always can take back the information in the registers which is stored before power-off the main power supply, after the voltage is restored.
The S-35391A has the function to correct advance / delay of the clock data speed, in the wide range, which is caused by the crystal oscillation circuit's frequency deviation. Correcting according to the temperature change by combining this function and a temperature sensor, it is possible to make a high precise clock function which is not affected by the ambient temperature.

■ Features

- Low current consumption: 0.25 μA typ. (V_{DD} = 3.0 V, Ta = +25°C)
- Wide range of operating voltage: 1.3 V to 5.5 V
- Built-in clock correction function
- Built-in free user register
- 2-wire (I^2C-bus) CPU interface
- Built-in alarm interrupter
- Built-in flag generator during detection of low power voltage or at power-on
- Auto calendar up to the year 2099, automatic leap year calculation function
- Built-in constant voltage circuit
- Built-in 32.768 kHz crystal oscillation circuit (built-in C_d, external C_g)
- Lead-free, Sn 100%, halogen-free*1

***1.** Refer to "■ **Product Name Structure**" for details.

■ Applications

- Mobile game device
- Mobile AV device
- Digital still camera
- Digital video camera
- Electronic power meter
- DVD recorder
- TV, VCR
- Mobile phone, PHS

■ Packages

- 8-Pin SOP (JEDEC)
- SNT-8A

■ Block Diagram

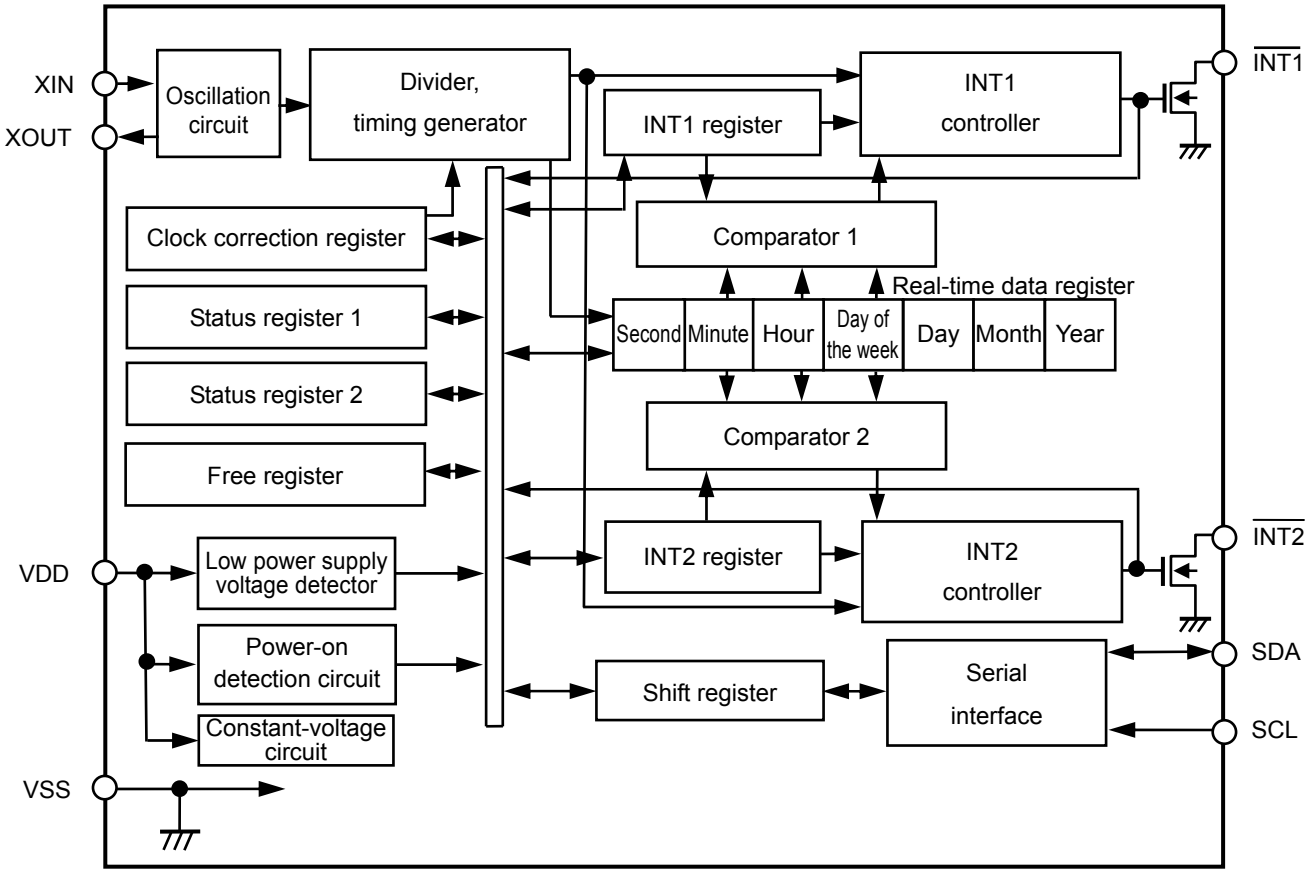
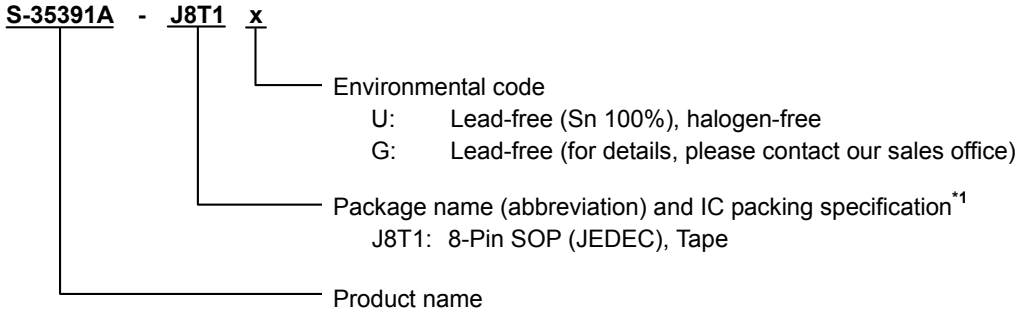


Figure 1

■ Product Name Structure

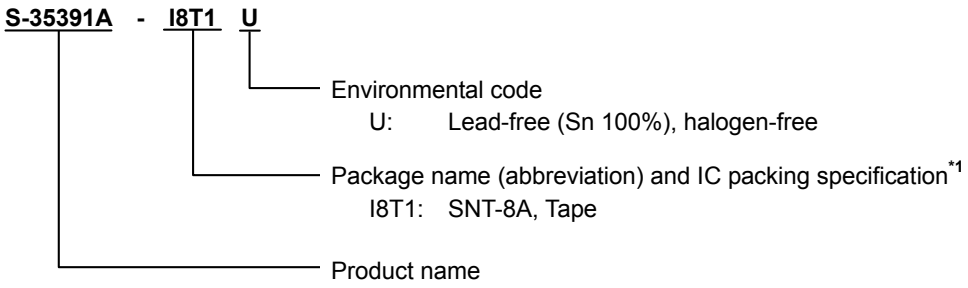
1. Product name

1. 1 8-Pin SOP (JEDEC)



***1.** Refer to the tape drawing.

1. 2 SNT-8A



***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name		Dimension	Tape	Reel	Land
8-Pin SOP (JEDEC)	Environmental code = G	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-SD	–
	Environmental code = U	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-S1	–
SNT-8A		PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

■ Pin Configuration

1. 8-Pin SOP (JEDEC)

Top view

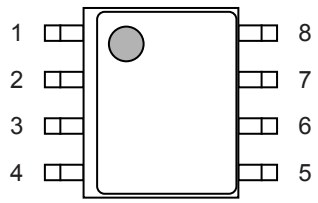


Figure 2 S-35391A-J8T1x

2. SNT-8A

Top view

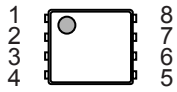


Figure 3 S-35391A-I8T1U

Table 2 List of Pins

Pin No	Symbol	Description	I/O	Configuration
1	$\overline{\text{INT1}}$	Output pin for interrupt signal 1	Output	Nch open-drain output (no protective diode at VDD)
2	XOUT	Connection pins for quartz crystal	–	–
3	XIN			
4	VSS	GND pin	–	–
5	$\overline{\text{INT2}}$	Output pin for interrupt signal 2	Output	Nch open-drain output (no protective diode at VDD)
6	SCL	Input pin for serial clock	Input	CMOS input (no protective diode at VDD)
7	SDA	I/O pin for serial data	Bi-directional	Nch open-drain output (no protective diode at VDD) CMOS input
8	VDD	Pin for positive power supply	–	–

Remark 1. x: G or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Functions

1. SDA (I/O for serial data) pin

This is a data input / output pin of I^2C-bus interface. This pin inputs / outputs data by synchronizing with a clock pulse from the SCL pin. This pin has CMOS input and Nch open drain output. Generally in use, pull up this pin to the VDD potential via a resistor, and connect it to any other device having open drain or open collector output with wired-OR connection.

2. SCL (input for serial clock) pin

This pin is to input a clock pulse for I^2C-bus interface. The SDA pin inputs / outputs data by synchronizing with the clock pulse.

3. XIN, XOUT (quartz crystal connect) pins

Connect a quartz crystal between XIN and XOUT.

4. $\overline{\text{INT1}}$ (output for interrupt signal 1) pin

This pin outputs a signal of interrupt, or a clock pulse. By using the status register 2, users can select either of; alarm 1 interrupt, output of user-set frequency, minute-periodical interrupt 1, minute-periodical interrupt 2, or 32.768 kHz output. This pin has Nch open drain output.

5. $\overline{\text{INT2}}$ (output for interrupt signal 2) pin

This pin outputs a signal of interrupt, or a clock pulse. By using the status register 2, users can select either of; alarm 2 interrupt, output of user-set frequency, or minute-periodical interrupt 1. This pin has Nch open drain output.

6. VDD (positive power supply) pin

Connect this VDD pin with a positive power supply. Regarding the values of voltage to be applied, refer to "**■ Recommended Operation Conditions**".

7. VSS pin

Connect this VSS pin to GND.

■ Equivalent Circuits of Pins

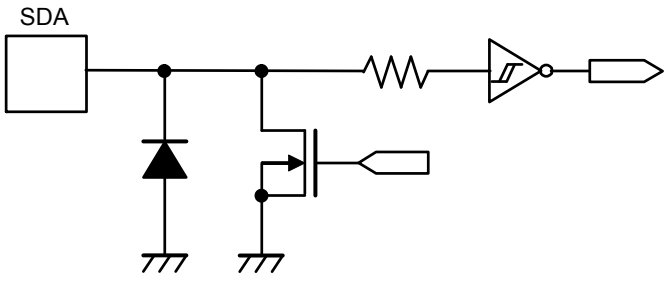


Figure 4 SDA Pin

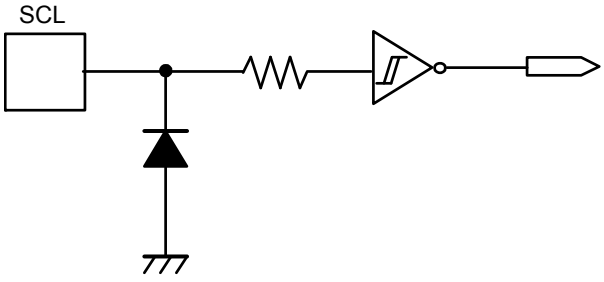


Figure 5 SCL Pin

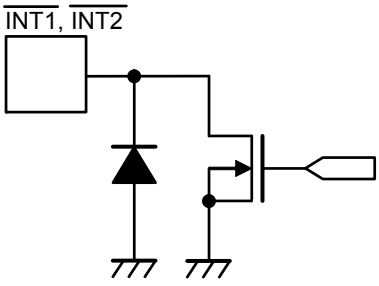


Figure 6 $\overline{\text{INT1}}$ Pin, $\overline{\text{INT2}}$ Pin

■ Absolute Maximum Ratings

Table 3

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	–	V_{SS} – 0.3 to V_{SS} + 6.5	V
Input voltage	V_{IN}	SCL, SDA	V_{SS} – 0.3 to V_{SS} + 6.5	V
Output voltage	V_{OUT}	SDA, $\overline{INT1}$, $\overline{INT2}$	V_{SS} – 0.3 to V_{SS} + 6.5	V
Operating ambient temperature*1	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–55 to +125	°C

***1.** Conditions with no condensation or frost. Condensation or frost causes short-circuiting between pins, resulting in a malfunction.

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operation Conditions

Table 4

(V_{SS} = 0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage*1	V_{DD}	Ta = –40°C to +85°C	1.3	3.0	5.5	V
Time keeping power supply voltage*2	V_{DDT}	Ta = –40°C to +85°C	V_{DET} – 0.15	–	5.5	V
Quartz crystal C_L value	C_L	–	–	6	7	pF

***1.** The power supply voltage that allows communication under the conditions shown in **Table 9** of "**■ AC Electrical Characteristics**".

***2.** The power supply voltage that allows time keeping. For the relationship with V_{DET} (low power supply voltage detection voltage), refer to "**■ Characteristics (Typical Data)**".

■ Oscillation Characteristics

Table 5

(Ta = +25°C, V_{DD} = 3.0 V, V_{SS} = 0 V, VT-200 quartz crystal (C_L = 6 pF, 32.768 kHz) manufactured by Seiko Instruments Inc.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	Within 10 seconds	1.1	–	5.5	V
Oscillation start time	t_{STA}	–	–	–	1	s
IC-to-IC frequency deviation*1	δIC	–	–10	–	+10	ppm
Frequency voltage deviation	δV	V_{DD} = 1.3 V to 5.5 V	–3	–	+3	ppm/V
External capacitance	C_g	Applied to XIN pin	–	–	9.1	pF
Internal oscillation capacitance	C_d	Applied to XOUT pin	–	8	–	pF

***1.** Reference value

■ DC Electrical Characteristics

Table 6 DC Characteristics (V_{DD} = 3.0 V)

(Ta = −40°C to +85°C, V_{SS} = 0 V, VT-200 quartz crystal (C_L = 6 pF, 32.768 kHz, C_g = 9.1 pF) manufactured by Seiko Instruments Inc.)

Item	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	–	Out of communication	–	0.25	0.93	μA
Current consumption 2	I_{DD2}	–	During communication (SCL = 100 kHz)	–	6	14	μA
Input current leakage 1	I_{IZH}	SCL, SDA	V_{IN} = V_{DD}	−0.5	–	0.5	μA
Input current leakage 2	I_{IZL}	SCL, SDA	V_{IN} = V_{SS}	−0.5	–	0.5	μA
Output current leakage 1	I_{OZH}	SDA, $\overline{INT1}$, $\overline{INT2}$	V_{OUT} = V_{DD}	−0.5	–	0.5	μA
Output current leakage 2	I_{OZL}	SDA, $\overline{INT1}$, $\overline{INT2}$	V_{OUT} = V_{SS}	−0.5	–	0.5	μA
Input voltage 1	V_{IH}	SCL, SDA	–	0.8 × V_{DD}	–	V_{SS} + 5.5	V
Input voltage 2	V_{IL}	SCL, SDA	–	V_{SS} − 0.3	–	0.2 × V_{DD}	V
Output current 1	I_{OL1}	$\overline{INT1}$, $\overline{INT2}$	V_{OUT} = 0.4 V	3	5	–	mA
Output current 2	I_{OL2}	SDA	V_{OUT} = 0.4 V	5	10	–	mA
Power supply voltage detection voltage	V_{DET}	–	–	0.65	1	1.35	V

Table 7 DC Characteristics (V_{DD} = 5.0 V)

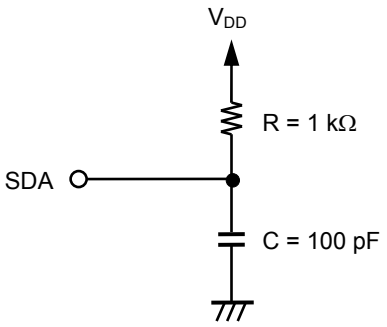
(Ta = −40°C to +85°C, V_{SS} = 0 V, VT-200 quartz crystal (C_L = 6 pF, 32.768 kHz, C_g = 9.1 pF) manufactured by Seiko Instruments Inc.)

Item	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	–	Out of communication	–	0.3	1.1	μA
Current consumption 2	I_{DD2}	–	During communication (SCL = 100 kHz)	–	14	30	μA
Input current leakage 1	I_{IZH}	SCL, SDA	V_{IN} = V_{DD}	−0.5	–	0.5	μA
Input current leakage 2	I_{IZL}	SCL, SDA	V_{IN} = V_{SS}	−0.5	–	0.5	μA
Output current leakage 1	I_{OZH}	SDA, $\overline{INT1}$, $\overline{INT2}$	V_{OUT} = V_{DD}	−0.5	–	0.5	μA
Output current leakage 2	I_{OZL}	SDA, $\overline{INT1}$, $\overline{INT2}$	V_{OUT} = V_{SS}	−0.5	–	0.5	μA
Input voltage 1	V_{IH}	SCL, SDA	–	0.8 × V_{DD}	–	V_{SS} + 5.5	V
Input voltage 2	V_{IL}	SCL, SDA	–	V_{SS} − 0.3	–	0.2 × V_{DD}	V
Output current 1	I_{OL1}	$\overline{INT1}$, $\overline{INT2}$	V_{OUT} = 0.4 V	5	8	–	mA
Output current 2	I_{OL2}	SDA	V_{OUT} = 0.4 V	6	13	–	mA
Power supply voltage detection voltage	V_{DET}	–	–	0.65	1	1.35	V

■ AC Electrical Characteristics

Table 8 Measurement Conditions

Input pulse voltage	$V_{IH} = 0.9 \times V_{DD}$, $V_{IL} = 0.1 \times V_{DD}$
Input pulse rise / fall time	20 ns
Output determination voltage	$V_{OH} = 0.5 \times V_{DD}$, $V_{OL} = 0.5 \times V_{DD}$
Output load	100 pF + pull-up resistor 1 kΩ



Remark The power supplies of the IC and load have the same electrical potential.

Figure 7 Output Load Circuit

Table 9 AC Electrical Characteristics

(Ta = −40°C to +85°C)

Item	Symbol	V_{DD} *2 ≥ 1.3 V			V_{DD} *2 ≥ 3.0 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	–	100	0	–	400	kHz
SCL clock low time	t_{LOW}	4.7	–	–	1.3	–	–	µs
SCL clock high time	t_{HIGH}	4	–	–	0.6	–	–	µs
SDA output delay time*1	t_{PD}	–	–	3.5	–	–	0.9	µs
Start condition setup time	$t_{SU.STA}$	4.7	–	–	0.6	–	–	µs
Start condition hold time	$t_{HD.STA}$	4	–	–	0.6	–	–	µs
Data input setup time	$t_{SU.DAT}$	250	–	–	100	–	–	ns
Data input hold time	$t_{HD.DAT}$	0	–	–	0	–	–	µs
Stop condition setup time	$t_{SU.STO}$	4.7	–	–	0.6	–	–	µs
SCL, SDA rise time	t_R	–	–	1	–	–	0.3	µs
SCL, SDA fall time	t_F	–	–	0.3	–	–	0.3	µs
Bus release time	t_{BUF}	4.7	–	–	1.3	–	–	µs
Noise suppression time	t_I	–	–	100	–	–	50	ns

***1.** Since the output format of the SDA pin is Nch open-drain output, SDA output delay time is determined by the values of the load resistance (R_L) and load capacity (C_L) outside the IC. Therefore, use this value only as a reference value.

***2.** Regarding the power supply voltage, refer to "**■ Recommended Operation Conditions**".

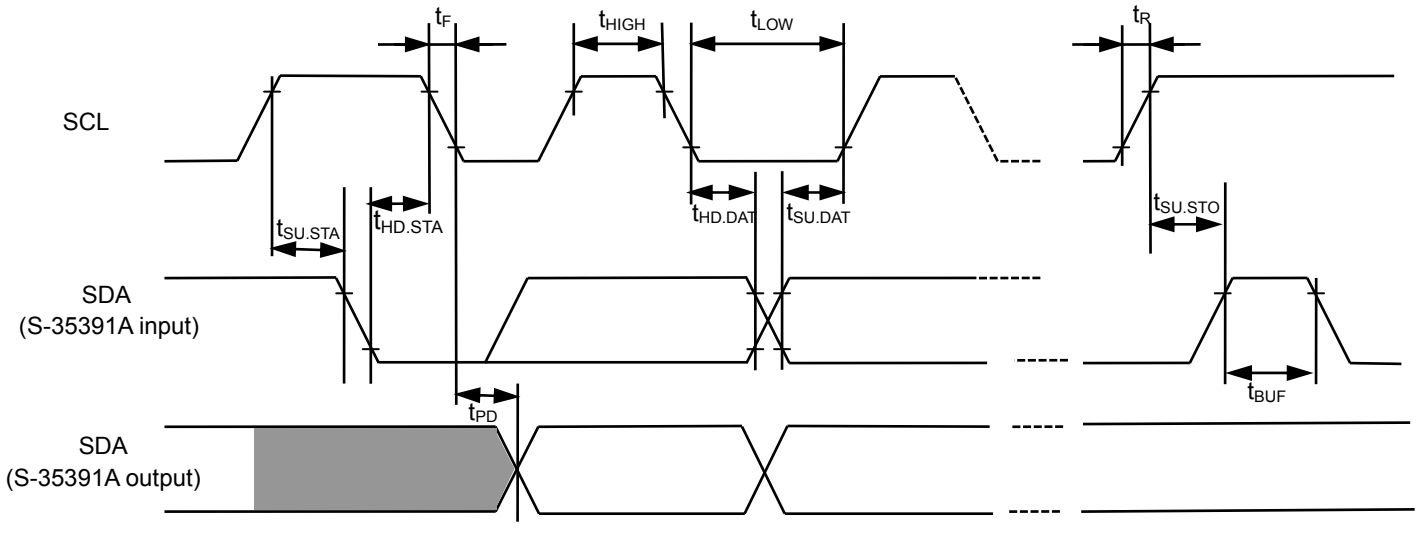


Figure 8 Bus Timing

■ Configuration of Data Communication

1. Data communication

For data communication, the master device in the system generates a start condition for the S-35391A. Next, the master device transmits 4-bit device code "1011", 3-bit command and 1-bit read / write command to the SDA line. After that, output or input is performed from B7 of data. If data I/O has been completed, finish communication by inputting a stop condition to the S-35391A. The master device generates an acknowledgment signal for every 1-byte. Regarding details, refer to "■ **Serial Interface**".

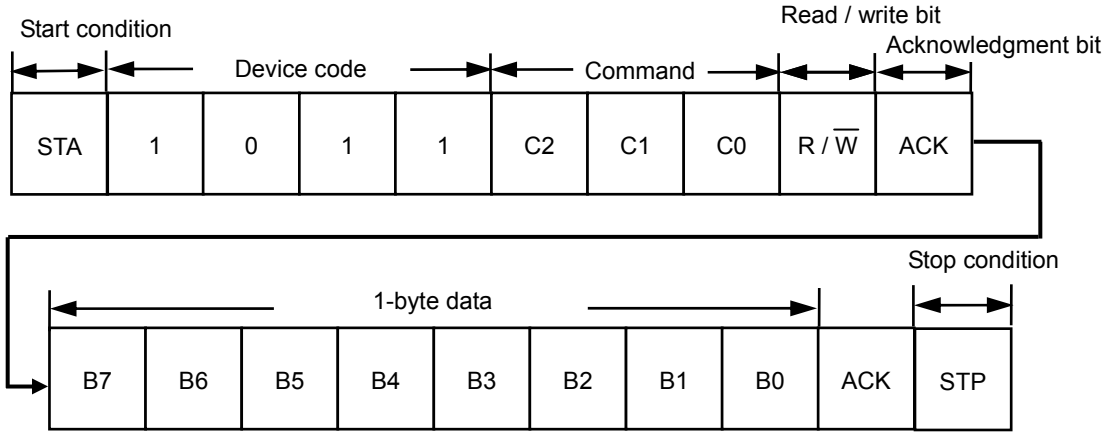


Figure 9 Data Communication

2. Configuration of command

8 types of command are available for the S-35391A. The S-35391A reads / writes the various registers by inputting these codes and commands. The S-35391A does not perform any operation with any codes and commands other than those below.

Table 10 List of Commands

Device Code	Command				Data							
	C2	C1	C0	Description	B7	B6	B5	B4	B3	B2	B1	B0
1011	0	0	0	Status register 1 access	RESET*1	$\overline{12}$ / 24	SC0*2	SC1*2	INT1*3	INT2*3	BLD*4	POC*4
	0	0	1	Status register 2 access	INT1FE	INT1ME	INT1AE	32kE	INT2FE	INT2ME	INT2AE	TEST*5
	0	1	0	Real-time data 1 access (year data to)	Y1 M1 D1 W1 H1 m1 s1	Y2 M2 D2 W2 H2 m2 s2	Y4 M4 D4 W4 H4 m4 s4	Y8 M8 D8 –*6 H8 m8 s8	Y10 M10 D10 –*6 H10 m10 s10	Y20 –*6 D20 –*6 H20 m20 s20	Y40 –*6 –*6 –*6 $\overline{\text{AM}}$ / PM m40 s40	Y80 –*6 –*6 –*6 –*6 –*6 –*6
	0	1	1	Real-time data 2 access (hour data to)	H1 m1 s1	H2 m2 s2	H4 m4 s4	H8 m8 s8	H10 m10 s10	H20 m20 s20	$\overline{\text{AM}}$ / PM m40 s40	–*6 –*6 –*6
	1	0	0	INT1 register access (alarm time 1: week / hour / minute) (INT1AE = 1, INT1ME = 0, INT1FE = 0)	W1 H1 m1	W2 H2 m2	W4 H4 m4	–*6 H8 m8	–*6 H10 m10	–*6 H20 m20	–*6 $\overline{\text{AM}}$ / PM m40	A1WE A1HE A1mE
				INT1 register access (output of user-set frequency) (INT1ME = 0, INT1FE = 1)	1 Hz	2 Hz	4 Hz	8 Hz	16 Hz	SC2*2	SC3*2	SC4*2
	1	0	1	INT2 register access (alarm time 2: week / hour / minute) (INT2AE = 1, INT2ME = 0, INT2FE = 0)	W1 H1 m1	W2 H2 m2	W4 H4 m4	–*6 H8 m8	–*6 H10 m10	–*6 H20 m20	–*6 $\overline{\text{AM}}$ / PM m40	A2WE A2HE A2mE
				INT2 register access (output of user-set frequency) (INT2ME = 0, INT2FE = 1)	1 Hz	2 Hz	4 Hz	8 Hz	16 Hz	SC5*2	SC6*2	SC7*2
	1	1	0	Clock correction register access	V0	V1	V2	V3	V4	V5	V6	V7
	1	1	1	Free register access	F0	F1	F2	F3	F4	F5	F6	F7

***1.** Write-only flag. The S-35391A initializes by writing "1" in this register.

***2.** Scratch bit. This is a register which is available for read / write operations and can be used by users freely.

***3.** Read-only flag. Valid only when using the alarm function. When the alarm time matches, this flag is set to "1", and it is cleared to "0" when reading.

***4.** Read-only flag. "POC" is set to "1" when power is applied. It is cleared to "0" when reading. Regarding "BLD", refer to "■ **Low Power Supply Voltage Detection Circuit**".

***5.** Test bit for ABLIC Inc. Be sure to set to "0" in use.

***6.** No effect when writing. It is "0" when reading.

■ Configuration of Registers

1. Real-time data register

The real-time data register is a 7-byte register that stores the data of year, month, day, day of the week, hour, minute, and second in the BCD code. To write / read real-time data 1 access, transmit / receive the data of year in B7, month, day, day of the week, hour, minute, second in B0, in 7-byte. When you skip the procedure to access the data of year, month, day, day of the week, read / write real-time data 2 accesses. In this case, transmit / receive the data of hour in B7, minute, second in B0, in 3-byte.
The S-35391A transfers a set of data of time to the real-time data register when it recognizes a reading instruction. Therefore, the S-35391A keeps precise time even if time-carry occurs during the reading operation of the real-time data register.

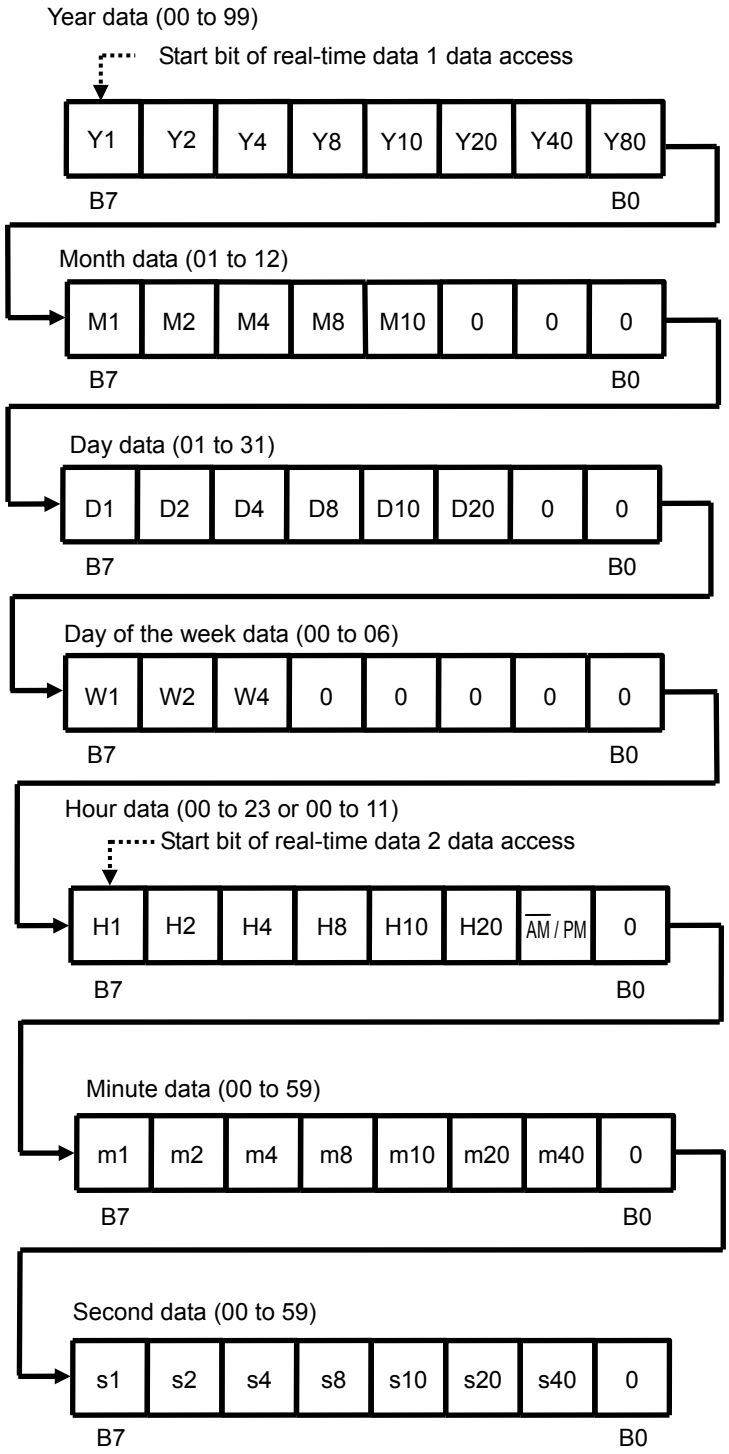


Figure 10 Real-Time Data Register

Year data (00 to 99): Y1, Y2, Y4, Y8, Y10, Y20, Y40, Y80

Sets the lower two digits of the Western calendar year (00 to 99) and links together with the auto calendar function until 2099.
Example: 2053 (Y1, Y2, Y4, Y8, Y10, Y20, Y40, Y80) = (1, 1, 0, 0, 1, 0, 1, 0)

Month data (01 to 12): M1, M2, M4, M8, M10

Example: December (M1, M2, M4, M8, M10, 0, 0, 0) = (0, 1, 0, 0, 1, 0 ,0 ,0)

Day data (01 to 31): D1, D2, D4, D8, D10, D20

The count value is automatically changed by the auto calendar function.
1 to 31: Jan., Mar., May, July, Aug., Oct., Dec., 1 to 30: April, June, Sep., Nov.
1 to 29: Feb. (leap year), 1 to 28: Feb. (non-leap year)
Example: 29 (D1, D2, D4, D8, D10, D20, 0, 0) = (1, 0, 0, 1, 0, 1, 0, 0)

Day of the week data (00 to 06): W1, W2, W4

A septenary up counter. Day of the week is counted in the order of 00, 01, 02, …, 06, and 00. Set up day of the week and the count value.

Hour data (00 to 23 or 00 to 11): H1, H2, H4, H8, H10, H20, $\overline{\text{AM}}$ / PM

In 12-hour mode, write 0; AM, 1; PM in the $\overline{\text{AM}}$ / PM bit. In 24-hour mode, users can write either 0 or 1. 0 is read when the hour data is from 00 to 11, and 1 is read when from 12 to 23.

Example (12-hour mode): 11 p.m. (H1, H2, H4, H8, H10, H20, $\overline{\text{AM}}$ / PM , 0) = (1, 0, 0, 0, 1, 0, 1, 0)
Example (24-hour mode): 22 (H1, H2, H4, H8, H10, H20, $\overline{\text{AM}}$ / PM , 0) = (0, 1, 0, 0, 0, 1, 1, 0)

Minute data (00 to 59): m1, m2, m4, m8, m10, m20, m40

Example: 32 minutes (m1, m2, m4, m8, m10, m20, m40, 0) = (0, 1, 0, 0, 1, 1, 0, 0)
Example: 55 minutes (m1, m2, m4, m8, m10, m20, m40, 0) = (1, 0, 1, 0, 1, 0, 1, 0)

Second data (00 to 59): s1, s2, s4, s8, s10, s20, s40

Example: 19 seconds (s1, s2, s4, s8, s10, s20, s40, 0) = (1, 0, 0, 1, 1, 0, 0, 0)

2. Status register 1

Status register 1 is a 1-byte register that is used to display and set various modes. The bit configuration is shown below.

B7	B6	B5	B4	B3	B2	B1	B0
RESET	$\overline{12}$ / 24	SC0	SC1	INT1	INT2	BLD	POC
W	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R	R	R	R

R: Read
W: Write
R / $\overline{W}$: Read / write

Figure 11 Status Register 1

B0: POC

This flag is used to confirm whether the power is on. The power-on detection circuit operates at power-on and B0 is set to "1". This flag is read-only. Once it is read, it is automatically set to "0". When this flag is "1", be sure to initialize. Regarding the operation after power-on, refer to "■ **Power-on Detection Circuit and Register Status**".

B1: BLD

This flag is set to "1" when the power supply voltage decreases to the level of detection voltage (V_{DET}) or less. Users can detect a drop in the power supply voltage. Once this flag is set to "1", it is not set to "0" again even if the power supply increases to the level of detection voltage (V_{DET}) or more. This flag is read-only. When this flag is "1", be sure to initialize. Regarding the operation of the power supply voltage detection circuit, refer to "■ **Low Power Supply Voltage Detection Circuit**".

B2: INT2, B3: INT1

This flag indicates the time set by alarm and when the time has reached it. This flag is set to "1" when the time that users set by using the alarm interrupt function has come. The INT1 flag at alarm 1 interrupt mode and the INT2 flag at alarm 2 interrupt mode are set to "1". Set "0" in INT1AE (B5 in the status register 2) or in INT2AE (B1 in the status register 2) after reading "1" in the INT1 flag or in the INT2 flag. This flag is read-only. Once this flag is read, it is set to "0" automatically.

B4: SC1, B5: SC0

These flags are SRAM type registers, they are 2 bits as a whole, can be freely set by users.

B6: $\overline{12}$ / 24

This flag is used to set 12-hour or 24-hour mode. Set the flag ahead of write operation of the real-time data register in case of 24-hour mode.

0: 12-hour mode
1: 24-hour mode

B7: RESET

The internal IC is initialized by setting this bit to "1". This bit is write-only. It is always "0" when reading. When applying the power supply voltage to the IC, be sure to write "1" to this bit to initialize the circuit. Regarding each status of registers after initialization, refer to "■ **Register Status After Initialization**".

3. Status register 2

Status register 2 is a 1-byte register that is used to display and set various modes. The bit configuration is shown below.

B7	B6	B5	B4	B3	B2	B1	B0
INT1FE	INT1ME	INT1AE	32kE	INT2FE	INT2ME	INT2AE	TEST
R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$

R / $\overline{W}$: Read / write

Figure 12 Status Register 2

B0: TEST

This is a test flag for ABLIC Inc. Be sure to set this flag to "0" in use. If this flag is set to "1", be sure to initialize to set "0".

B1: INT2AE, B2: INT2ME, B3: INT2FE

These bits are used to select the output mode for the $\overline{INT2}$ pin. **Table 11** shows how to select the mode. To use an alarm 2 interrupt, set alarm interrupt mode, then access the INT2 register.

Table 11 Output Modes for $\overline{INT2}$ Pin

INT2AE	INT2ME	INT2FE	$\overline{INT2}$ Pin Output Mode
0	0	0	No interrupt
–*1	0	1	Output of user-set frequency
–*1	1	0	Per-minute edge interrupt
–*1	1	1	Minute-periodical interrupt 1 (50% duty)
1	0	0	Alarm 2 interrupt

***1.** Don't care (both of 0 and 1 are acceptable).

B4: 32kE, B5: INT1AE, B6: INT1ME, B7: INT1FE

These bits are used to select the output mode for the $\overline{INT1}$ pin. **Table 12** shows how to select the mode. To use alarm 1 interrupt, access the INT1 register after setting the alarm interrupt mode.

Table 12 Output Modes for $\overline{INT1}$ Pin

32kE	INT1AE	INT1ME	INT1FE	$\overline{INT1}$ Pin Output Mode
0	0	0	0	No interrupt
0	–*1	0	1	Output of user-set frequency
0	–*1	1	0	Per-minute edge interrupt
0	0	1	1	Minute-periodical interrupt 1 (50% duty)
0	1	0	0	Alarm 1 interrupt
0	1	1	1	Minute-periodical interrupt 2
1	–*1	–*1	–*1	32.768 kHz output

***1.** Don't care (both of 0 and 1 are acceptable).

4. INT1 register and INT2 register

The INT1 and INT2 registers are to set up the output of user-set frequency, or to set up alarm interrupt. Users are able to switch the output mode by using the status register 2. If selecting to use the output mode for alarm interrupt by status register 2; these registers work as alarm-time data registers. If selecting the output of user-set frequency by status register 2; these registers work as data registers to set the frequency for clock output. From each $\overline{INT1}$ and $\overline{INT2}$ pin, a clock pulse and alarm interrupt are output.

4. 1 Alarm interrupt

Users can set the alarm time (the data of day of the week, hour, minute) by using the INT1 and INT2 registers which are 3-byte data registers. The configuration of register is as well as the data register of day of the week, hour, minute, in the real-time data register; is expressed by the BCD code. Do not set a nonexistent day. Users are necessary to set up the alarm-time data according to the 12 / 24 hour mode that they set by using the status register 1.

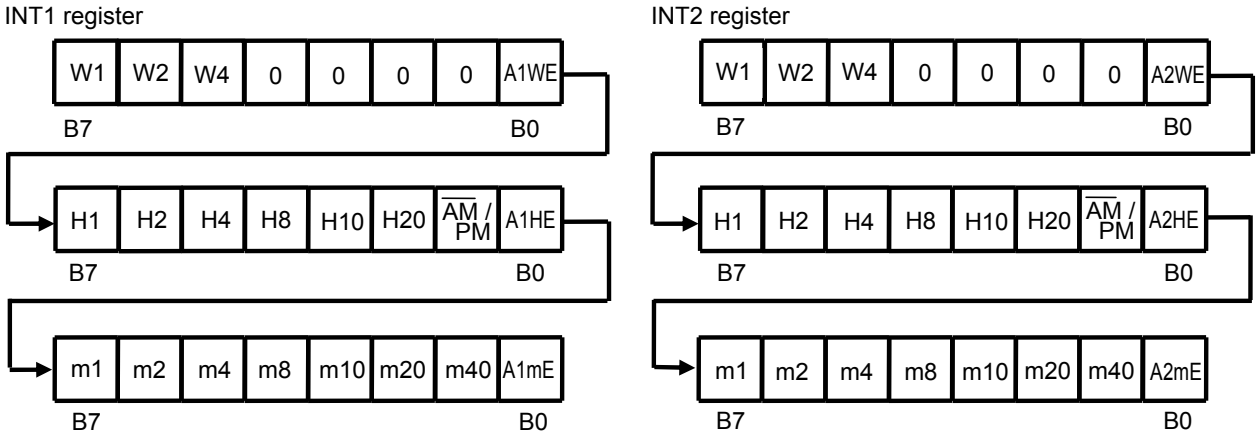


Figure 13 INT1 Register and INT2 Register (Alarm-Time Data)

The INT1 register has A1WE, A1HE, A1mE at B0 in each byte. It is possible to make data valid; the data of day of the week, hour, minute which are in the corresponding byte; by setting these bits to "1". This is as well in A2WE, A2HE, A2mE in the INT2 register.

Setting example: alarm time "7:00 pm" in the INT1 register

(1) 12-hour mode (status register 1 B6 = 0)

Set up 7:00 PM
Data written to INT1 register

	B7							B0
Day of the week	_*1	_*1	_*1	_*1	_*1	_*1	_*1	0
Hour	1	1	1	0	0	0	1	1
Minute	0	0	0	0	0	0	0	1

***1.** Don't care (both of 0 and 1 are acceptable).

(2) 24-hour mode (status register 1 B6 = 1)

Set up 19:00 PM
Data written to INT1 register

	B7							B0
Day of the week	_*1	_*1	_*1	_*1	_*1	_*1	_*1	0
Hour	1	0	0	1	1	0	1*2	1
Minute	0	0	0	0	0	0	0	1

***1.** Don't care (both of 0 and 1 are acceptable).

***2.** Set up the $\overline{AM}$ / PM flag along with the time setting.

4. 2 Output of user-set frequency

The INT1 and INT2 registers are 1-byte data registers to set up the output frequency. Setting each bit B7 to B3 in the register to "1", the frequency which corresponds to the bit is output in the AND-form. SC2 to SC4 in the INT1 register, and SC5 to SC7 in the INT2 register are 3-bit SRAM type registers that can be freely set by users.

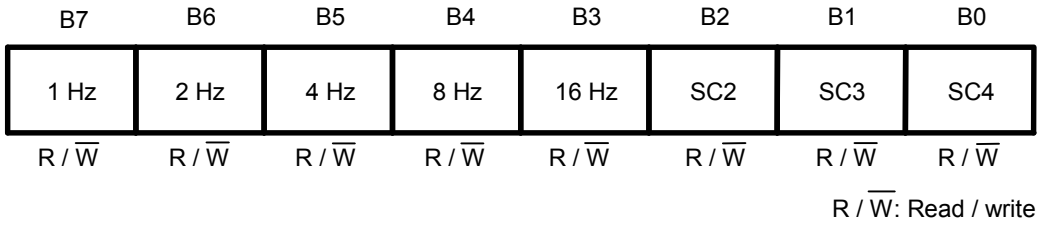


Figure 14 INT1 Register (Data Register for Output Frequency)

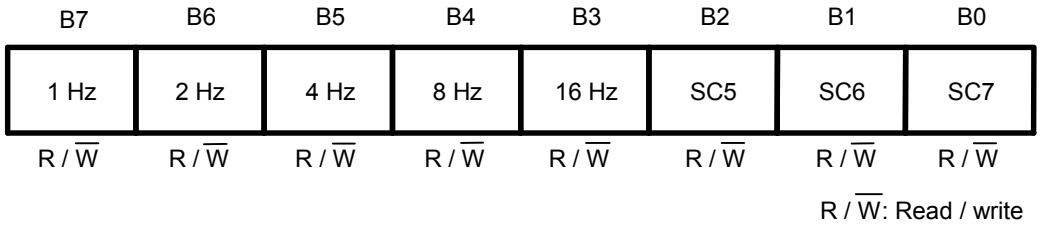


Figure 15 INT2 Register (Data Register for Output Frequency)

Example: B7 to B3 = 50h

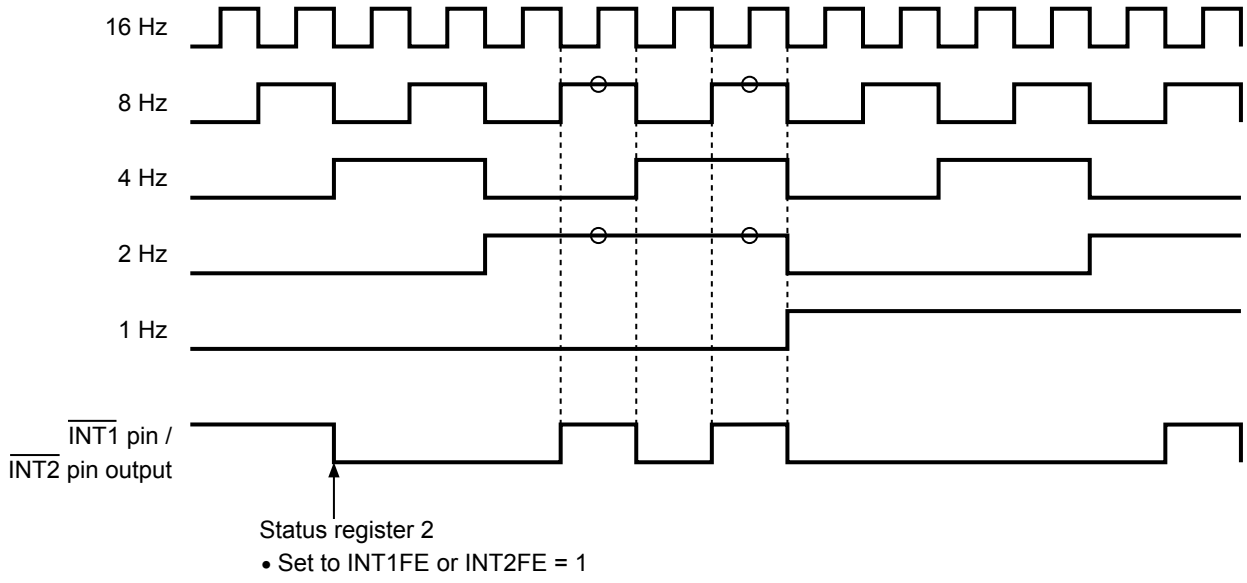


Figure 16 Example of Output from INT1 and INT2 Registers (Data Register for Output Frequency)

1 Hz clock output is synchronized with second-counter of the S-35391A.

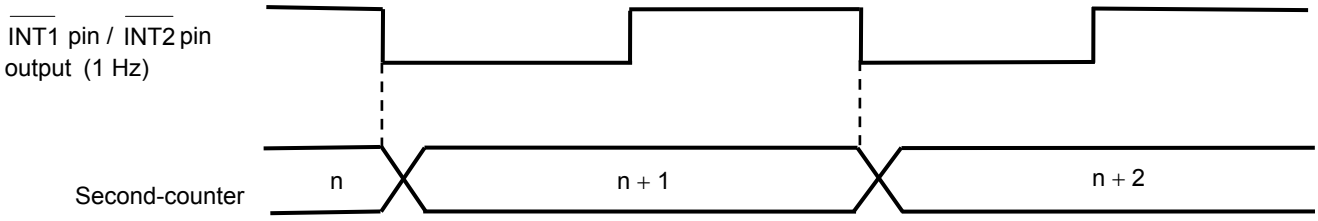


Figure 17 1 Hz Clock Output and Second-counter

5. Clock correction register

The clock correction register is a 1-byte register that is used to correct advance / delay of the clock. When not using this function, set this register to "00h". Regarding the register values, refer to "■ **Function of Clock Correction**".

B7	B6	B5	B4	B3	B2	B1	B0
V0	V1	V2	V3	V4	V5	V6	V7
R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$

R / $\overline{W}$: Read / write

Figure 18 Clock Correction Register

6. Free register

This free register is a 1-byte SRAM type register that can be set freely by users.

B7	B6	B5	B4	B3	B2	B1	B0
F0	F1	F2	F3	F4	F5	F6	F7
R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$

R / $\overline{W}$: Read / write

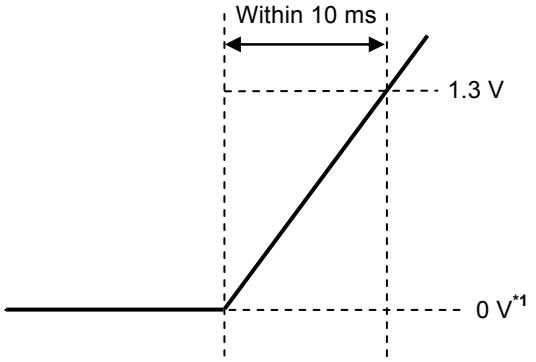
Figure 19 Free Register

■ Power-on Detection Circuit and Register Status

The power-on detection circuit operates by power-on the S-35391A, as a result each register is cleared; each register is set as follows.

Real-time data register:	00 (Y), 01 (M), 01 (D), 0 (day of the week), 00 (H), 00 (M), 00 (S)
Status register 1:	"01h"
Status register 2:	"80h"
INT1 register:	"80h"
INT2 register:	"00h"
Clock correction register:	"00h"
Free register:	"00h"

"1" is set in the POC flag (B0 in the status register 1) to indicate that power has been applied. To correct the oscillation frequency, the status register 2 goes in the mode the output of user-set frequency, so that 1 Hz clock pulse is output from the $\overline{INT1}$ pin. When "1" is set in the POC flag, be sure to initialize. The POC flag is set to "0" due to initialization so that the output of user-set frequency mode is cleared (Refer to "**■ Register Status After Initialization**").
For the regular operation of power-on detection circuit, as seen in **Figure 20**, the period to power-up the S-35391A is that the voltage reaches 1.3 V within 10 ms after setting the IC's power supply voltage at 0 V. When the power-on detection circuit is not working normally is; the POC flag (B0 in the status register 1) is not in "1", or 1 Hz is not output from the $\overline{INT1}$ pin. In this case, power-on the S-35391A once again because the internal data may be in the indefinite status.
Moreover, regarding the processing right after power-on, refer to "**■ Flowchart of Initialization and Example of Real-time Data Set-up**".



***1.** 0 V indicates that there are no potential differences between the VDD pin and VSS pin of S-35391A.

Figure 20 How to Raise the Power Supply Voltage

■ Register Status After Initialization

The status of each register after initialization is as follows.

Real-time data register:	00 (Y), 01 (M), 01 (D), 0 (day of the week), 00 (H), 00 (M), 00 (S)
Status register 1:	"0 B6 B5 B4 0 0 0 0 b" (In B6, B5, B4, the data of B6, B5, B6 in the status register 1 at initialization is set. Refer to **Figure 21**.)
Status register 2:	"00h"
INT1 register:	"00h"
INT2 register:	"00h"
Clock correction register:	"00h"
Free register:	"00h"

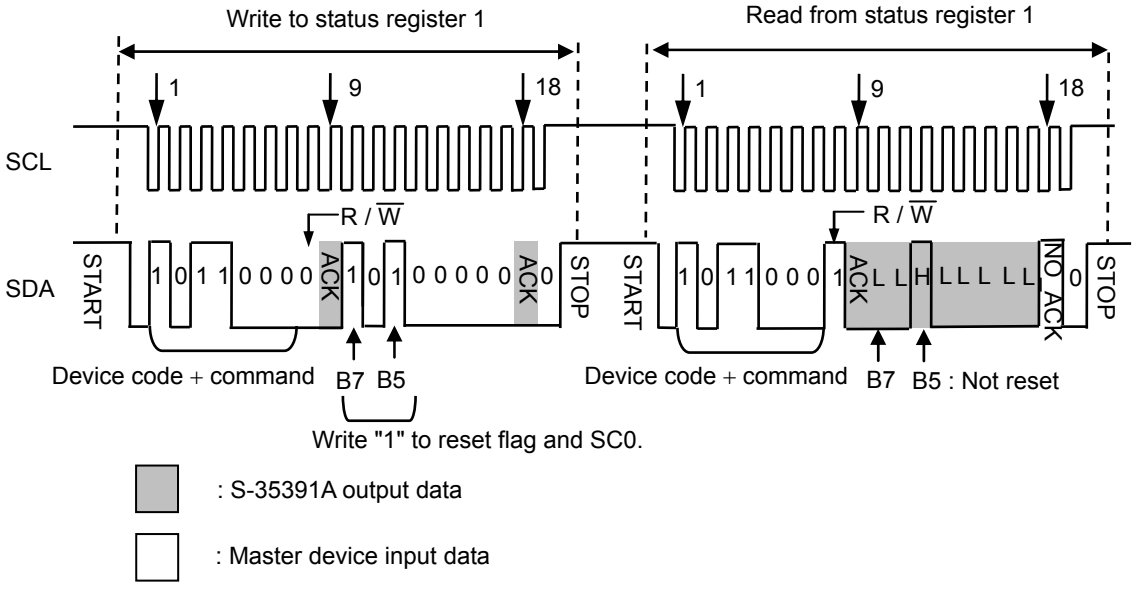


Figure 21 Data of Status Register 1 at Initialization

■ Low Power Supply Voltage Detection Circuit

The S-35391A has a low power supply voltage detection circuit, so that users can monitor drops in the power supply voltage by reading the BLD flag (B1 in the status register 1). There is a hysteresis width of approx. 0.15 V typ. between detection voltage and release voltage (refer to "■ **Characteristics (Typical Data)**"). The low power supply voltage detection circuit does the sampling operation only once in one sec for 15.6 ms.
If the power supply voltage decreases to the level of detection voltage (V_{DET}) or less, "1" is set to the BLD flag so that sampling operation stops. Once "1" is detected in the BLD flag, no sampling operation is performed even if the power supply voltage increases to the level of release voltage or more, and "1" is held in the BLD flag.
Furthermore, the S-35391A does not initialize the internal circuit even if "1" is set to the BLD flag. If the BLD flag is "1" even after the power supply voltage is recovered, the internal circuit may be in the indefinite status. In this case, be sure to initialize the circuit. Without initializing, if the next BLD flag reading is done after sampling, the BLD flag gets reset to "0". In this case, be sure to initialize although the BLD flag is in "0" because the internal circuit may be in the indefinite status.

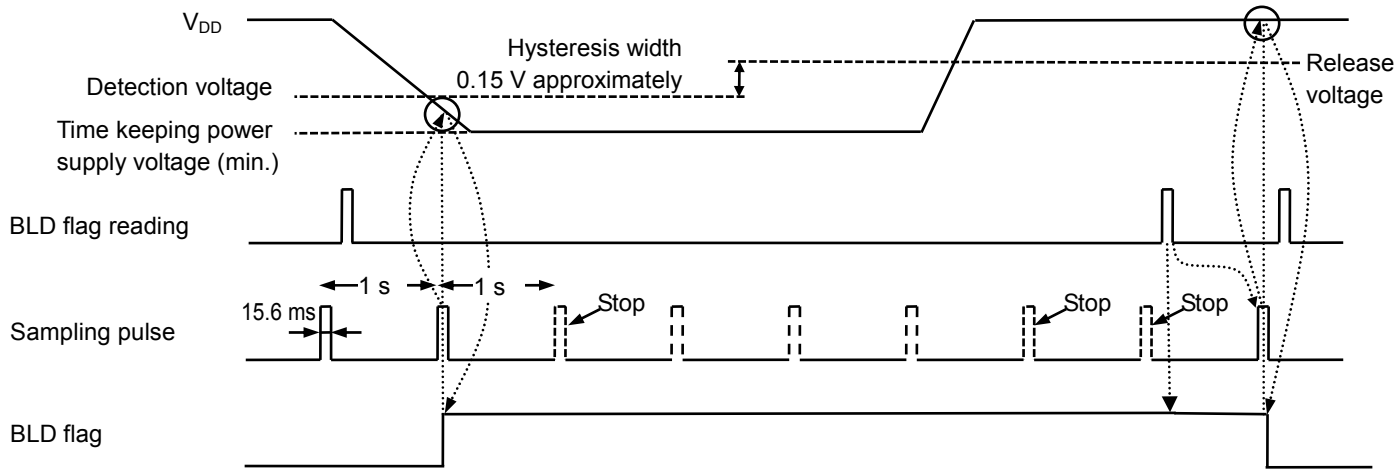


Figure 22 Timing of Low Power Supply Voltage Detection Circuit

■ Circuits Power-on and Low Power Supply Voltage Detection

Figure 23 shows the changes of the POC flag and BLD flag due to V_{DD} fluctuation.

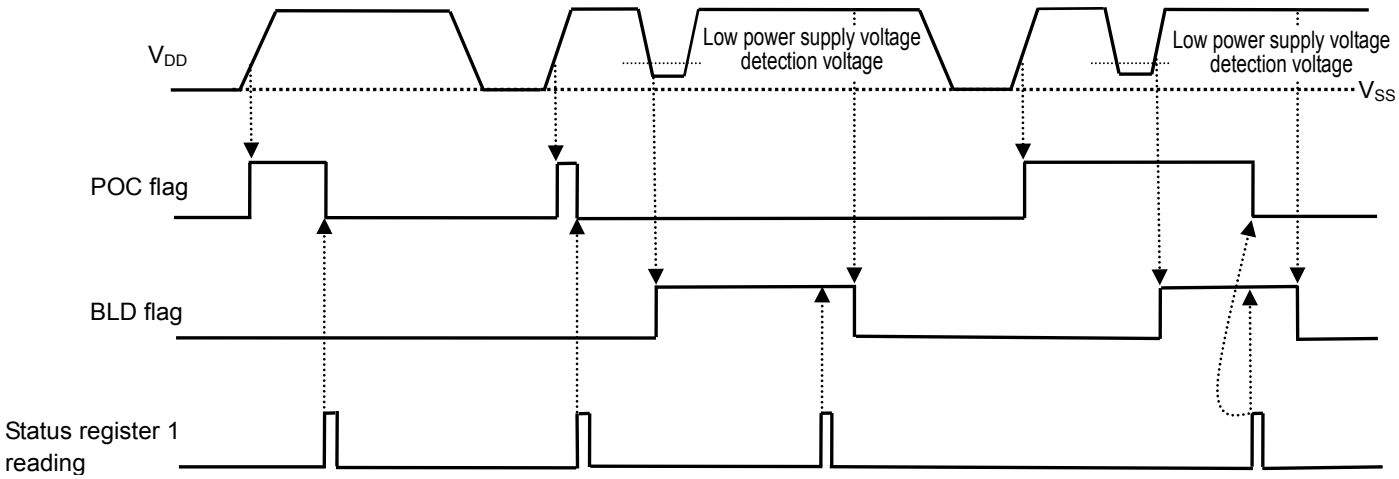


Figure 23 POC Flag and BLD Flag

■ Correction of Nonexistent Data and End-of-Month

When users write the real-time data, the S-35391A checks it. In case that the data is invalid, the S-35391A does the following procedures.

1. Processing of nonexistent data

Table 13 Processing of Nonexistent Data

Register		Normal Data	Nonexistent Data	Result
Year data		00 to 99	XA to XF, AX to FX	00
Month data		01 to 12	00, 13 to 19, XA to XF	01
Day data		01 to 31	00, 32 to 39, XA to XF	01
Day of the week data		0 to 6	7	0
Hour data*1	24-hour	0 to 23	24 to 29, 3X, XA to XF	00
	12-hour	0 to 11	12 to 20, XA to XF	00
Minute data		00 to 59	60 to 79, XA to XF	00
Second data*2		00 to 59	60 to 79, XA to XF	00

***1.** In 12-hour mode, write the $\overline{\text{AM}}$ / PM flag (B1 in hour data in the real-time data register).

In 24-hour mode, the $\overline{\text{AM}}$ / PM flag in the real-time data register is omitted. However in the flag of reading, users are able to read 0; 0 to 11, 1; 12 to 23.

***2.** Processing of nonexistent data, regarding second data, is done by a carry pulse which is generated in 1 second, after writing. At this point the carry pulse is sent to the minute-counter.

2. Correction of end-of-month

A nonexistent day, such as February 30 and April 31, is set to the first day of the next month.

■ $\overline{\text{INT1}}$ Pin and $\overline{\text{INT2}}$ Pin Output Mode

These are selectable for the output mode for $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ pins;
Alarm interrupt, the output of user-set frequency, per-minute edge interrupt output, minute-periodical interrupt output 1. In the $\overline{\text{INT1}}$ pin output mode, in addition to the above modes, minute-periodical interrupt output 2 and 32.768 kHz output are also selectable.
To switch the output mode, use the status register 2. Refer to "**3. Status register 2**" in "**■ Configuration of Registers**".
When switching the output mode, be careful of the output status of the pin. Especially, when using alarm interrupt / output of frequency, switch the output mode after setting "00h" in the INT1 / INT2 register. In 32.768 kHz output / per-minute edge interrupt output / minute-periodical interrupt output, it is unnecessary to set data in the INT1 / INT2 register for users.
Refer to the followings regarding each operation of output modes.

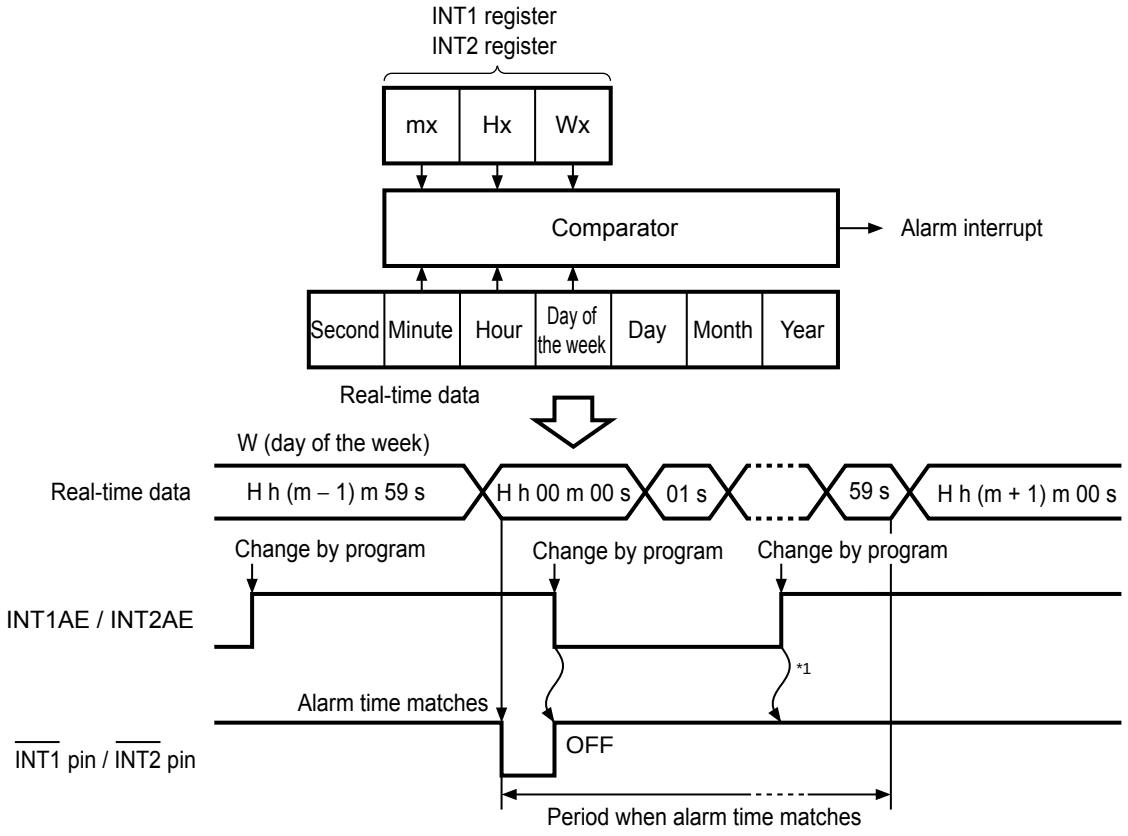
1. Alarm interrupt output

Alarm interrupt output is the function to output "L" from the $\overline{\text{INT1}}$ / $\overline{\text{INT2}}$ pin, at the alarm time which is set by user has come. If setting the pin output to "H", turn off the alarm function by setting "0" in INT1AE / INT2AE in the status register 2. To set the alarm time, set the data of day of the week, hour and minute in the INT1 / INT2 register. Refer to "**4. INT1 register and INT2 register**" in "**■ Configuration of Registers**".

1. 1 Alarm setting of "W (day of the week), H (hour), m (minute)"

Status register 2 setting
- $\overline{\text{INT1}}$ pin output mode
  $\overline{\text{32kE}}$ = 0, INT1ME = INT1FE = 0
- $\overline{\text{INT2}}$ pin output mode
  INT2ME = INT2FE = 0

INTx register alarm enable flag
- AxHE = AxmE = AxWE = "1"



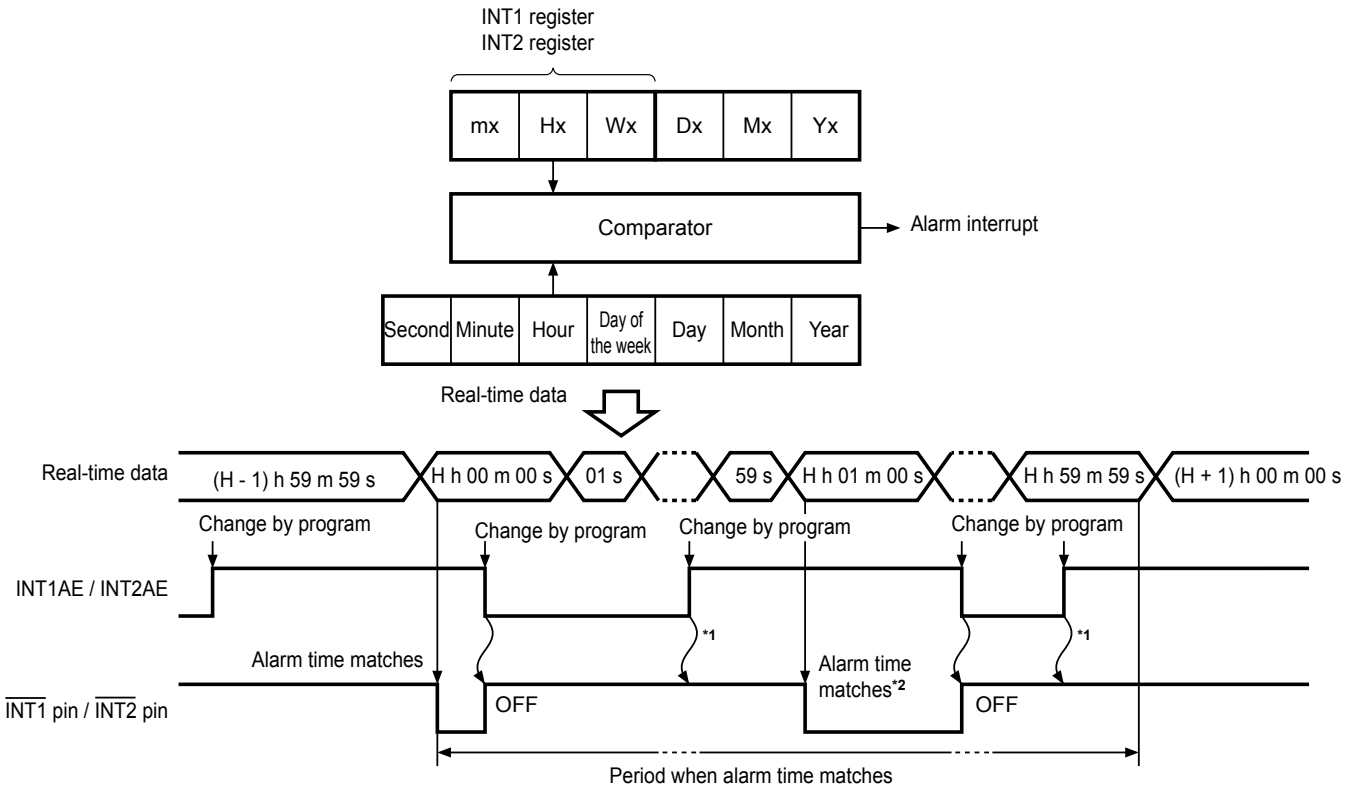
***1.** If users clear INT1AE / INT2AE once; "L" is not output from the $\overline{\text{INT1}}$ / $\overline{\text{INT2}}$ pin by setting INT1AE / INT2AE enable again, within a period when the alarm time matches real-time data.

Figure 24 Alarm Interrupt Output Timing

1. 2 Alarm setting of "H (hour)"

Status register 2 setting
- $\overline{INT1}$ pin output mode
  32kE = 0, INT1ME = INT1FE = 0
- $\overline{INT2}$ pin output mode
  INT2ME = INT2FE = 0

INTx register alarm enable flag
- AxHE = AxmE = AxWE = "1"



***1.** If users clear INT1AE / INT2AE once; "L" is not output from the $\overline{INT1}$ / $\overline{INT2}$ pin by setting INT1AE / INT2AE enable again, within a period when the alarm time matches real-time data.

***2.** If turning the alarm output on by changing the program, within the period when the alarm time matches real-time data, "L" is output again from the $\overline{INT1}$ / $\overline{INT2}$ pin when the minute is counted up.

Figure 25 Alarm Interrupt Output Timing

2. Output of user-set frequency

The output of user-set frequency is the function to output the frequency which is selected by using data, from the $\overline{INT1}$ / $\overline{INT2}$ pin, in the AND-form. Set up the data of frequency in the INT1 / INT2 register.
Refer to "**4. INT1 register and INT2 register**" in "**■ Configuration of Registers**".

Status register 2 setting
- $\overline{INT1}$ pin output mode
  32kE = 0, INT1AE = Don't care (0 or 1), INT1ME = 0
- $\overline{INT2}$ pin output mode
  INT2AE = Don't care (0 or 1), INT2ME = 0

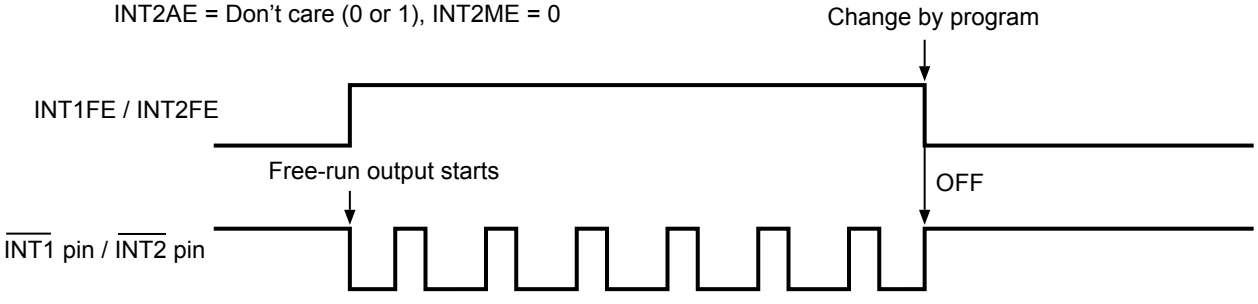


Figure 26 Output Timing of User-set Frequency

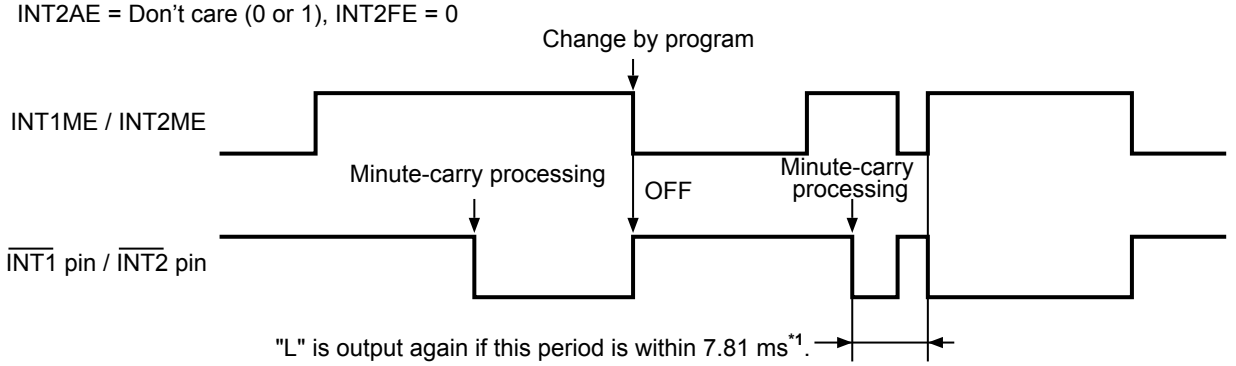
3. Per-minute edge interrupt output

Per-minute edge interrupt output is the function to output "L" from the $\overline{INT1}$ / $\overline{INT2}$ pin, when the first minute-carry processing is done, after selecting the output mode.

To set the pin output to "H", turn off the output mode of per-minute edge interrupt. In the $\overline{INT1}$ pin output mode, input "0" in INT1ME in the status register 2. In the $\overline{INT2}$ pin output mode, input "0" in INT2ME.

Status register 2 setting

- $\overline{INT1}$ pin output mode
  32kE = 0, INT1AE = Don't care (0 or 1), INT1FE = 0
- $\overline{INT2}$ pin output mode
  INT2AE = Don't care (0 or 1), INT2FE = 0

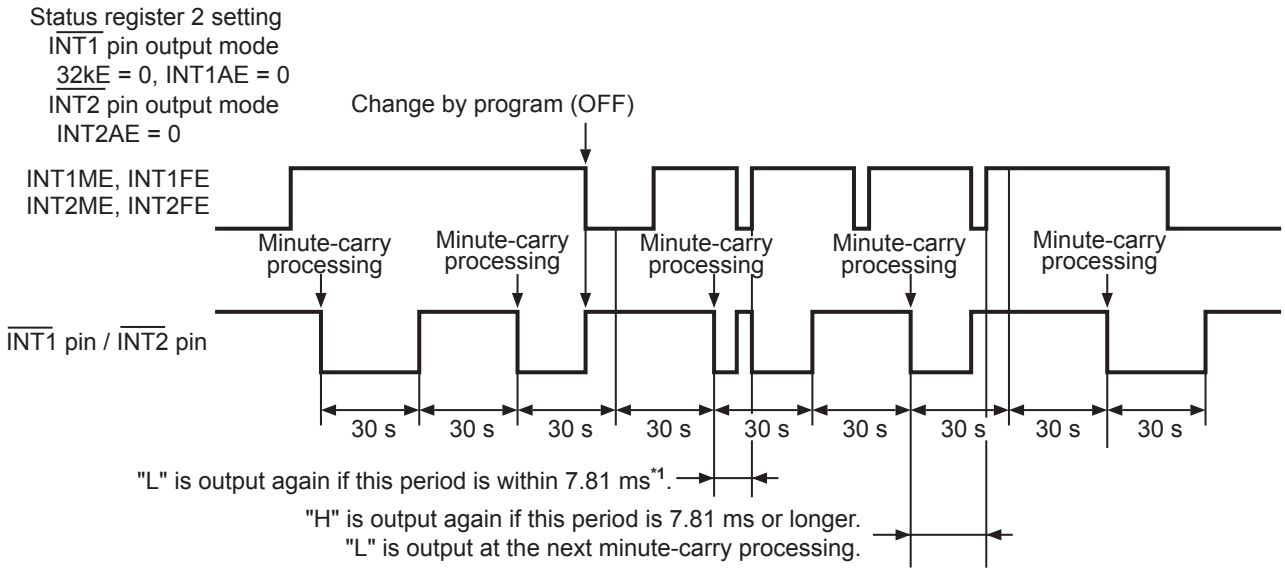


***1.** Pin output is set to "H" by disabling the output mode within 7.81 ms, because the signal of this procedure is maintained for 7.81 ms. Note that pin output is set to "L" by setting enable the output mode again.

Figure 27 Timing of Per-Minute Edge Interrupt Output

4. Minute-periodical interrupt output 1

The minute-periodical interrupt 1 is the function to output the one-minute clock pulse (Duty 50%) from the $\overline{INT1}$ / $\overline{INT2}$ pin, when the first minute-carry processing is done, after selecting the output mode.



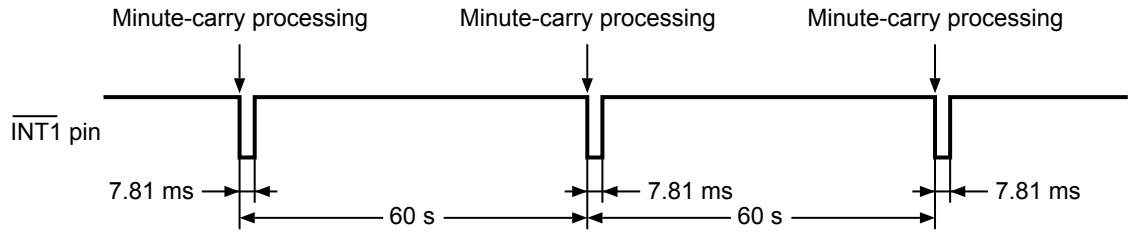
***1.** Setting the output mode disable makes the pin output "H", while the output from the $\overline{INT1}$ / $\overline{INT2}$ pin is in "L". Note that pin output is set to "L" by setting enable the output mode again.

Figure 28 Timing of Per-Minute Steady Interrupt Output 1

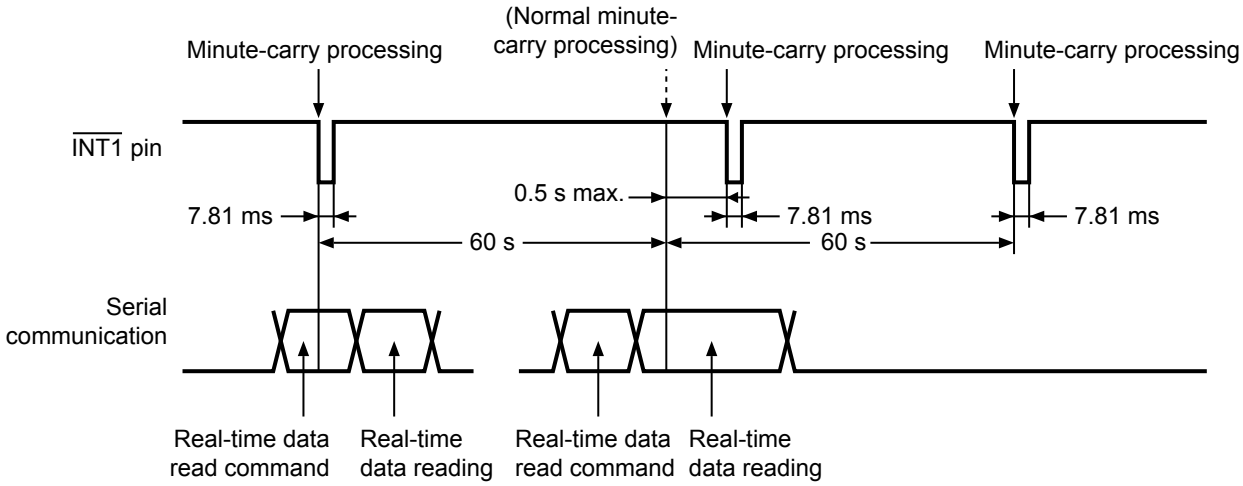
5. Minute-periodical interrupt output 2 (only in the $\overline{\text{INT1}}$ pin output mode)

The output of minute-periodical interrupt 2 is the function to output "L", for 7.81 ms, from the $\overline{\text{INT1}}$ pin, synchronizing with the first minute-carry processing after selecting the output mode. However, during reading in the real-time data register, the procedure delays at 0.5 seconds max. thus output "L" from the $\overline{\text{INT1}}$ pin also delays at 0.5 seconds max. During writing in the real-time data register, some delay is made in the output period due to write timing and the second-data of writing.

(1) During normal operation



(2) During reading operation in the real-time data register



(3) During writing operation in the real-time data register

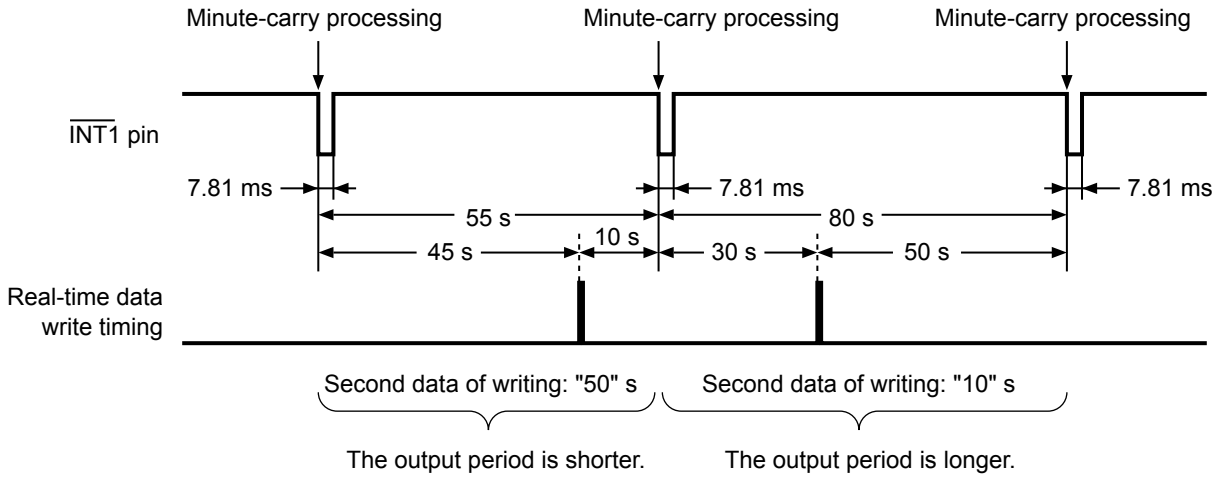


Figure 29 Timing of Minute-periodical Interrupt Output 2

6. Operation of power-on detection circuit (only in the $\overline{\text{INT1}}$ pin output mode)

When power is applied to the S-35391A, the power-on detection operates to set "1" in the POC flag (B0 in the status register 1). A 1 Hz clock pulse is output from the $\overline{\text{INT1}}$ pin.

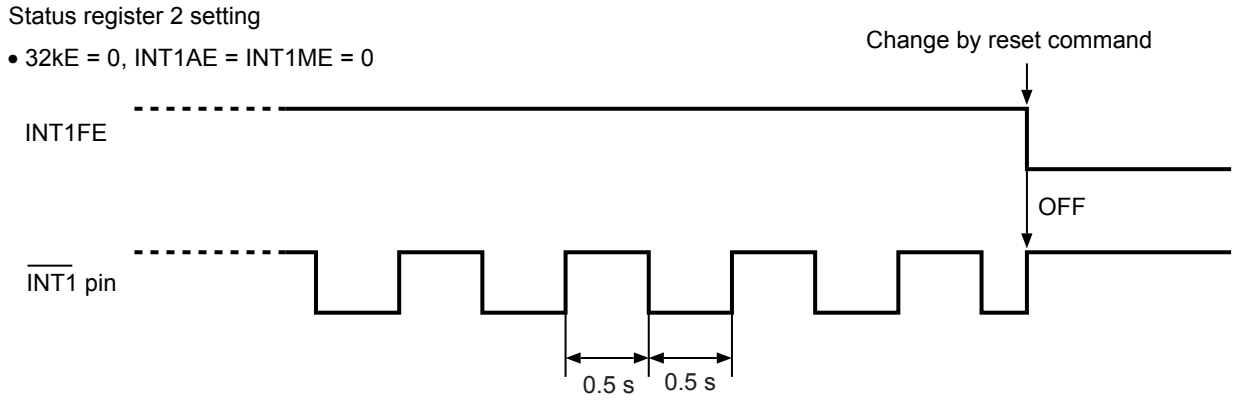


Figure 30 Output Timing of $\overline{\text{INT1}}$ Pin during Operation of Power-on Detection Circuit

■ Function of Clock Correction

The function of clock correction is to correct advance / delay of the clock due to the deviation of oscillation frequency, in order to make a high precise clock. For correction, the S-35391A adjusts the clock pulse by using a certain part of the dividing circuit, not adjusting the frequency of the quartz crystal. Correction is performed once every 20 seconds (or 60 seconds). The minimum resolution is approx. 3 ppm (or approx. 1 ppm) and the S-35391A corrects in the range of −195.3 ppm to +192.2 ppm (or of −65.1 ppm to +64.1 ppm). (Refer to **Table 14**.) Users can set up this function by using the clock correction register. Regarding how to calculate the setting data, refer to **"1. How to calculate"**. When not using this function, be sure to set "00h".

Table 14 Function of Clock Correction

Item	B0 = 0	B0 = 1
Correction	Every 20 seconds	Every 60 seconds
Minimum resolution	3.052 ppm	1.017 ppm
Correction range	−195.3 ppm to +192.2 ppm	−65.1 ppm to +64.1 ppm

1. How to calculate

1. 1 If current oscillation frequency > target frequency (in case the clock is fast)

$$\text{Correction value}^{*1} = 128 - \text{Integral value}\left(\frac{(\text{Current oscillation frequency actual measurement value}^{*2}) - (\text{Target oscillation frequency}^{*3})}{(\text{Current oscillation frequency actual measurement value}^{*2}) \times (\text{Minimum resolution}^{*4})}\right)$$

Caution The figure range which can be corrected is that the calculated value is from 0 to 64.

***1.** Convert this value to be set in the clock correction register. For how to convert, refer to "**(1) Calculation example 1**".
***2.** Measurement value when 1 Hz clock pulse is output from the $\overline{\text{INT1}}$ pin (or $\overline{\text{INT2}}$ pin).
***3.** Target value of average frequency when the clock correction function is used.
***4.** Refer to "**Table 14 Function of Clock Correction**".

(1) Calculation example 1

In case of current oscillation frequency actual measurement value = 1.000070 [Hz], target oscillation frequency = 1.000000 [Hz], B0 = 0 (Minimum resolution = 3.052 ppm)

$$\text{Correction value} = 128 - \text{Integral value}\left(\frac{(1.000070) - (1.000000)}{(1.000070) \times (3.052 \times 10^{-6})}\right)$$

$$= 128 - \text{Integral value}\,(22.93) = 128 - 22 = 106$$

Convert the correction value "106" to 7-bit binary and obtain "1101010b".
Reverse the correction value "1101010b" and set it to B7 to B1 of the clock correction register.
Thus, set the clock correction register:
(B7, B6, B5, B4, B3, B2, B1, B0) = (0, 1, 0, 1, 0, 1, 1, 0)

1. 2 If current oscillation frequency < target frequency (in case the clock is slow)

$$\text{Correction value} = \text{Integral value}\left(\frac{(\text{Target oscillation frequency}) - (\text{Current oscillation frequency actual measurement value})}{(\text{Current oscillation frequency actual measurement value}) \times (\text{Minimum resolution})}\right) + 1$$

Caution The figure range which can be corrected is that the calculated value is from 0 to 62.

(1) Calculation example 2

In case of current oscillation frequency actual measurement value = 0.999920 [Hz], target oscillation frequency = 1.000000 [Hz]. B0 = 0 (Minimum resolution = 3.052 ppm)

$$\text{Correction value} = \text{Integral value}\left(\frac{(1.000000) - (0.999920)}{(0.999920) \times (3.052 \times 10^{-6})}\right) + 1$$

$$= \text{Integral value}\,(26.21) + 1 = 26 + 1 = 27$$

Thus, set the clock correction register:
(B7, B6, B5, B4, B3, B2, B1, B0) = (1, 1, 0, 1, 1, 0, 0, 0)

(2) Calculation example 3

In case of current oscillation frequency actual measurement value = 0.999920 [Hz], target oscillation frequency = 1.000000 [Hz], B0 = 1 (Minimum resolution = 1.017 ppm)

$$\text{Correction value} = \text{Integral value}\left(\frac{(1.000000) - (0.999920)}{(0.999920) \times (1.017 \times 10^{-6})}\right) + 1$$

$$= \text{Integral value}\,(78.66) + 1$$

This calculated value exceeds the correctable range 0 to 62.
B0 = "1" (minimum resolution = 1.017 ppm) indicates the correction is impossible.

2. Setting values for registers and correction values

Table 15 Setting Values for Registers and Correction Values (Minimum Resolution: 3.052 ppm (B0 = 0))

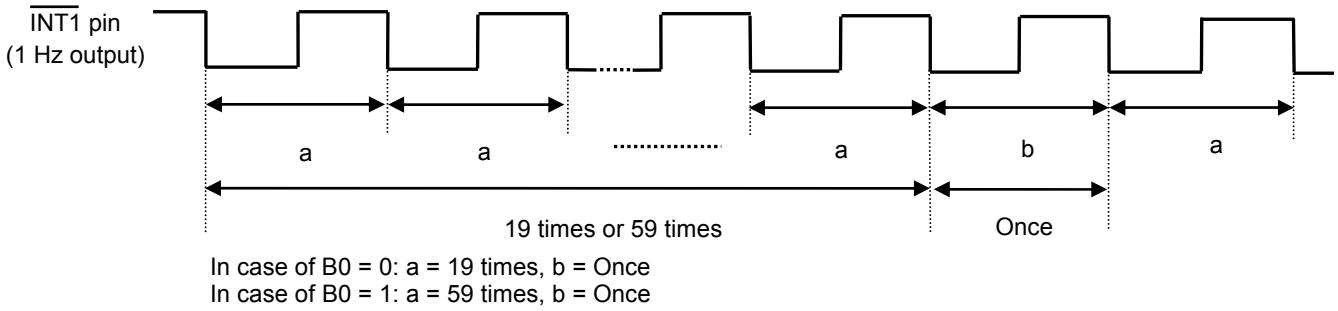
B7	B6	B5	B4	B3	B2	B1	B0	Correction Value [ppm]	Rate [s / day]
1	1	1	1	1	1	0	0	192.3	16.61
0	1	1	1	1	1	0	0	189.2	16.35
1	0	1	1	1	1	0	0	186.2	16.09
				•				•	•
				•				•	•
				•				•	•
0	1	0	0	0	0	0	0	6.1	0.53
1	0	0	0	0	0	0	0	3.1	0.26
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	0	−3.1	−0.26
0	1	1	1	1	1	1	0	−6.1	−0.53
1	0	1	1	1	1	1	0	−9.2	−0.79
				•				•	•
				•				•	•
				•				•	•
0	1	0	0	0	0	1	0	−189.2	−16.35
1	0	0	0	0	0	1	0	−192.3	−16.61
0	0	0	0	0	0	1	0	−195.3	−16.88

Table 16 Setting Values for Registers and Correction Values (Minimum Resolution: 1.017 ppm (B0 = 1))

B7	B6	B5	B4	B3	B2	B1	B0	Correction Value [ppm]	Rate [s / day]
1	1	1	1	1	1	0	1	64.1	5.54
0	1	1	1	1	1	0	1	63.1	5.45
1	0	1	1	1	1	0	1	62.0	5.36
				•				•	•
				•				•	•
				•				•	•
0	1	0	0	0	0	0	1	2.0	0.18
1	0	0	0	0	0	0	1	1.0	0.09
0	0	0	0	0	0	0	1	0	0
1	1	1	1	1	1	1	1	−1.0	−0.09
0	1	1	1	1	1	1	1	−2.0	−0.18
1	0	1	1	1	1	1	1	−3.0	−0.26
				•				•	•
				•				•	•
				•				•	•
0	1	0	0	0	0	1	1	−63.1	−5.45
1	0	0	0	0	0	1	1	−64.1	−5.54
0	0	0	0	0	0	1	1	−65.1	−5.62

3. How to confirm setting value for register and result of correction

The S-35391A does not adjust the frequency of the quartz crystal by using the clock correction function. Therefore users cannot confirm if it is corrected or not by measuring output 32.768 kHz. When the function to clock correction is being used, the cycle of 1 Hz clock pulse output from the $\overline{\text{INT1}}$ pin changes once in 20 times or 60 times, as shown in **Figure 31**.



In case of B0 = 0: a = 19 times, b = Once
In case of B0 = 1: a = 59 times, b = Once

Figure 31 Confirmation of Clock Correction

Measure a and b by using the frequency counter[*1]. Calculate the average frequency (Tave) based on the measurement results.

B0 = 0, Tave = (a × 19 + b) ÷ 20
B0 = 1, Tave = (a × 59 + b) ÷ 60

Calculate the error of the clock based on the average frequency (Tave). The following shows an example for confirmation.

Confirmation example: When B0 = 0, 66h is set

Measurement results: a = 1.000080 Hz, b = 0.998493 Hz

Clock Correction Register Setting Value		Average Frequency [Hz]	Per Day [s]
Before correction	00 h (Tave = a)	1.000080	86393
After correction	66 h (Tave = (a × 19 + b) ÷ 20)	1.00000065	86399.9

Calculating the average frequency allows to confirm the result of correction.

***1.** Use a frequency counter with 7-digit or greater precision.

Caution Measure the oscillation frequency under the usage conditions.

■ Serial Interface

The S-35391A transmits / receives various commands via I^2C-bus serial interface to read / write data. Regarding transmission is as follows.

1. Start condition

A start condition is when the SDA line changes "H" to "L" when the SCL line is in "H", so that the access starts.

2. Stop condition

A stop condition is when the SDA line changes "L" to "H" when the SCL line is in "H", and the access stops, so that the S-35391A gets standby.

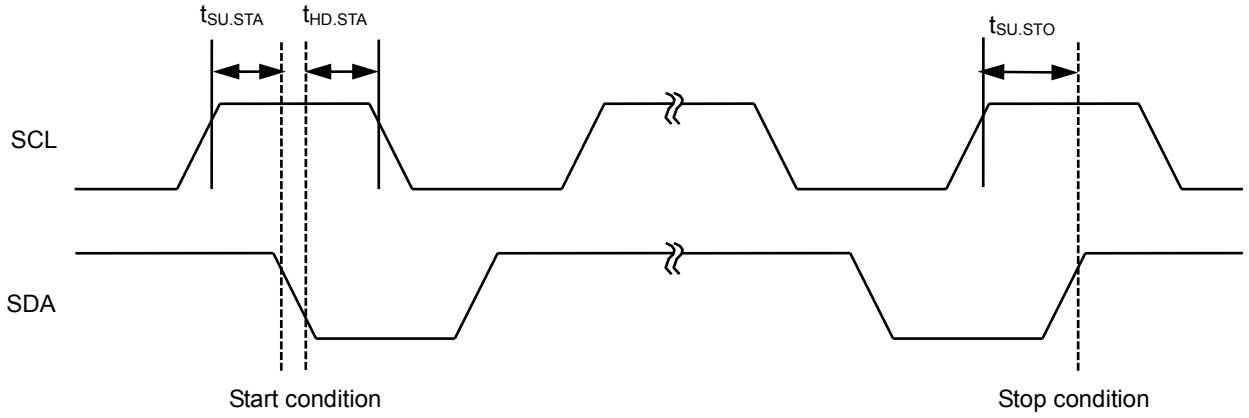


Figure 32 Start / Stop Conditions

3. Data transfer and acknowledgment signal

Data transmission is performed for every 1-byte, after detecting a start condition. Transmit data while the SCL line is in "L", and be careful of spec of $t_{SU.DAT}$ and $t_{HD.DAT}$ when changing the SDA line. If the SDA line changes while the SCL line is in "H", the data will be recognized as start/stop condition in spite of data transmission. Note that by this case, the access will be interrupted.

During data transmission, every moment receiving 1-byte data, the devices which work for receiving data send an acknowledgment signal back. For example, as seen in **Figure 33**, in case that the S-35391A is the device working for receiving data and the master device is the one working for sending data; when the 8th clock pulse falls, the master device releases the SDA line. After that, the S-35391A sends an acknowledgment signal back, and set the SDA line to "L" at the 9th clock pulse. The S-35391A does not output an acknowledgment signal is that the access is not being done regularly.

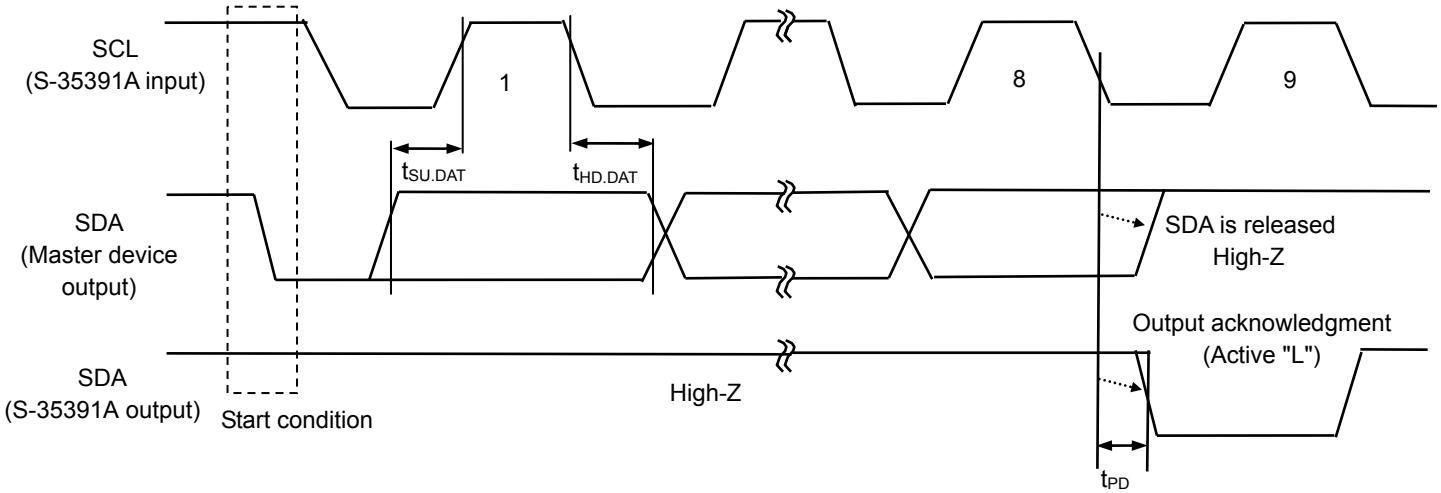


Figure 33 Output Timing of Acknowledgment Signal

The followings are data reading / writing in the S-35391A.

3. 1 Data reading in the S-35391A

After detecting a start condition, the S-35391A receives device code and command. The S-35391A enters the read-data mode by the read / write bit "1". The data is output from B7 in 1-byte. Input an acknowledgment signal from the master device every moment that the S-35391A outputs 1-byte data. However, do not input an acknowledgment signal (input NO_ACK) for the last data-byte output from the master device. This procedure notifies the completion of reading. Next, input a stop condition to the S-35391A to finish access.

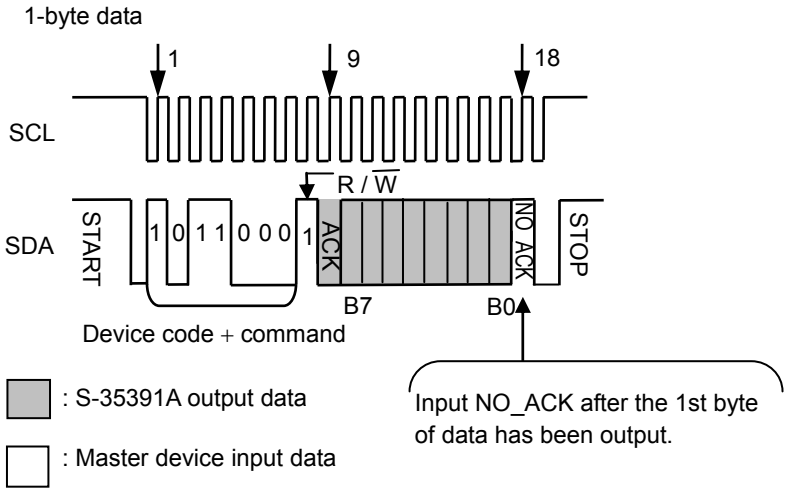


Figure 34 Example of Data Reading 1 (1-Byte Data Register)

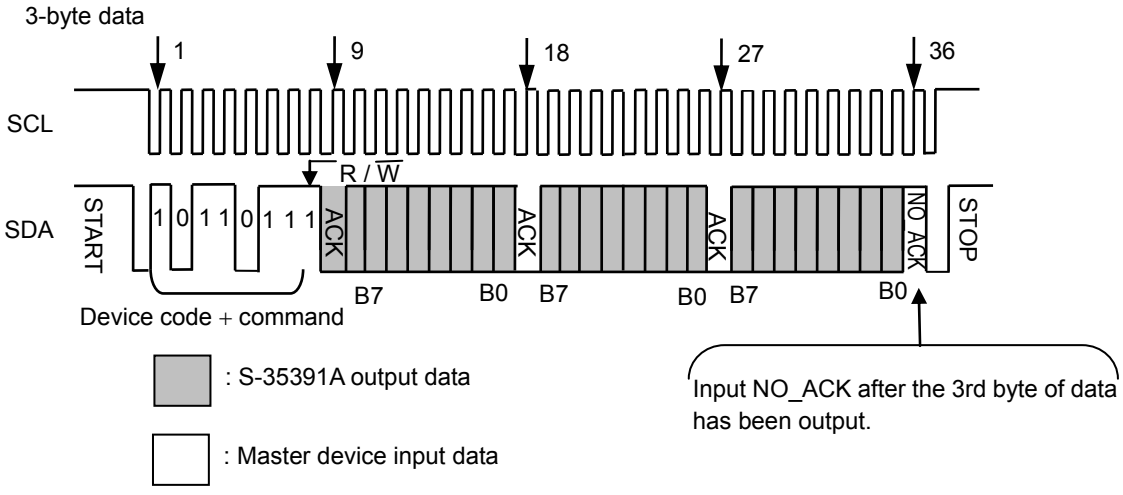


Figure 35 Example of Data Reading 2 (3-Byte Data Register)

3. 2 Data writing in the S-35391A

After detecting a start condition, the S-35391A receives device code and command. The S-35391A enters the write-data mode by the read / write bit "0". Input data from B7 to B0 in 1-byte. The S-35391A outputs an acknowledgment signal "L" every moment that 1-byte data is input. After receiving the acknowledgment signal which is for the last byte-data, input a stop condition to the S-35391A to finish access.

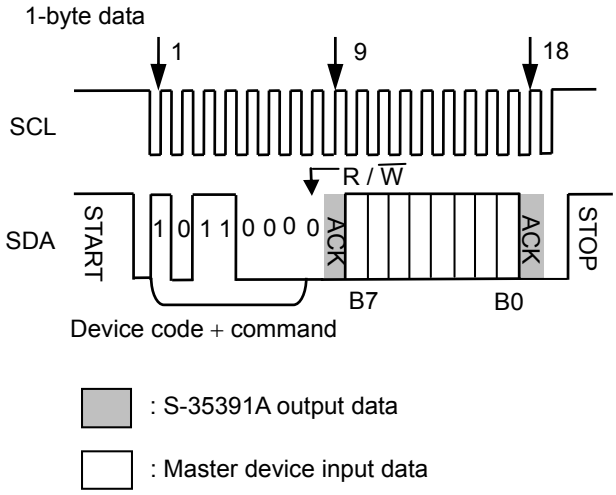


Figure 36 Example of Data Writing 1 (1-Byte Data Register)

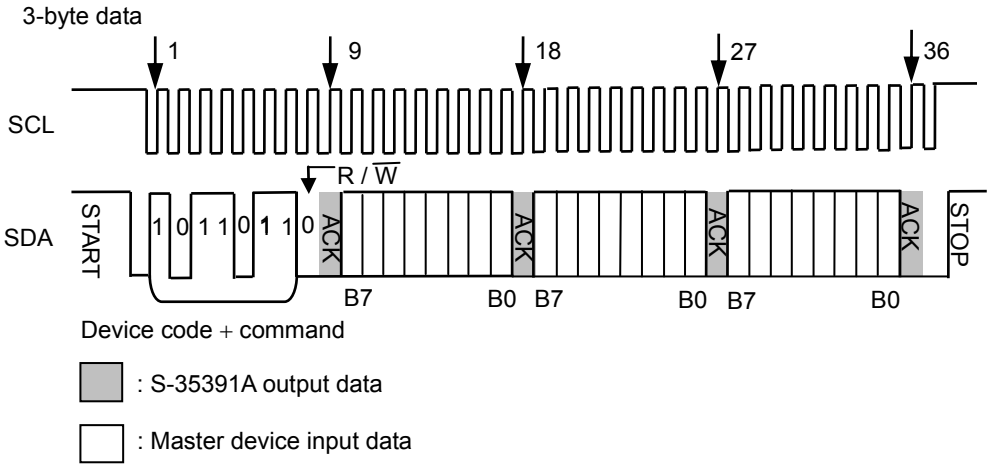
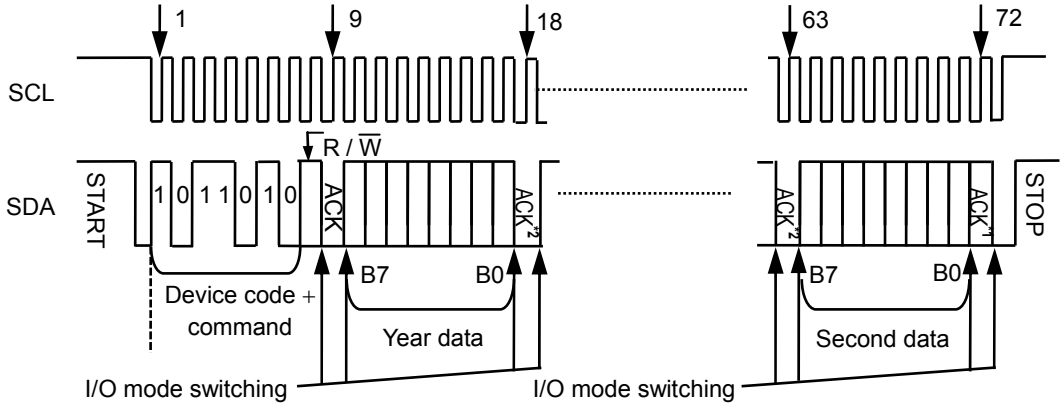


Figure 37 Example of Data Reading 2 (3-Byte Data Register)

4. Data access

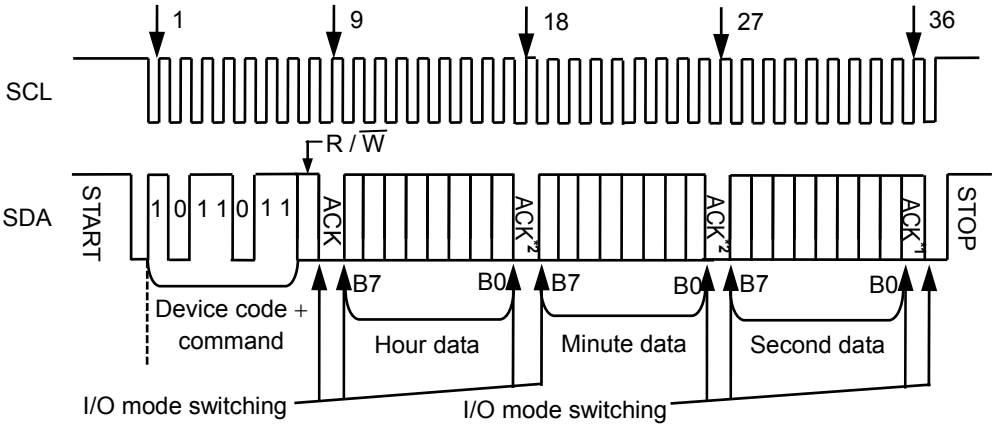
4. 1 Real-time data 1 access



***1.** Set NO_ACK = 1 when reading.
***2.** Transmit ACK = 0 from the master device to the S-35391A when reading.

Figure 38 Real-Time Data 1 Access

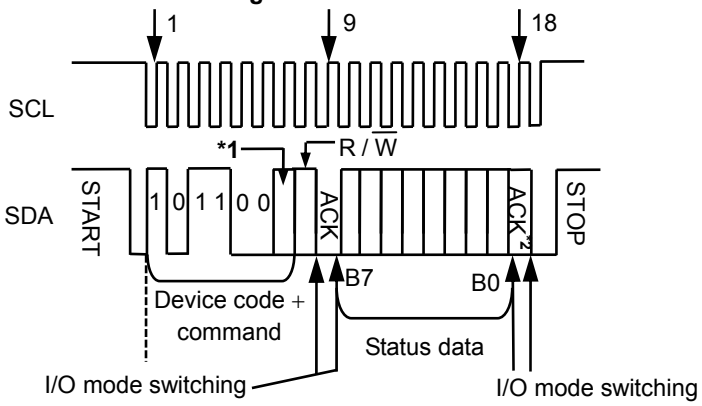
4. 2 Real-time data 2 access



***1.** Set NO_ACK = 1 when reading.
***2.** Transmit ACK = 0 from the master device to the S-35391A when reading.

Figure 39 Real-Time Data 2 Access

4. 3 Status register 1 access and status register 2 access



***1.** 0: Status register 1 selected, 1: Status register 2 selected
***2.** Set NO_ACK = 1 when reading.

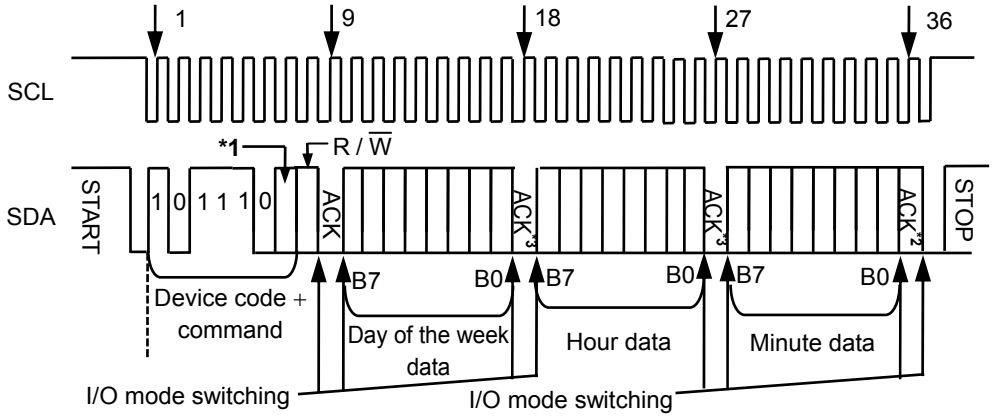
Figure 40 Status Register 1 Access and Status Register 2 Access

4. 4 INT1 register access and INT2 register access

In reading / writing the INT1 and INT2 registers, data varies depending on the setting of the status register 2. Be sure to read / write after setting the status register 2. When setting the alarm by using the status register 2, these registers work as 3-byte alarm time data registers, in other statuses, they work as 1-byte registers. When outputting the user-set frequency, they are the data registers to set up the frequency.

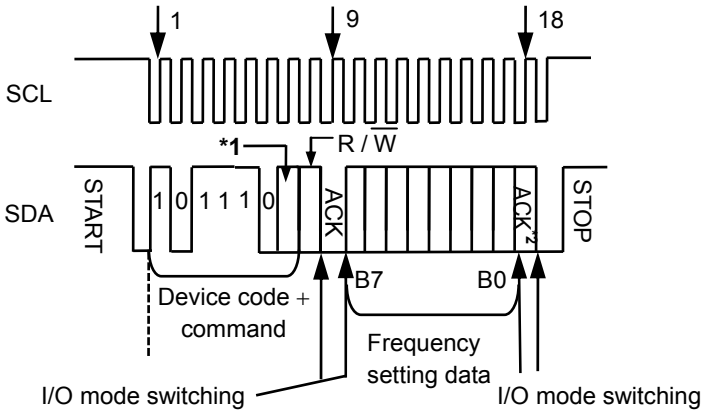
Regarding details of each data, refer to "**4. INT1 register and INT2 register**" in "**■ Configuration of Registers**".

Caution Users cannot use both functions of alarm 1 interrupt and output of user-set frequency for the $\overline{\text{INT1}}$ pin and $\overline{\text{INT2}}$ pin simultaneously.



***1.** 0: INT1 register selected, 1: INT2 register selected
***2.** Set NO_ACK = 1 when reading.
***3.** Transmit ACK = 0 from the master device to the S-35391A when reading.

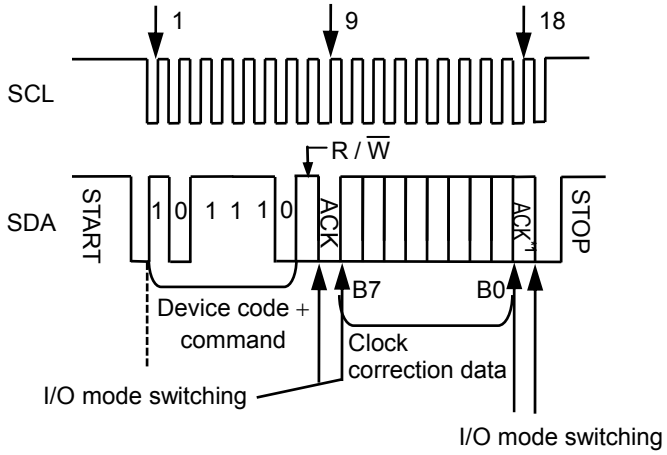
Figure 41 INT1 Register Access and INT2 Register Access



***1.** 0: INT1 register selected, 1: INT2 register selected
***2.** Set NO_ACK = 1 when reading.

Figure 42 INT1 Register and INT2 Register (Data Register for Output Frequency) Access

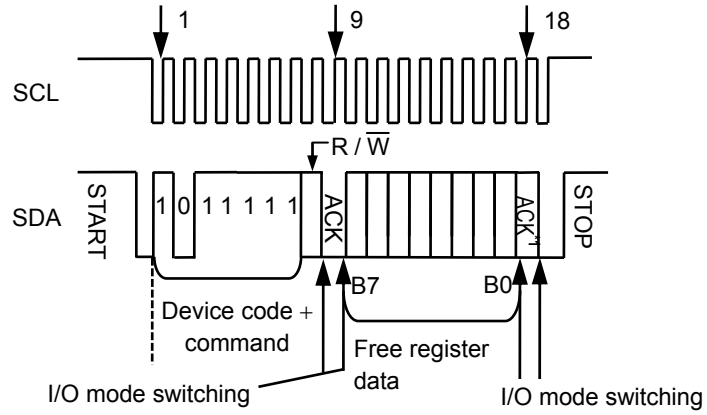
4. 5 Clock correction register access



***1.** Set NO_ACK = 1 when reading.

Figure 43 Clock Correction Register Access

4. 6 Free register access



***1.** Set NO_ACK = 1 when reading.

Figure 44 Free Register Access

■ Reset After Communication Interruption

In case of communication interruption in the S-35391A, for example, if the power supply voltage drops and only the master device is reset during communication, the S-35391A does not perform the next operation because the internal circuit keeps the status prior to communication interruption. Since the S-35391A does not have a reset pin, users usually reset its internal circuit by inputting a stop condition. However, if the SDA is outputting "L" (during output of acknowledgment signal or reading), the S-35391A does not accept a stop condition from the master device. In this case, users are necessary to finish acknowledgment output or reading of the SDA. **Figure 45** shows how to reset.
First, input a start condition from the master device (the S-35391A cannot detect a start condition because the SDA in the S-35391A is outputting "L"). Next, input a clock pulse equivalent to 7-byte data access (63-clock) from the SCL. During this period, release the SDA line for the master device. By this procedure, SDA I/O before communication interruption is finished, and the SDA line in the S-35391A is released. After that, inputting a stop condition resets the internal circuit and restores the regular communication. This reset procedure is recommended to be executed at initialization of the system after the master device's power supply voltage is raised.
If this reset procedure is executed when the S-35391A outputs an acknowledgment signal of a writing instruction, the writing operation may be performed at the corresponding register, so caution should be exercised.

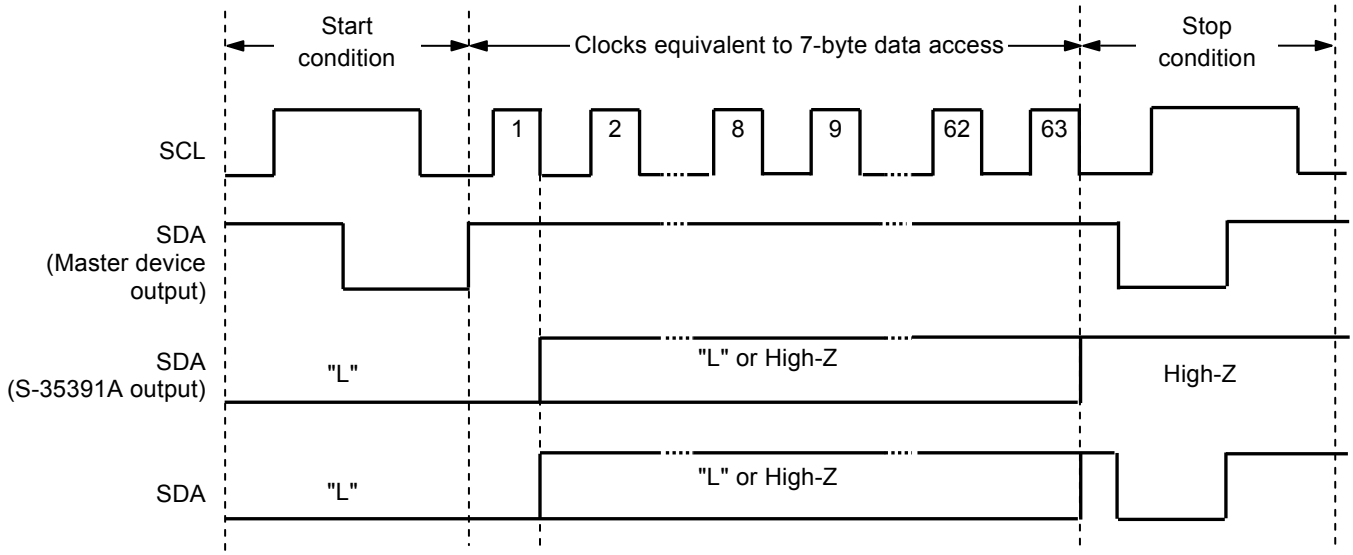
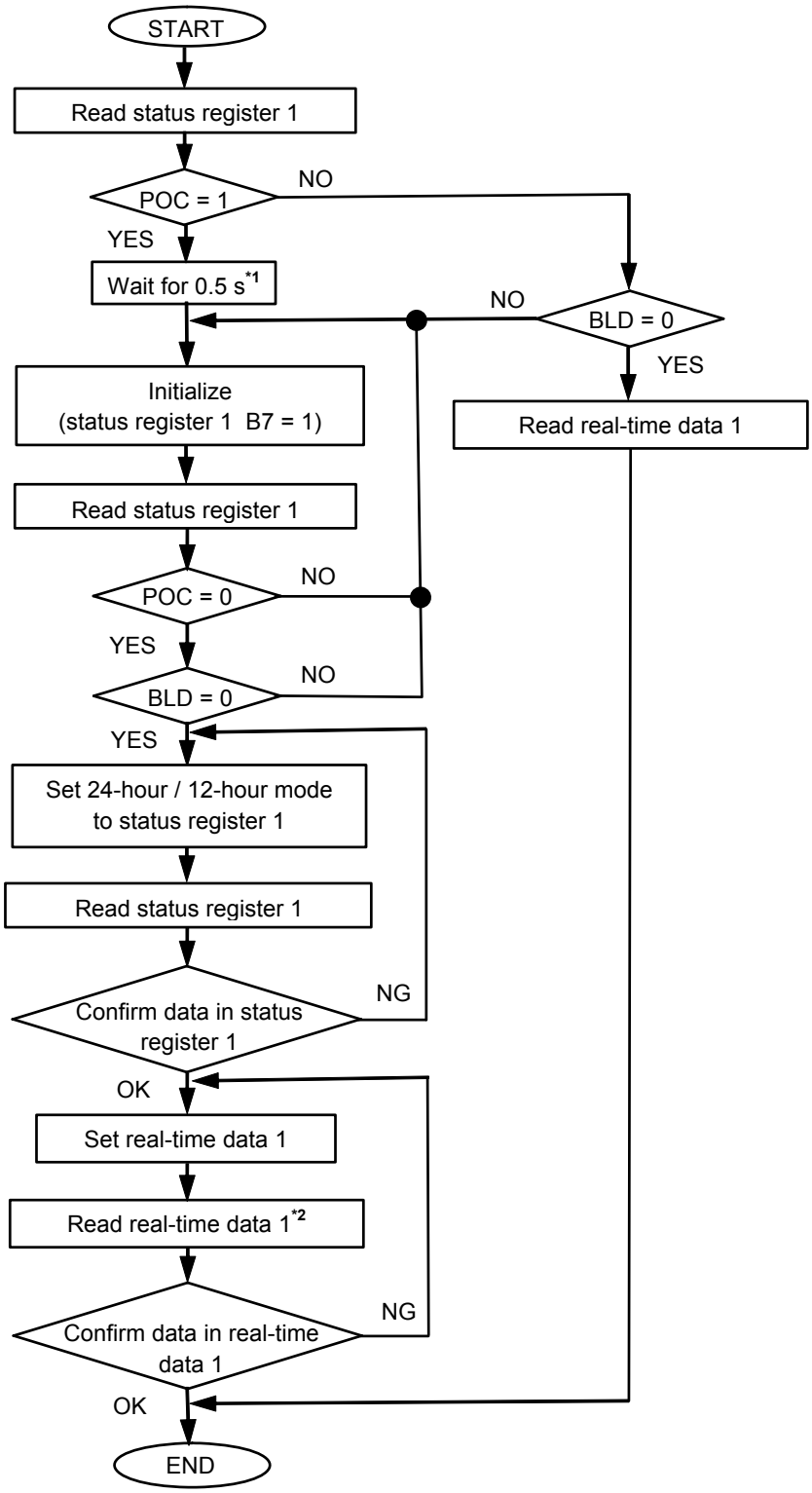


Figure 45 How to Reset

■ Flowchart of Initialization and Example of Real-time Data Set-up

Figure 46 is a recommended flowchart when the master device shifts to a normal operation status and initiates communication with the S-35391A. Regarding how to apply power, refer to "**■ Power-on Detection Circuit and Register Status**". It is unnecessary for users to comply with this flowchart of real-time data strictly. And if using the default data at initializing, it is also unnecessary to set up again.

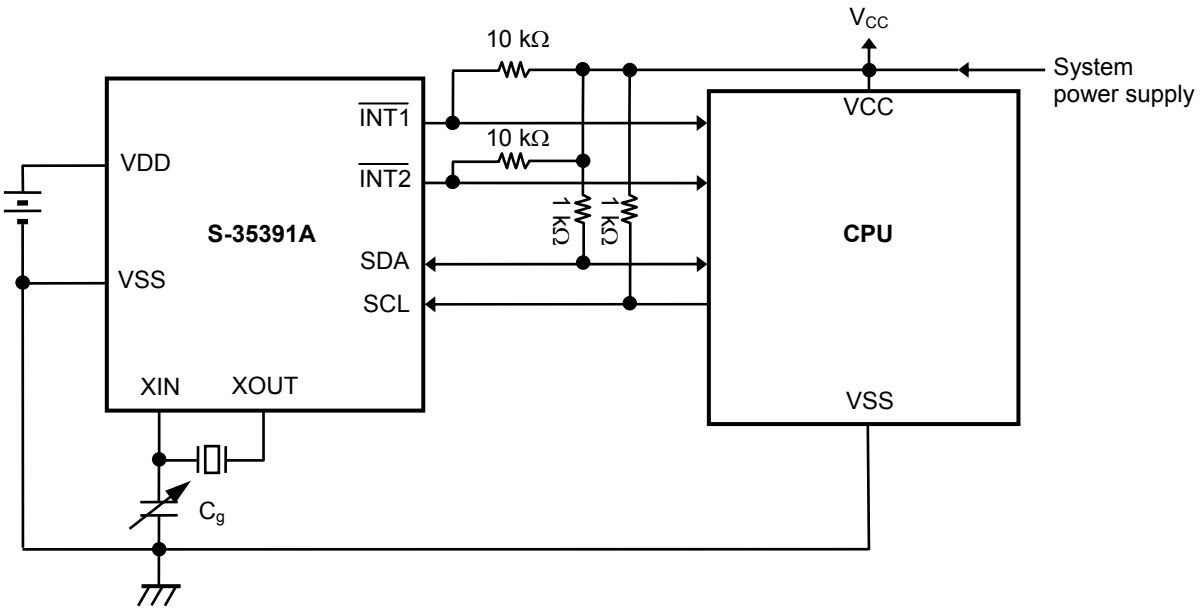


***1.** Do not communicate for 0.5 seconds since the power-on detection circuit is in operation.

***2.** Reading the real-time data 1 should be completed within 1 second after setting the real-time data 1.

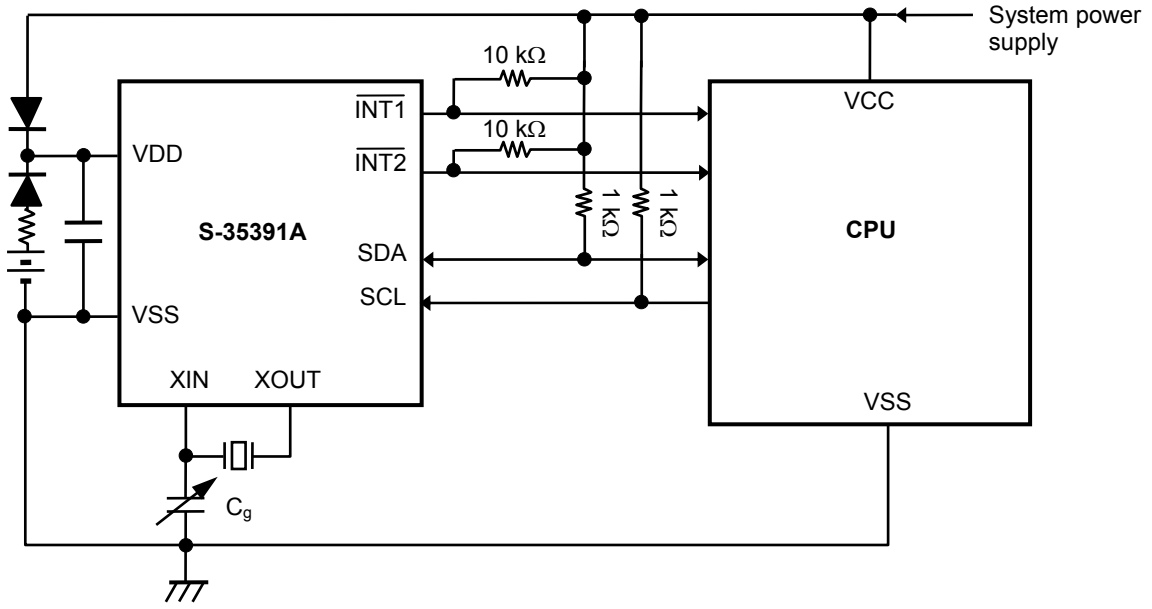
Figure 46 Example of Initialization Flowchart

■ Examples of Application Circuits



Caution 1. Because the I/O pin has no protective diode on the VDD side, the relation of $V_{CC} \geq V_{DD}$ is possible, but pay careful attention to the specifications.
2. Start communication under stable condition after power-on the power supply in the system.

Figure 47 Application Circuit 1



Caution Start communication under stable condition after power-on the power supply in the system.

Figure 48 Application Circuit 2

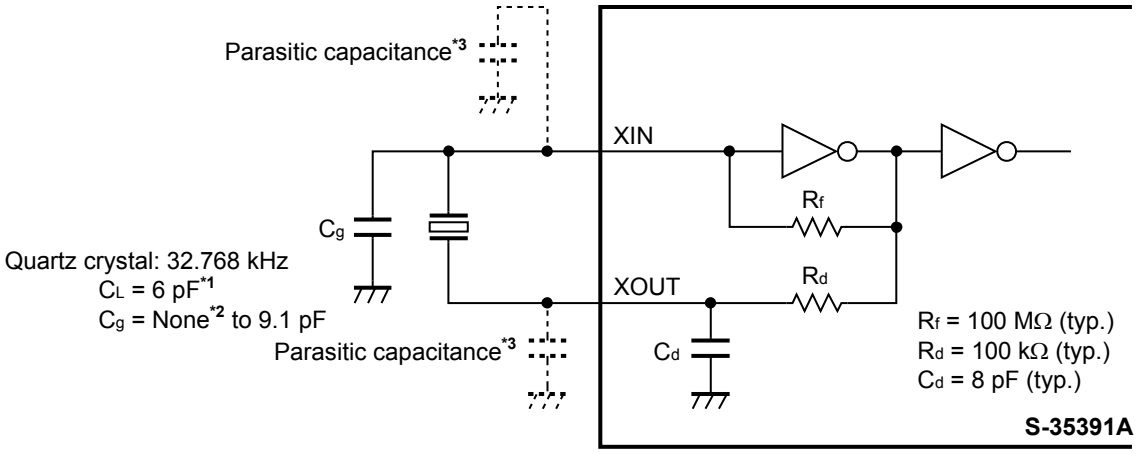
Caution The above connection diagrams do not guarantee operation. Set the constants after performing sufficient evaluation using the actual application.

■ Adjustment of Oscillation Frequency

1. Configuration of crystal oscillation circuit

Since the crystal oscillation circuit is sensitive to external noise (the clock accuracy is affected), the following measures are essential for optimizing the configuration.

- Place the S-35391A, quartz crystal, and external capacitor (C_g) as close to each other as possible.
- Increase the insulation resistance between pins and the substrate wiring patterns of XIN and XOUT.
- Do not place any signal or power lines close to the crystal oscillation circuit.
- Locating the GND layer immediately below the crystal oscillation circuit is recommended.
- Locate the bypass capacitor adjacent to the power supply pin of the S-35391A.



***1.** When setting the value for the quartz crystal's C_L as 7 pF, connect C_d externally if necessary.

***2.** The crystal oscillation circuit operates even when C_g is not connected. Note that the oscillation frequency is in the direction that it advances.

***3.** Design the board so that the parasitic capacitance is within 5 pF.

Figure 49 Connection Diagram 1

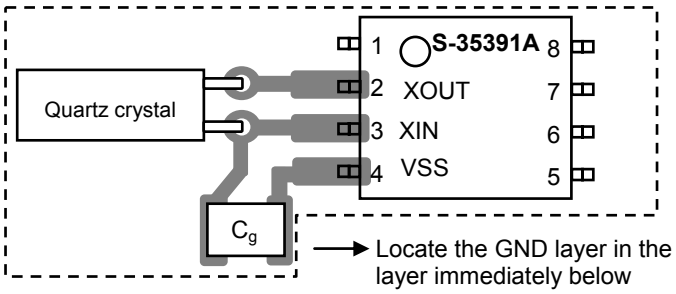


Figure 50 Connection Diagram 2

Caution 1. When using the quartz crystal with a C_L exceeding the rated value (7 pF) (e.g: C_L = 12.5 pF), oscillation operation may become unstable. Use a quartz crystal with a C_L value of 6 pF or 7 pF.

2. Oscillation characteristics is subject to the variation of each component such as substrate parasitic capacitance, parasitic resistance, quartz crystal, and C_g. When configuring a crystal oscillation circuit, pay sufficient attention for them.

2. Measurement of oscillation frequency

When the S-35391A is turned on, the internal power-on detector operates and a signal of 1 Hz is output from the $\overline{INT1}$ pin to select the quartz crystal and optimize the C_g value. Turn the power on and measure the signal with a frequency counter following the circuit configuration shown in **Figure 51**.
If 1 Hz signal is not output, the power-on detector does not operate normally. Turn off the power and then turn it on again. For how to apply power, refer to "■ **Power-on Detection Circuit and Register Status**".

Remark If the error range is ±1 ppm in relation to 1 Hz, the time is shifted by approximately 2.6 seconds per month (calculated using the following mode).
10^{-6} (1 ppm) × 60 seconds × 60 minutes × 24 hours × 30 days = 2.592 seconds

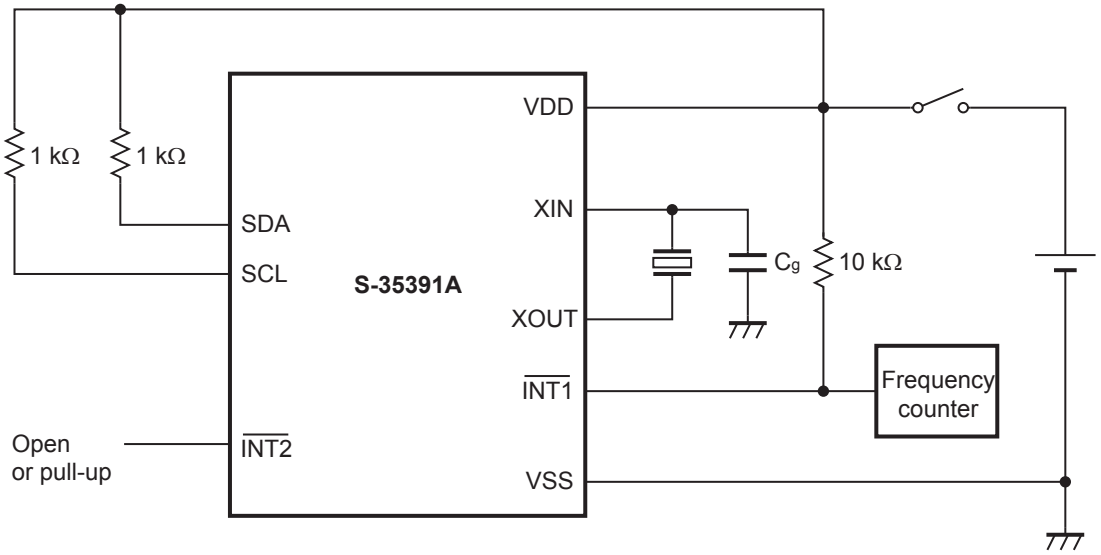


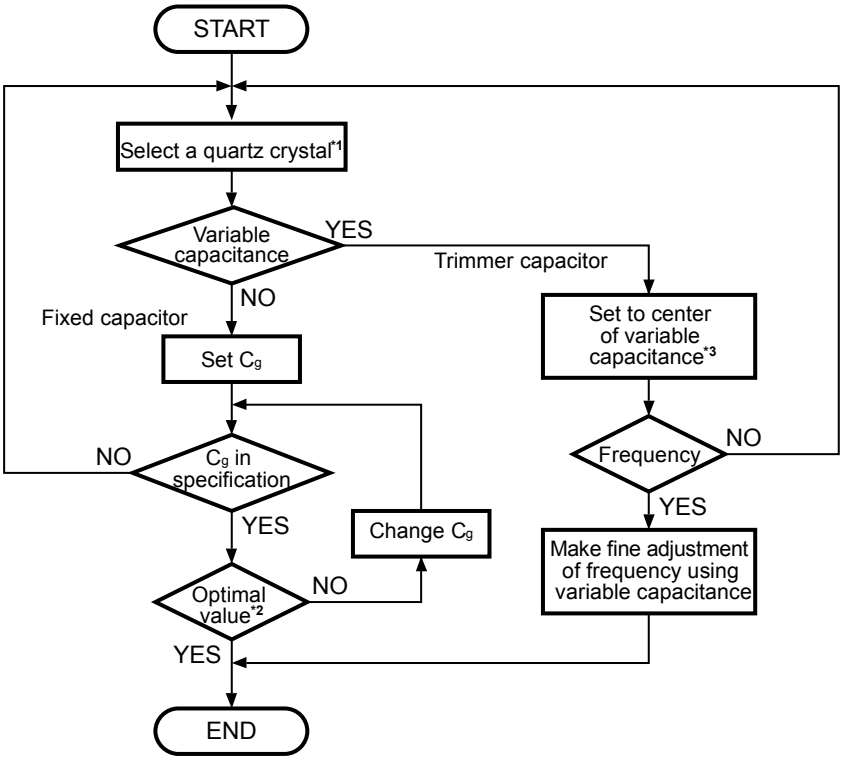
Figure 51 Configuration of Oscillation Frequency Measurement Circuit

Caution
1. **Use a high-accuracy frequency counter of 7 digits or more.**
2. **Measure the oscillation frequency under the usage conditions.**
3. **Since the 1 Hz signal continues to be output, initialization must be executed during normal operation.**

3. Adjustment of oscillation frequency

3. 1 Adjustment by setting C_g

Matching of the quartz crystal with the nominal frequency must be performed with the parasitic capacitance on the board included. Select a quartz crystal and optimize the C_g value in accordance with the flowchart below.



***1.** Request a quartz crystal manufacturer for a matching evaluation between the IC and the quartz crystal. The recommended quartz crystal characteristic values are, C_L value (load capacitance) = 6 pF, R_1 value (equivalent serial resistance) = 50 kΩ max.

***2.** The C_g value must be selected on the actual PCB since it is affected by parasitic capacitance. Select the external C_g value in a range of 0 pF to 9.1 pF.

***3.** Adjust the rotation angle of the variable capacitance so that the capacitance value is slightly smaller than the center, and confirm the oscillation frequency and the center value of the variable capacitance. This is done in order to make the capacitance of the center value smaller than one half of the actual capacitance value because a smaller capacitance value increases the frequency variation.

Figure 52 Quartz Crystal Setting Flow

Caution 1. The oscillation frequency varies depending on the ambient temperature and power supply voltage. Refer to "■ Characteristics (Typical Data)".

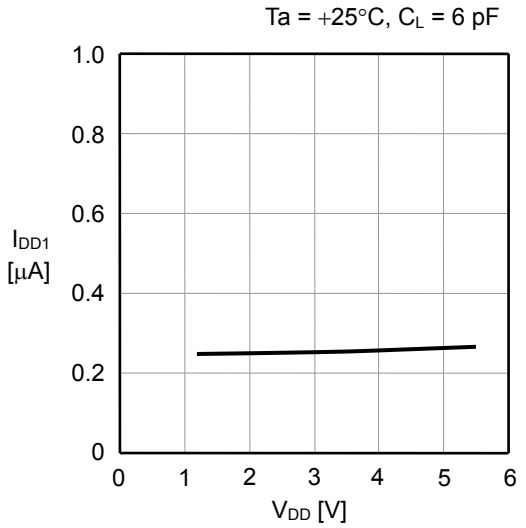
2. The 32.768 kHz quartz crystal operates more slowly at an operating temperature higher or lower than +20°C to +25°C. Therefore, it is recommended to set the oscillator to operate slightly faster at normal temperature.

■ Precautions

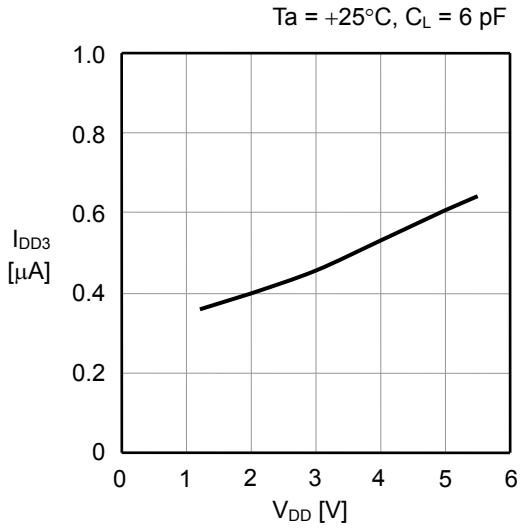
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

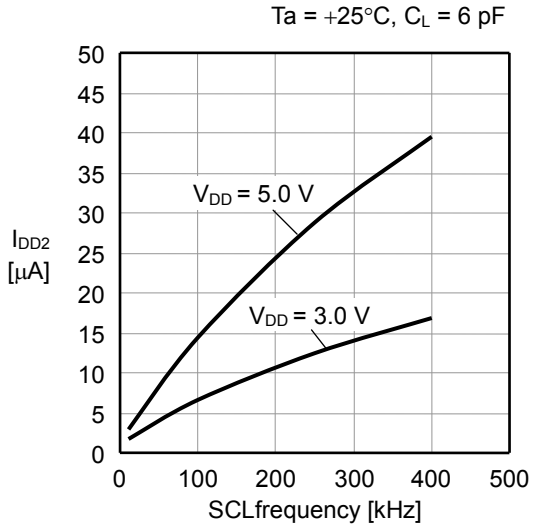
1. Standby current vs. V_{DD} characteristics



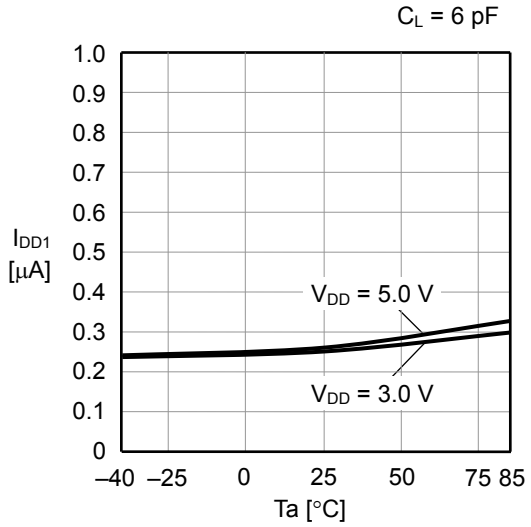
2. Current consumption when 32 kHz is output vs. V_{DD} characteristics



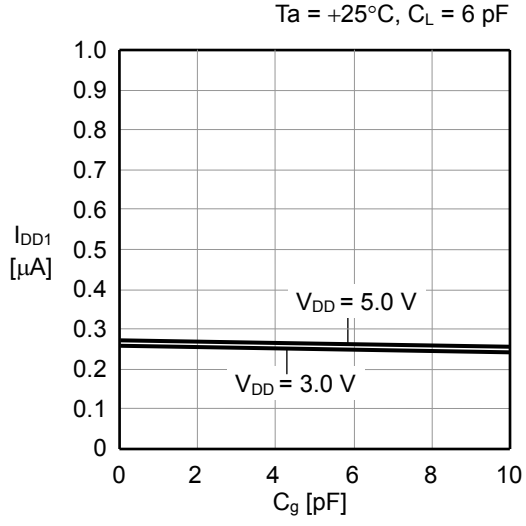
3. Current consumption during operation vs. Input clock characteristics



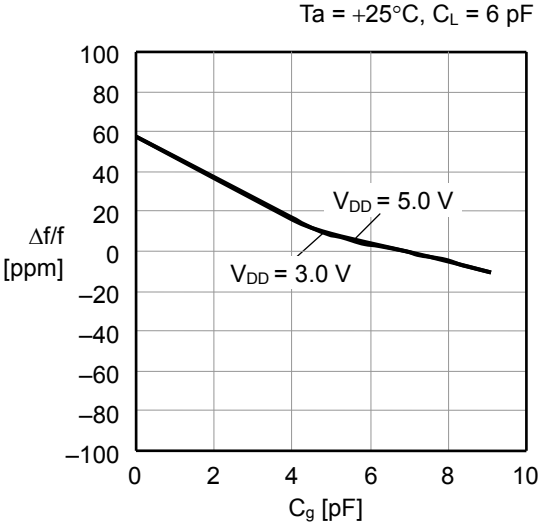
4. Standby current vs. Temperature characteristics



5. Standby current vs. C_g characteristics

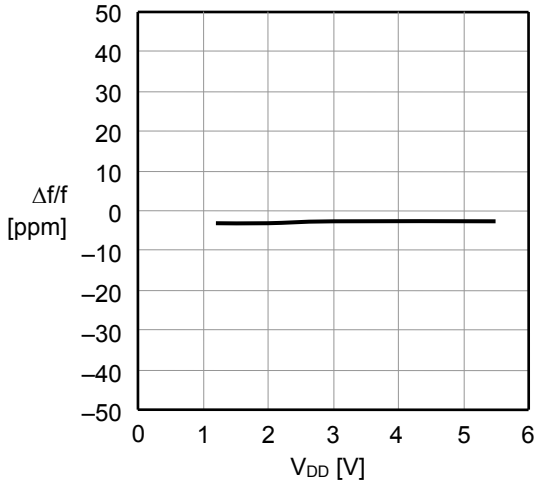


6. Oscillation frequency vs. C_g characteristics



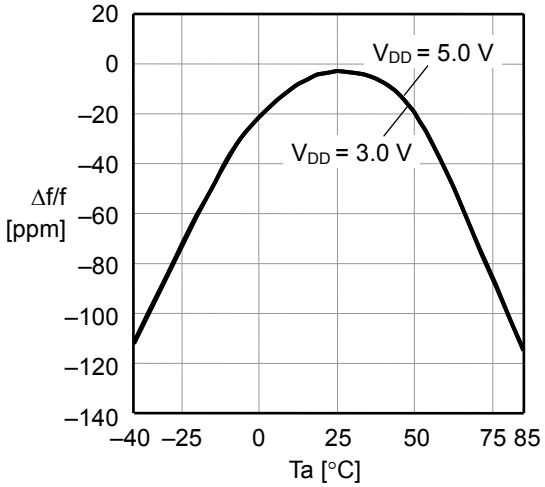
7. Oscillation frequency vs. V_{DD} characteristics

Ta = +25°C, C_g = 7.5 pF



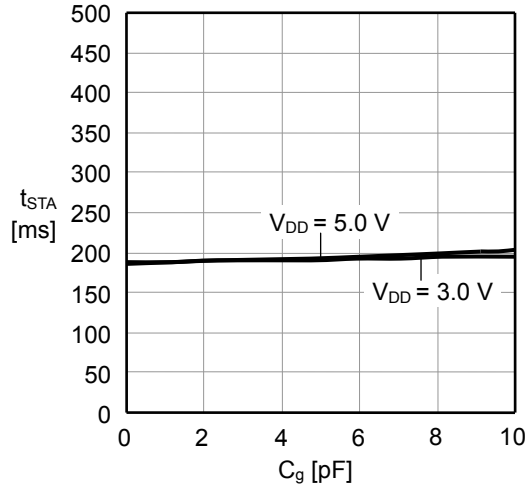
8. Oscillation frequency vs. Temperature characteristics

C_g = 7.5 pF



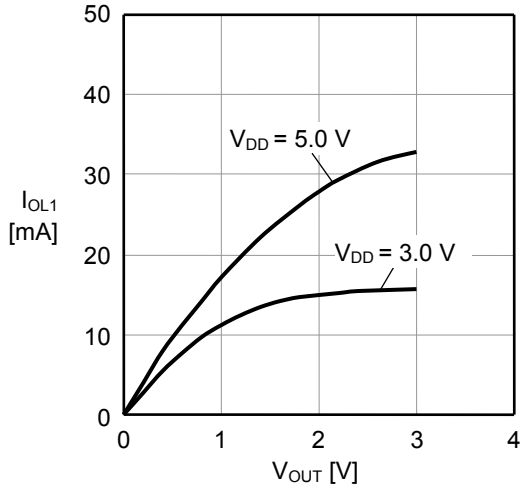
9. Oscillation start time vs. C_g characteristics

Ta = +25°C



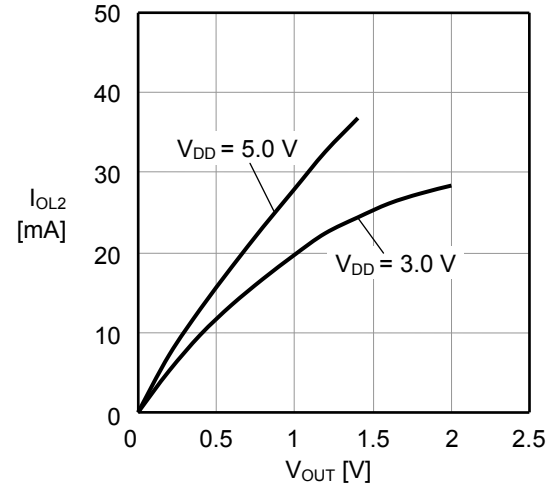
10. Output current characteristics 1 (V_{OUT} vs. I_{OL1})

$\overline{INT1}$ pin, $\overline{INT2}$ pin, Ta = +25°C



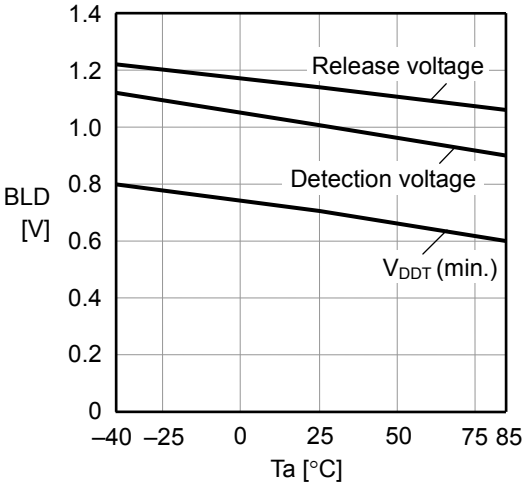
11. Output current characteristics 2 (V_{OUT} vs. I_{OL2})

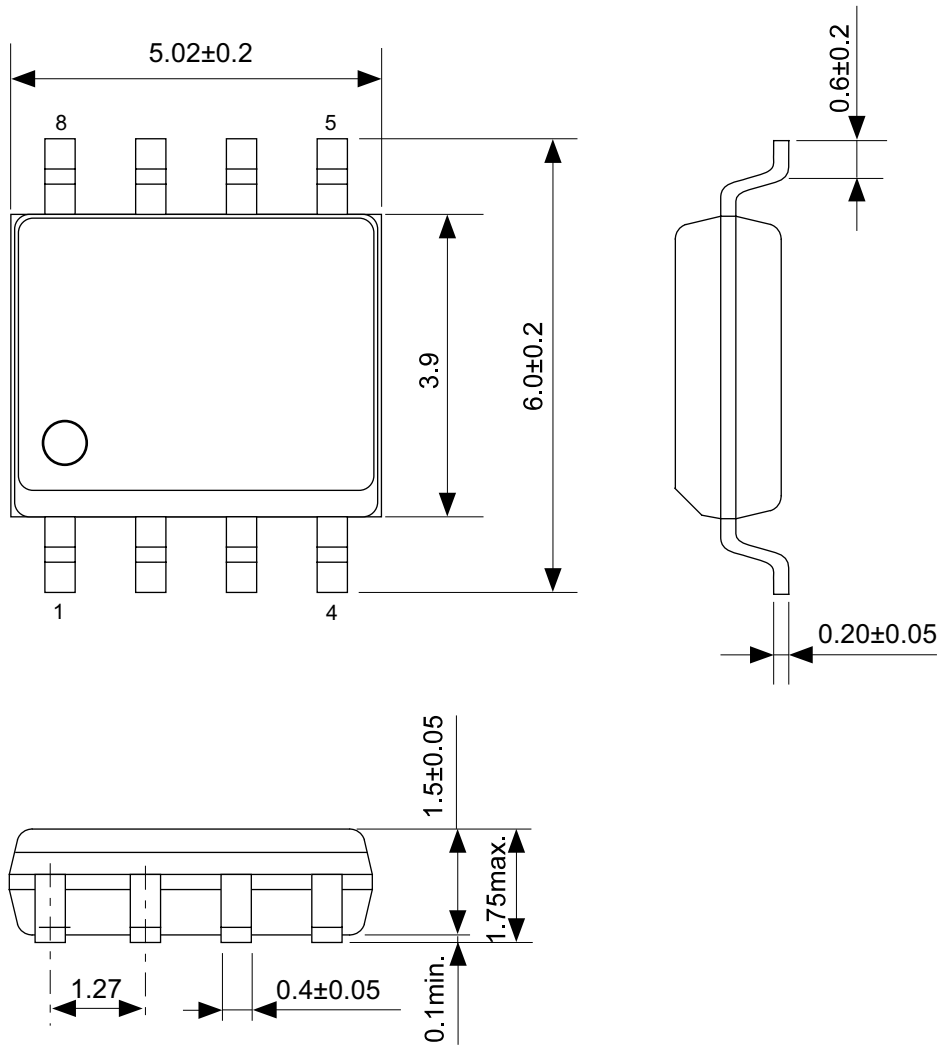
SDA pin, Ta = +25°C



12. BLD detection, release voltage, V_{DDT} (min.) vs. Temperature characteristics

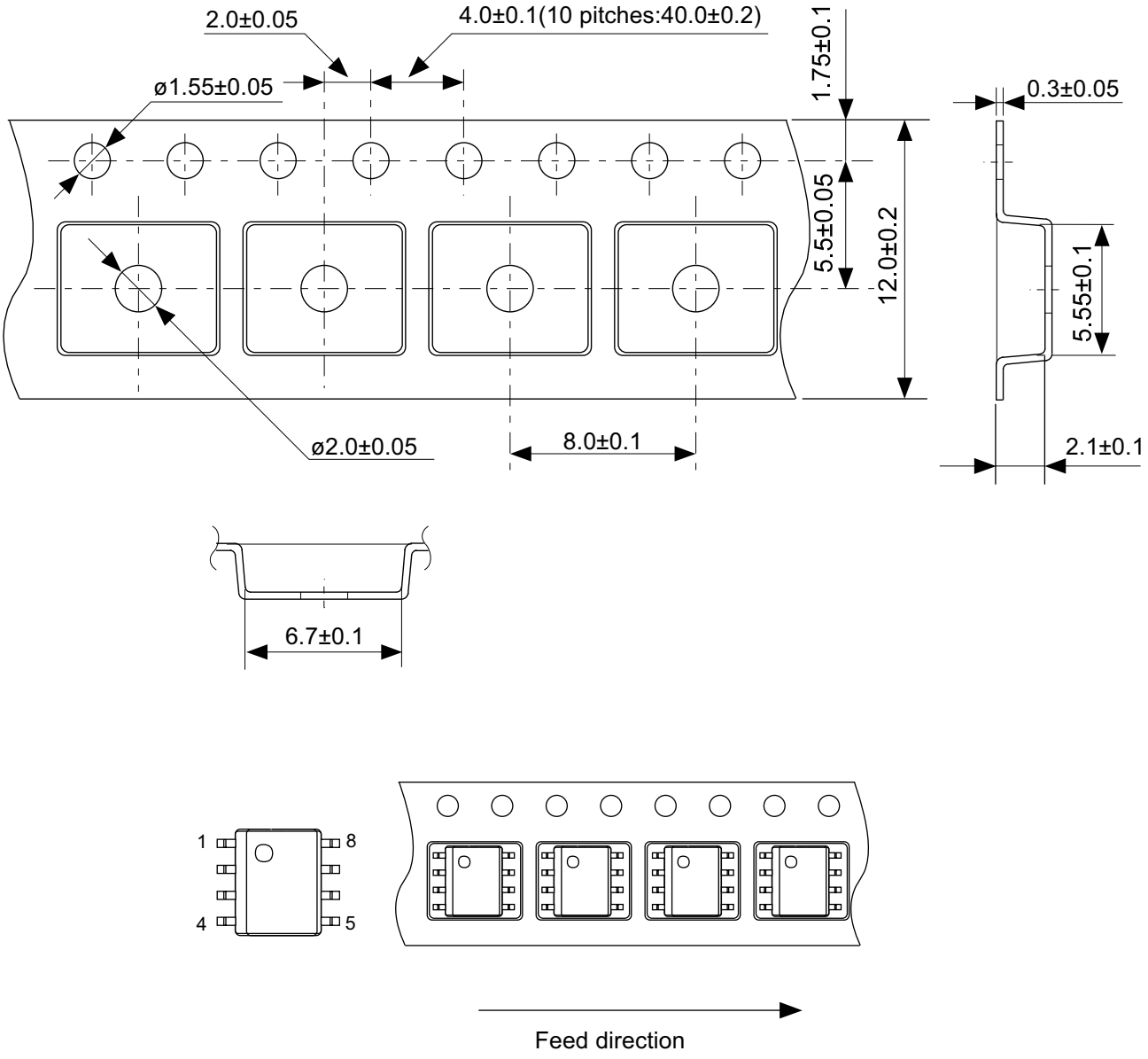
C_L = 6 pF





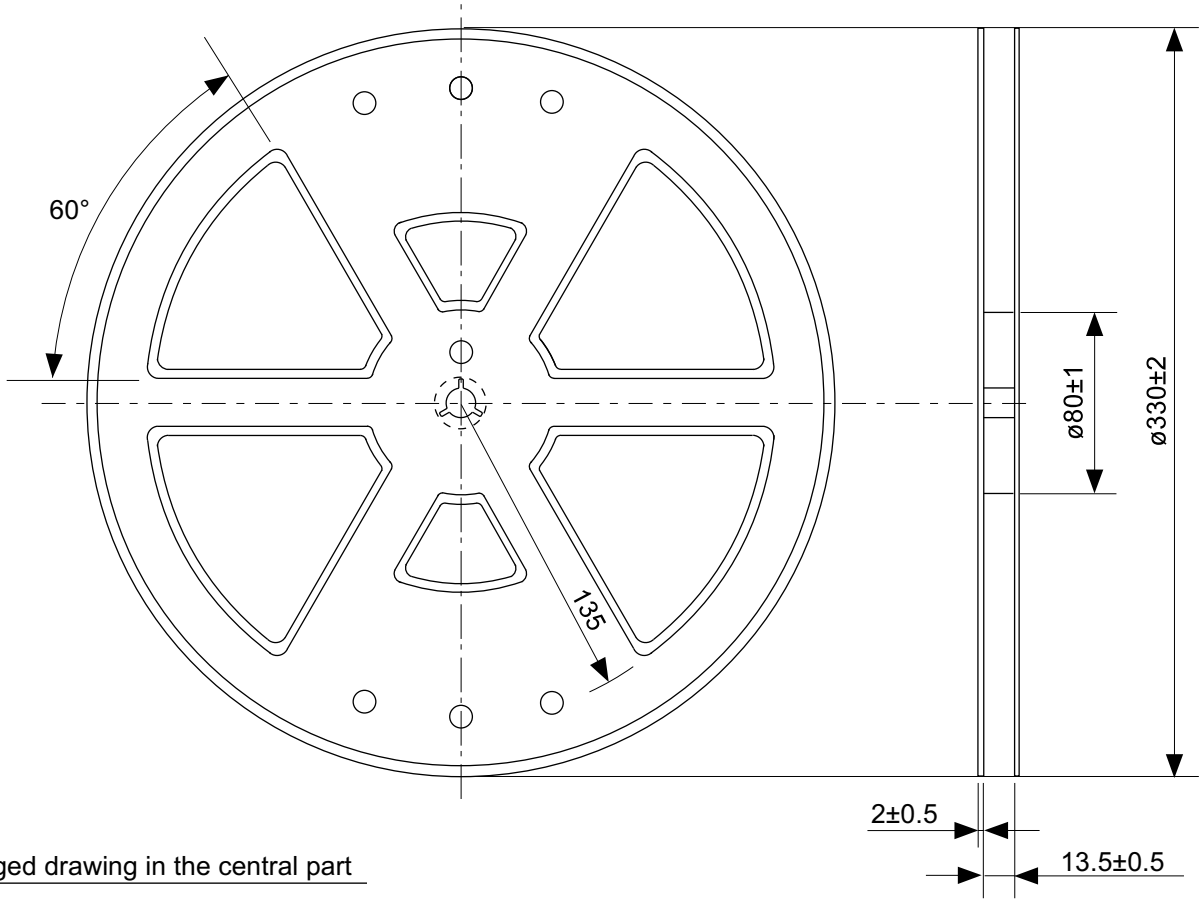
No. FJ008-A-P-SD-2.2

TITLE	SOP8J-D-PKG Dimensions
No.	FJ008-A-P-SD-2.2
ANGLE	
UNIT	mm
ABLIC Inc.	

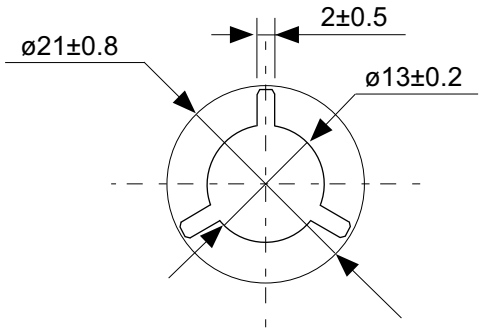


No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
ANGLE	
UNIT	mm
	ABLIC Inc.

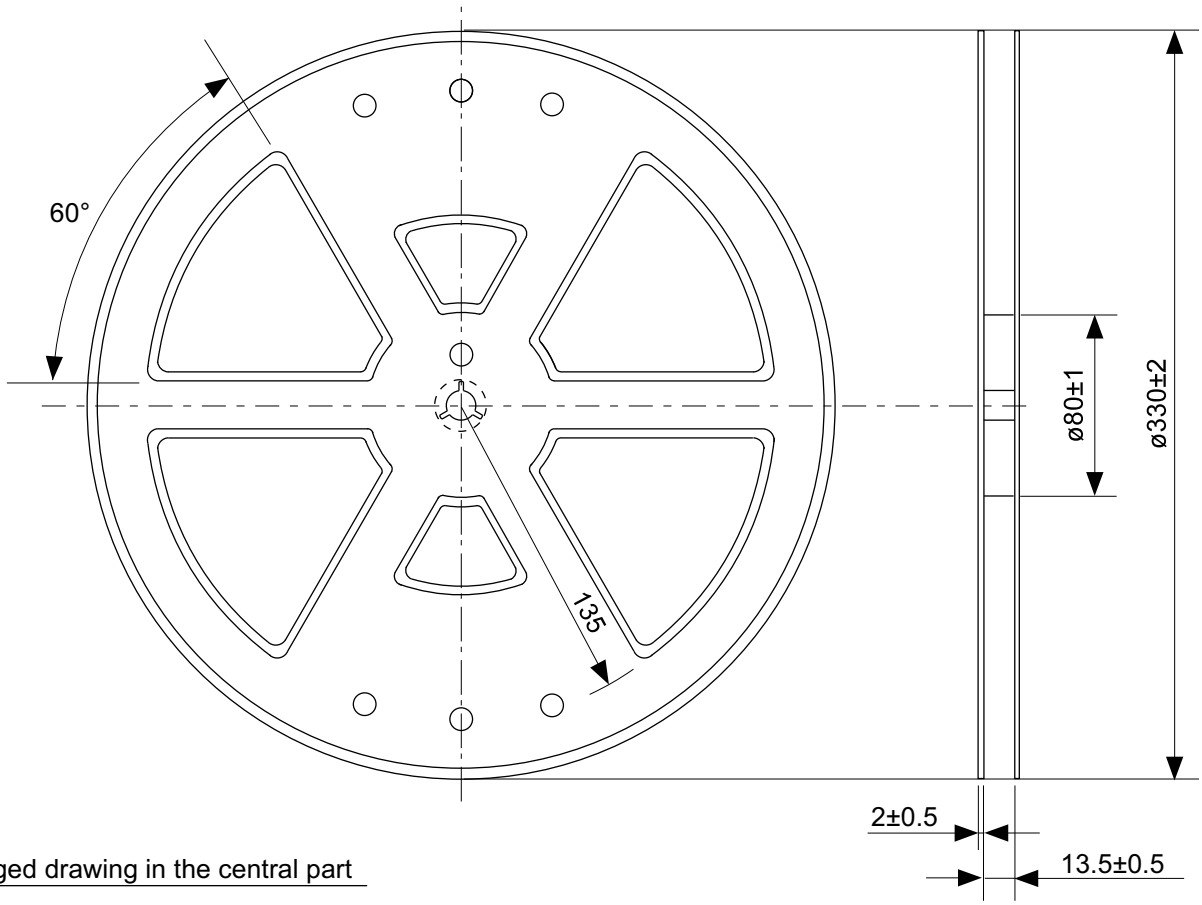


Enlarged drawing in the central part

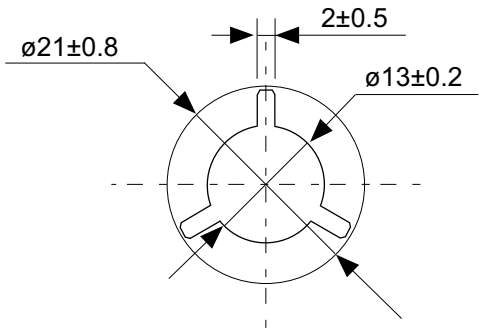


No. FJ008-D-R-SD-1.1

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-SD-1.1		
ANGLE		QTY.	2,000
UNIT	mm		
ABLIC Inc.			

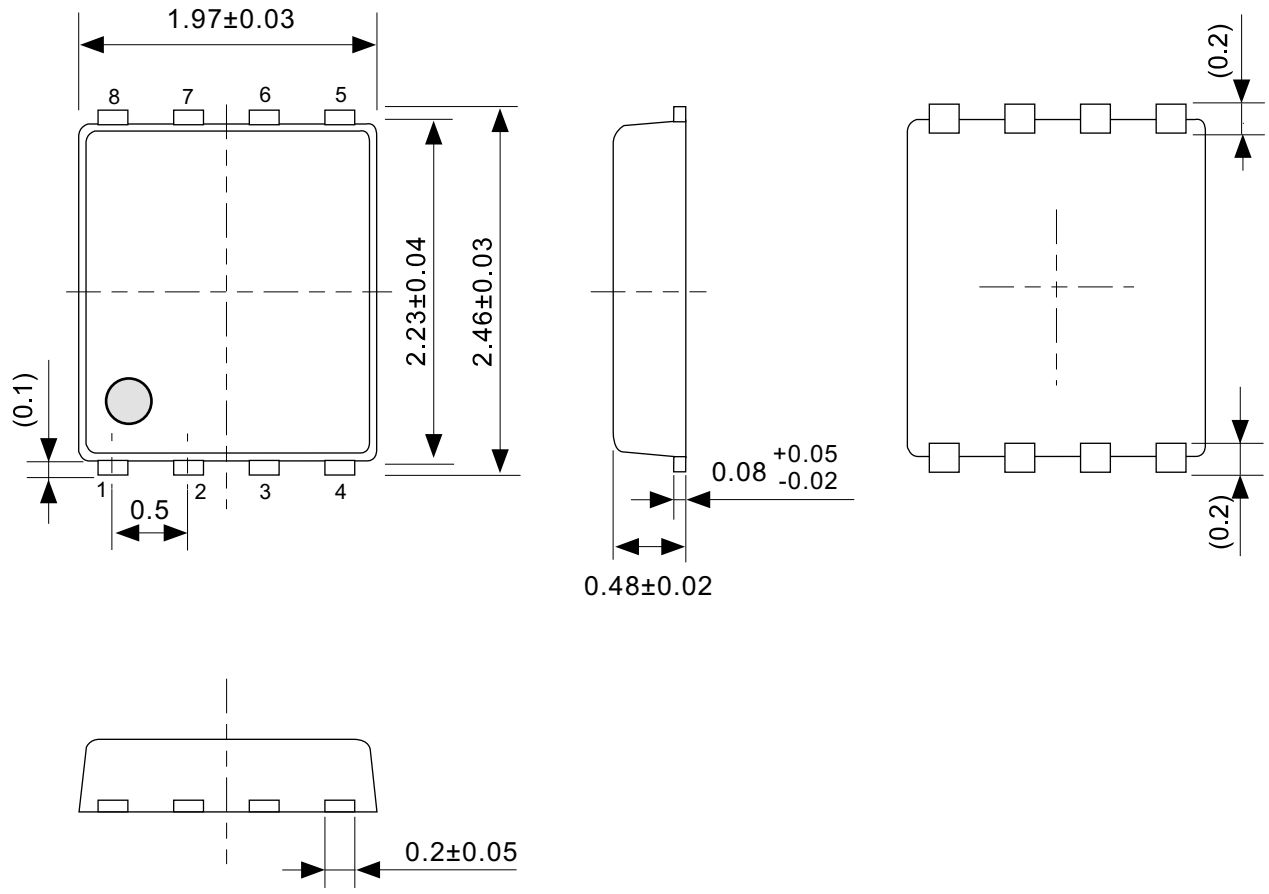


Enlarged drawing in the central part



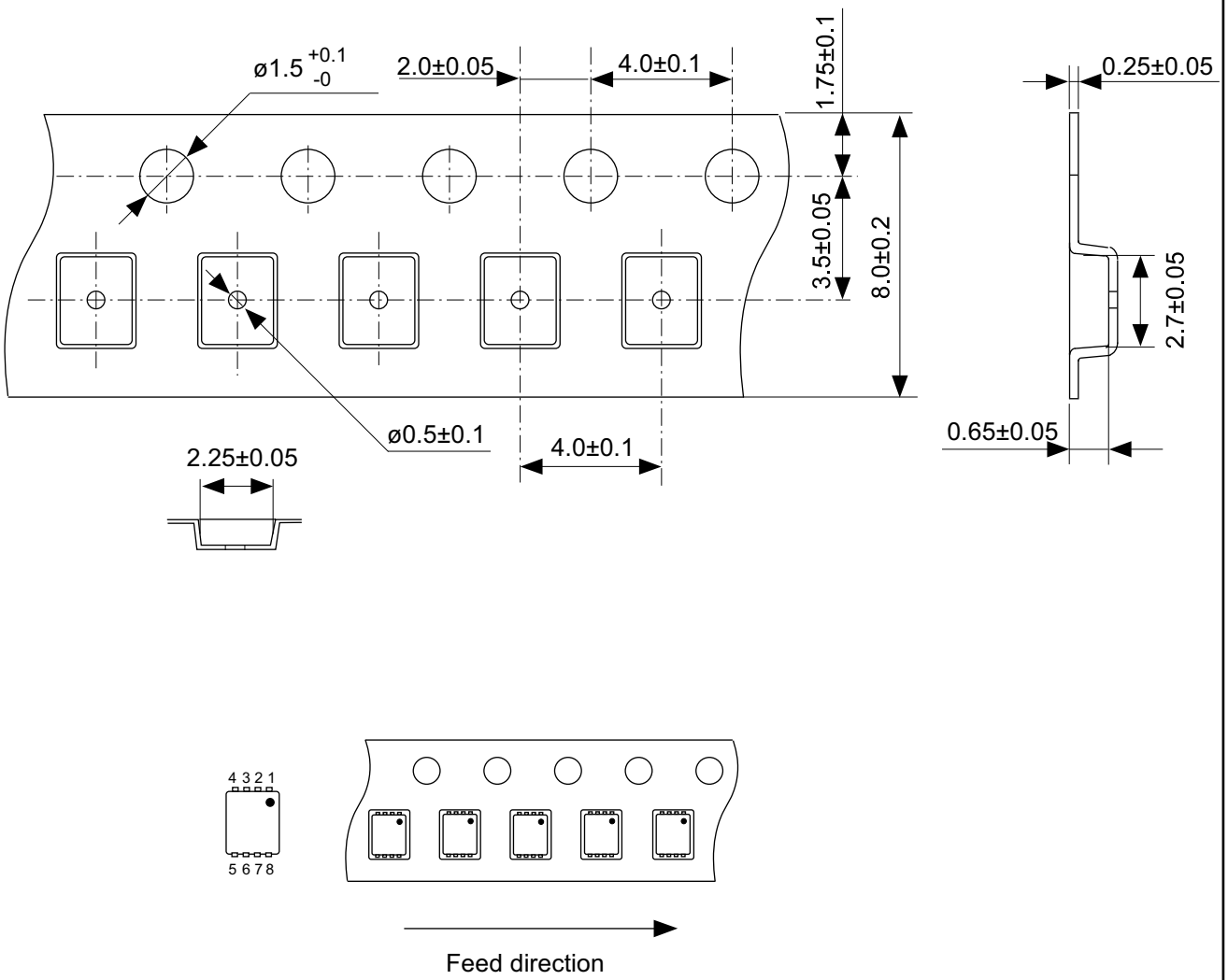
No. FJ008-D-R-S1-1.0

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-S1-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
	ABLIC Inc.		



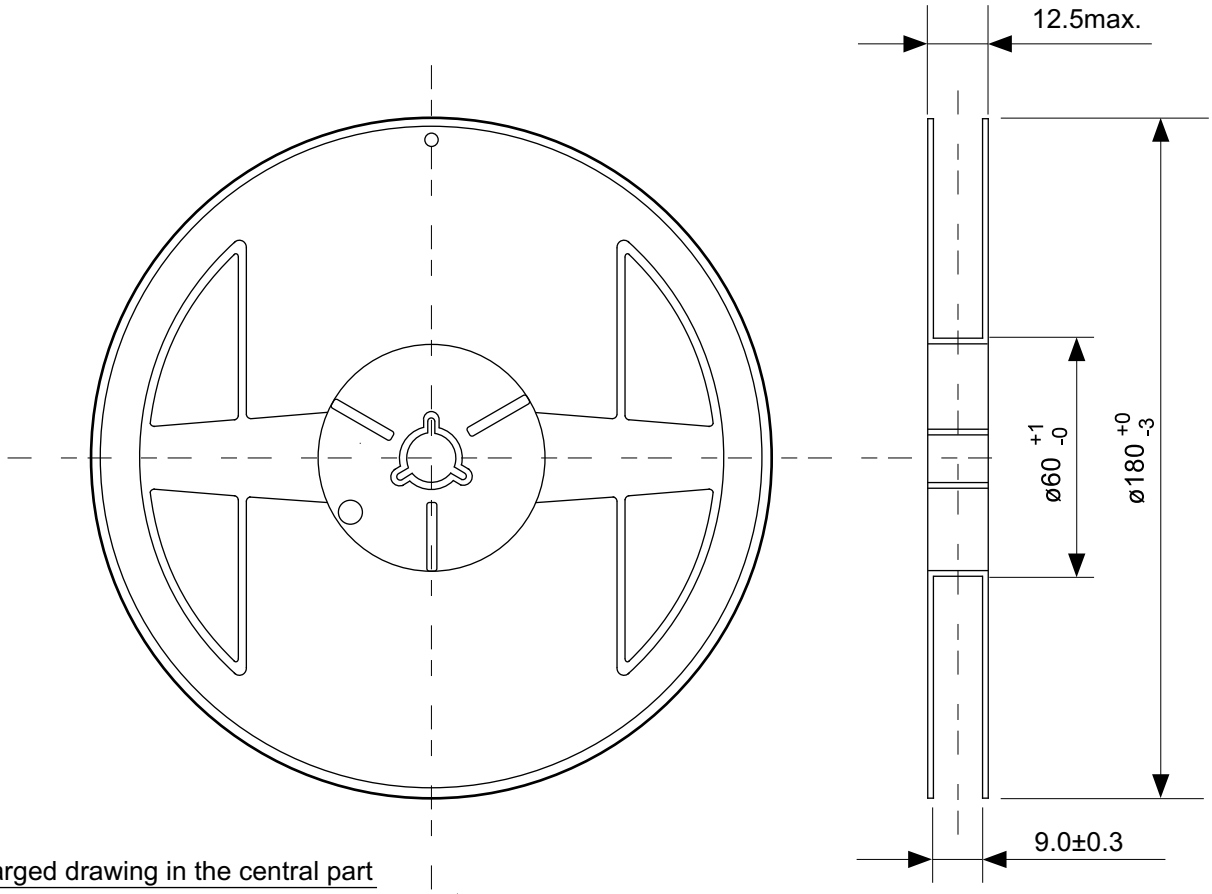
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

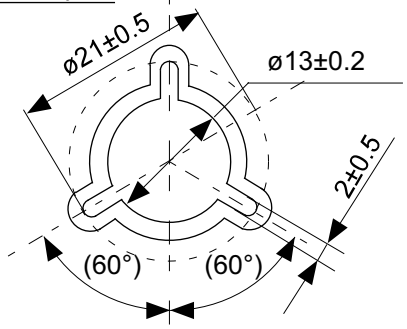


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

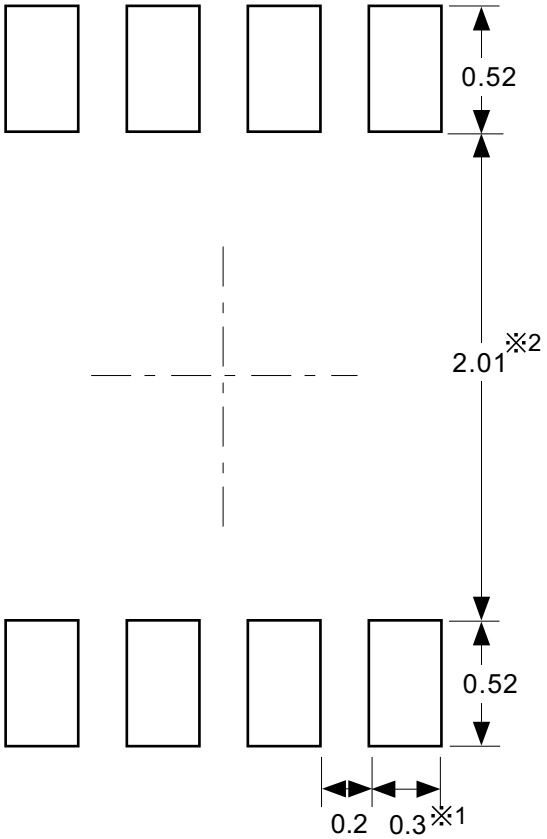


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
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2.4-2019.07