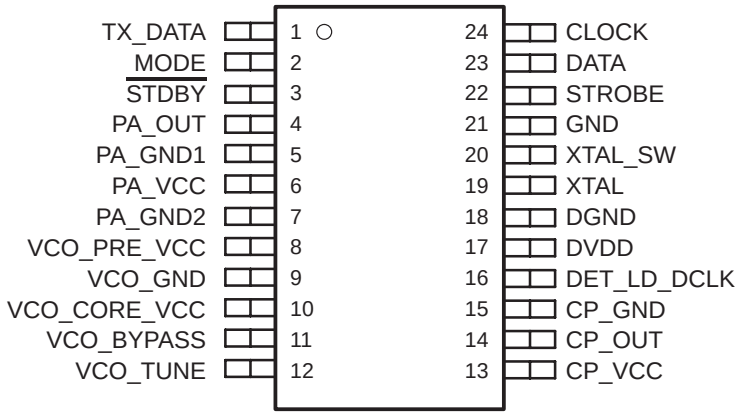
- **Single-Chip RF Transmitter for 315-MHz, 433-MHz, 868-MHz, and 915-MHz Industrial, Scientific, and Medical (ISM) Bands**
- **2.2-V to 3.6-V Operation**
- **Low Power Consumption**
- **FSK/OOK Operation**
- **Integer-N Synthesizer With Fully Integrated Voltage Controlled Oscillator (VCO)**
- **On-Chip Reference Oscillator and Phase-Locked Loop (PLL)**
- **Power Amplifier With 8-dBm Typical Output Power**
- **Programmable Brownout Detector**
- **Integrated Data Bit Synchronizer and Baud Rate Selection**
- **Flexible 3-Wire Serial Interface**
- **Minimal Number of External Components Required**
- **24-Pin Plastic Thin-Shrink Small Outline Package (TSSOP)**
- **Programmable XTAL Trimming**
- **Lock Detect Indicator**
- **Companion Transmitter to the TRF6903 Transceiver**

PW PACKAGE
(TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description

The TRF4903 single-chip solution is an integrated circuit intended for use as a low-cost multiband FSK or OOK transmitter to establish a frequency-programmable, half-duplex RF link. The multichannel transmitter is intended for digital (FSK, OOK) modulated applications in the North American and European 315-MHz, 433-MHz, 868-MHz, and 915-MHz ISM bands. The single-chip operates down to 2.2 V and is designed for low power consumption. The synthesizer has a typical channel spacing of better than 200 kHz and features a fully-integrated VCO. Only the PLL loop filter is external to the device.

Two fully-programmable operation modes, Mode0 and Mode1, allow extremely fast switching between two preprogrammed settings (for example, TX_frequency_0/TX_frequency_1; …) without reprogramming the device.

ISM band standards

Europe has assigned an unlicensed frequency band of 868 MHz to 870 MHz. This band is specifically defined for short range devices with duty cycles from 0.1% to 100% in several subbands. The new European frequency band, due to the duty cycle assignment, allows a reliable RF link and makes many new applications possible.

The North American unlicensed ISM band covers 902 MHz to 928 MHz (center frequency of 915 MHz) and is suitable for short range RF links.

transmitter

The transmitter consists of an integrated VCO and tank circuit, a complete integer-N synthesizer, and a power amplifier. The dividers, prescaler, and reference oscillator require only the addition of an external crystal and a loop filter to provide a complete PLL with a typical frequency resolution of better than 200 kHz.

Since the typical RF output power is approximately 8 dBm, no additional external RF power amplifier is necessary in most applications.

Four attenuation setting for the power amplifier are offered. This feature allows the user to fine tune the amplifier for optimal output power.

baseband interface

The TRF4903 can easily be interfaced to a baseband processor such as the Texas Instruments MSP430 ultralow-power microcontroller (see Figure 1). The TRF4903 serial control registers are programmed by the MSP430 and the MSP430 performs baseband operations in the software.

A synchronized data clock, programmable for most common data rates, is provided by the TRF4903. During transmit, the data clock can be used to clock the transmit data from the microcontroller to the TRF4903 at predefined data rates.

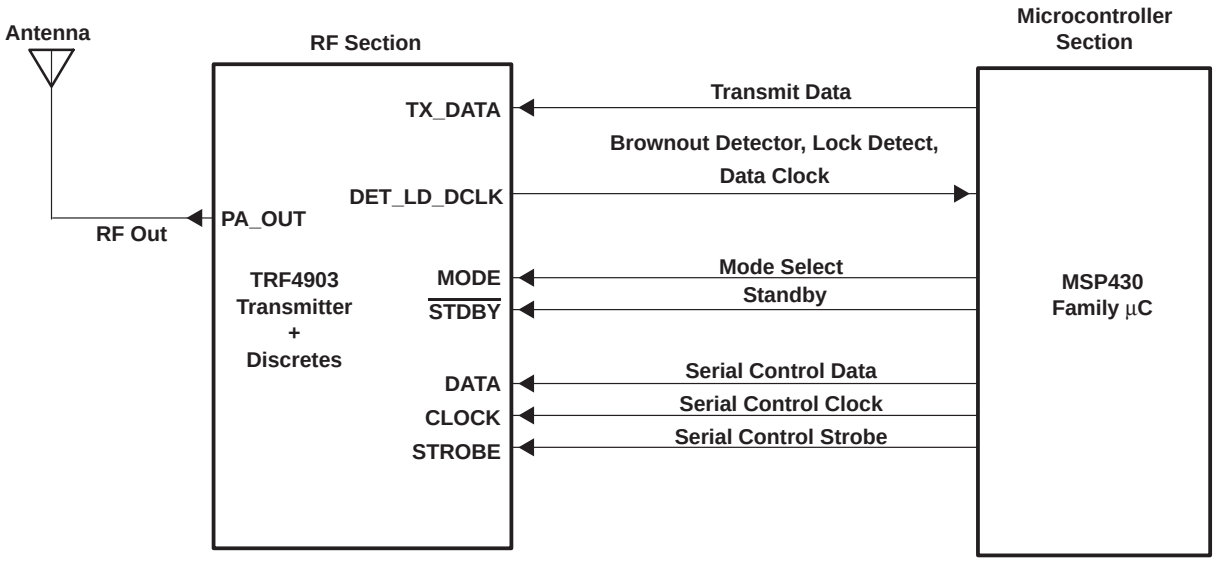
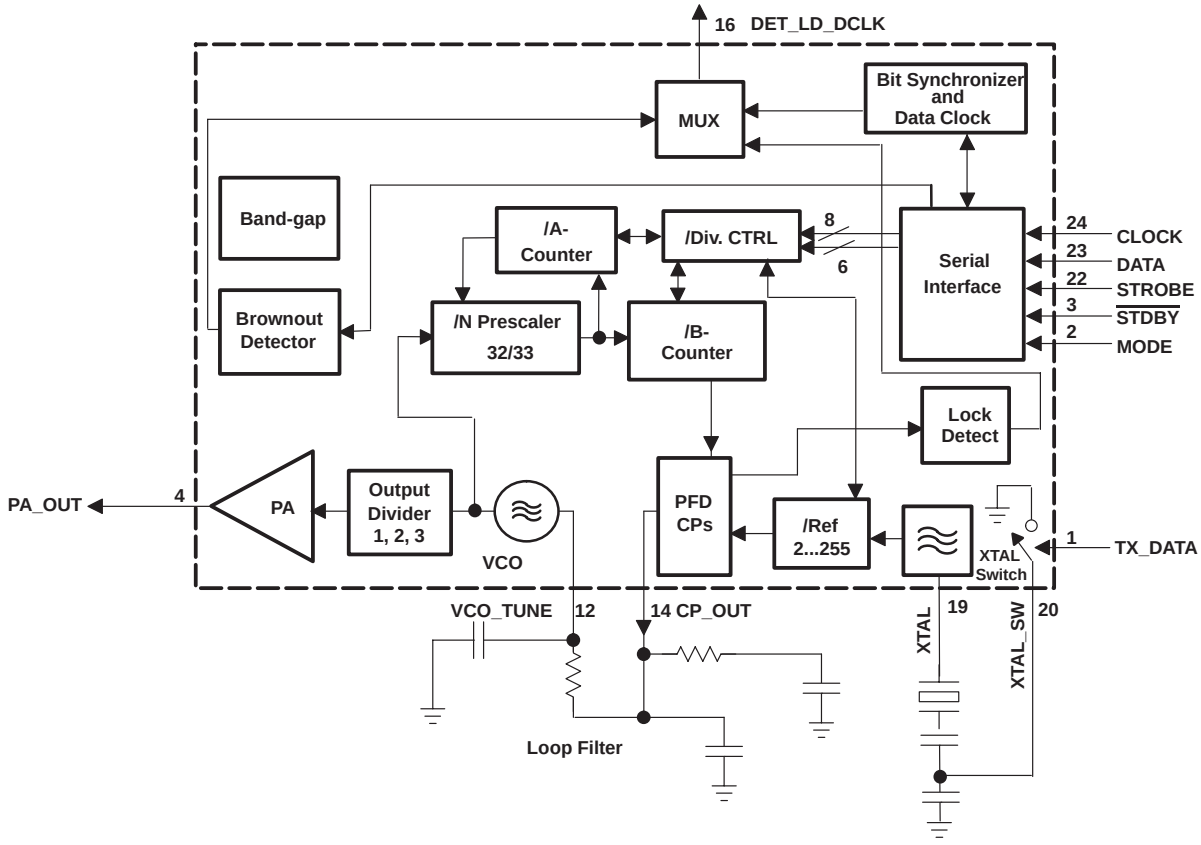


Figure 1. System Block Diagram for Interfacing to the MSP430 Microcontroller

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLOCK	24	I	Serial interface clock signal input
CP_GND	15		Charge pump ground
CP_OUT	14	O	Charge pump output
CP_VCC	13		Charge pump supply voltage
DATA	23	I	Serial interface data signal input
DET_LD_DCLK	16	O	Brownout detector (active high), PLL lock detect (active high), and data clock multiplexed output
DGND	18		Digital and XTAL oscillator ground
DVDD	17		Digital and XTAL oscillator power supply
GND	21		Substrate ground
MODE	2	I	Mode select input
PA_GND1	5		Power amplifier ground
PA_GND2	7		Power amplifier ground
PA_OUT	4	O	Power amplifier output
PA_VCC	6		Power amplifier supply voltage
$\overline{\text{STDBY}}$	3	I	Standby input signal; active low
STROBE	22	I	Serial interface strobe signal
TX_DATA	1	I	Buffered TX data input
VCO_BYPASS	11	I	VCO bypass; connect to ground through a 100-pF capacitor
VCO_GND	9		VCO ground
VCO_TUNE	12	I	Tuning voltage for the integrated VCO
VCO_CORE_VCC	10		VCO core supply voltage
VCO_PRE_VCC	8		Divider and prescaler supply voltage
XTAL	19	I/O	Connection to an external crystal reference
XTAL_SW	20	I	Connection to external capacitor, which sets the frequency deviation of the transmitted signal

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range . . . . . −0.6 to 4.5 Vdc
Input voltage, logic signals . . . . . −0.6 to 4.5 Vdc
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
ESD protection, human body model (HBM) . . . . . 2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog supply voltage		2.2		3.6	V
Digital supply voltage		2.2		3.6	V
Operating free-air temperature		−40		85	°C

dc electrical characteristics, V_{CC} = 2.7 V, T_A = 25°C

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standby current		$\overline{\text{STDBY}}$ low		0.6	4	μA
TX current, PA disabled. PLL, VCO, dividers, and reference active		315-MHz band		12	15	mA
		433-MHz band		11	14	
		868-MHz band		10	12	
		915-MHz band		10	12	
TX current‡, PA enabled. PLL, VCO, dividers, reference, and data clock active	0-dB attenuation	315-MHz band		37	43	mA
	10-dB attenuation	315-MHz band		30		
	20-dB attenuation	315-MHz band		29		
	0-dB attenuation	433-MHz band		36	42	
	10-dB attenuation	433-MHz band		29		
	20-dB attenuation	433-MHz band		28		
	0-dB attenuation	868-MHz band		35	40	
	10-dB attenuation	868-MHz band		28		
	20-dB attenuation	868-MHz band		27		
	0-dB attenuation	915-MHz band		35	40	
	10-dB attenuation	915-MHz band		28		
	20-dB attenuation	915-MHz band		27		

‡ The TX current consumption is dependent upon the external PA matching circuit. The matching network is normally designed to achieve the highest output power at the 0-dB attenuation setting. Changing the external matching components to optimize the output power for other attenuation settings alters the typical current consumption from the typical values noted.

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		V_{DD}−0.4		V_{DD}	V
V_{IL}	Low-level input voltage		0		0.4	V
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA	V_{DD}−0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 mA			0.4	V
	Digital input leakage current			<0.01		μA

VCO/output divider

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range: 315-MHz band	Low-side injection, A<1:0> = 11	304	315	316	MHz
Frequency range: 433-MHz band	High-side injection, A<1:0> = 10	430	433	450	MHz
Frequency range: 868-MHz band	High-side injection, A<1:0> = 01	868	869	870	MHz
Frequency range: 915-MHz band	Low-side injection, A<1:0> = 01	902	915	928	MHz
Closed loop phase noise	Frequency offset = 50 kHz		−77		dBc/Hz
	Frequency offset = 200 kHz		−90		
Tuning voltage		0.1		VCC at terminal 11	V

ac electrical characteristics, V_{CC} = 2.7 V, T_A = 25°C (continued)

impedances and loads

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PA_OUT			See Figure 6		

transmitter (XTAL, PLL, VCO, and PA), 315-MHz band

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX frequency range	A<1:0> = 11	304	315	316	MHz
Output power†	0-dB attenuation		8		dBm
	10-dB attenuation		−2		
	20-dB attenuation		−12		
	Disabled, B<3> = 0		−80		
Second harmonic			−25		dBc
Third harmonic			−30		dBc
DCLK spurious at $f_C \pm f_{DCLK}$§	DCLK active: E<15> = 1, E<12:11> = 01		−28		dBc
Frequency deviation‡	FSK		±32		kHz
Power ON-OFF ratio	OOK, 0-dB mode		75		dB
Maximum data rate (NRZ)	FSK		64		kbit/s
	OOK		32		

† Matched to 50 Ω using external matching network.
‡ Dependent upon external circuitry.
§ This spur is only present if DCLK is active. The resulting spur is within modulation (OOK or FSK) bandwidth and is considered a modulation product. Within the authorized bands, this spur does not violate FCC or ETSI regulatory compliance.

transmitter (XTAL, PLL, VCO, and PA), 433-MHz band

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX frequency range	A<1:0> = 10	430	433	450	MHz
Output power†	0-dB attenuation		8		dBm
	10-dB attenuation		−2		
	20-dB attenuation		−12		
	Disabled, B<3> = 0		−80		
Second harmonic			−25		dBc
Third harmonic			−30		dBc
DCLK spurious at $f_C \pm f_{DCLK}$§	DCLK active: E<15> = 1, E<12:11> = 01		−28		dBc
Frequency deviation‡	FSK		±32		kHz
Power ON-OFF ratio	OOK, 0-dB mode		75		dB
Maximum data rate (NRZ)	FSK		64		kbit/s
	OOK		32		

† Matched to 50 Ω using external matching network.
‡ Dependent upon external circuitry.
§ This spur is only present if DCLK is active. The resulting spur is within modulation (OOK or FSK) bandwidth and is considered a modulation product. Within the authorized bands, this spur does not violate FCC or ETSI regulatory compliance.

ac electrical characteristics, V_{CC} = 2.7 V, T_A = 25°C (continued)

transmitter (XTAL, PLL, VCO, and PA), 868-MHz band

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX frequency range	A<1:0> = 11	868	869	870	MHz
Output power†	0-dB attenuation		8		dBm
	10-dB attenuation		−2		
	20-dB attenuation		−12		
	Disabled, B<3> = 0		−80		
Second harmonic			−25		dBc
Third harmonic			−30		dBc
DCLK spurious at $f_C \pm f_{DCLK}$§	DCLK active: E<15> = 1, E<12:11> = 01		−28		dBc
Frequency deviation‡	FSK		±32		kHz
Power ON-OFF ratio	OOK, 0-dB mode		75		dB
Maximum data rate (NRZ)	FSK		64		kbit/s
	OOK		32		

† Matched to 50 Ω using external matching network.
‡ Dependent upon external circuitry.
§ This spur is only present if DCLK is active. The resulting spur is within modulation (OOK or FSK) bandwidth and is considered a modulation product. Within the authorized bands, this spur does not violate FCC or ETSI regulatory compliance.

transmitter (XTAL, PLL, VCO, and PA), 915-MHz band

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX frequency range	A<1:0> = 11	902	915	928	MHz
Output power†	0-dB attenuation		8		dBm
	10-dB attenuation		−2		
	20-dB attenuation		−12		
	Disabled, B<3> = 0		−80		
Second harmonic			−25		dBc
Third harmonic			−30		dBc
DCLK spurious at $f_C \pm f_{DCLK}$§	DCLK active: E<15> = 1, E<12:11> = 01		−28		dBc
Frequency deviation‡	FSK		±32		kHz
Power ON-OFF ratio	OOK, 0-dB mode		75		dB
Maximum data rate (NRZ)	FSK		64		kbit/s
	OOK		32		

† Matched to 50 Ω using external matching network.
‡ Dependent upon external circuitry.
§ This spur is only present if DCLK is active. The resulting spur is within modulation (OOK or FSK) bandwidth and is considered a modulation product. Within the authorized bands, this spur does not violate FCC or ETSI regulatory compliance.

ac electrical characteristics, V_{CC} = 2.7 V, T_A = 25°C (continued)

XTAL

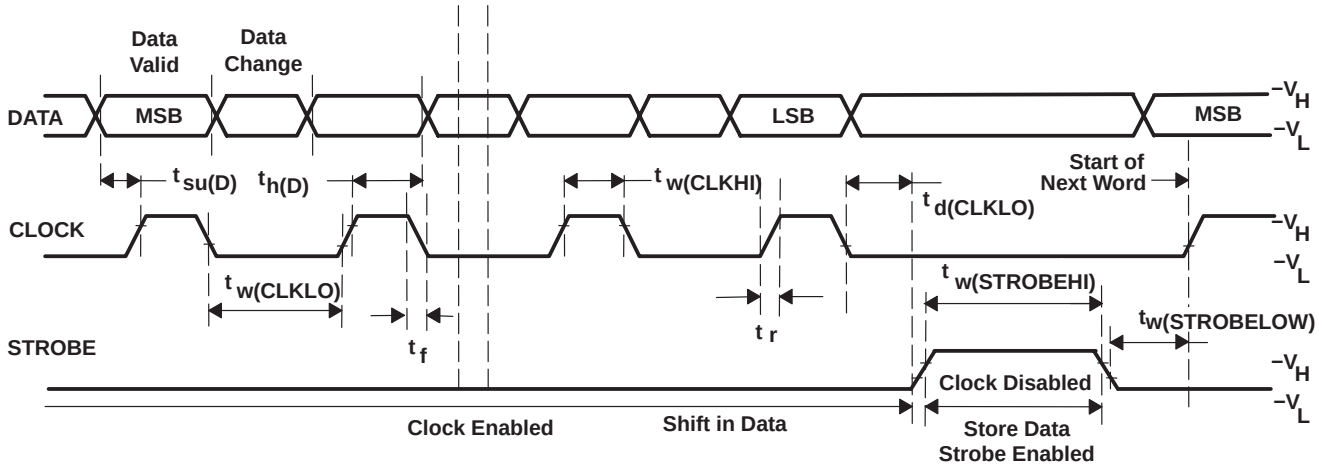
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range		9.5		20	MHz

brownout detector

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage threshold, V_{det}	Set by B<2:1>	2.2		2.8	V
Voltage steps (ΔV)			200		mV
Number of steps			4		
Output level	Connected to typical input port of microcontroller		CMOS		

timing data for serial interface

PARAMETER		MIN	TYP	MAX	UNIT
$f_{(CLOCK)}$	Clock frequency			20	MHz
$t_{w(CLKHI)}$	Clock high-time pulse width, clock high		20		ns
$t_{w(CLKLO)}$	Clock low-time pulse width, clock low		20		ns
$t_{su(D)}$	Setup time, data valid before CLOCK↑		0		ns
$t_{h(D)}$	Hold time, data valid after CLOCK ↑		10		ns
$t_{d(CLKLO)}$	Delay time of CLOCK low before STROBE high		20		ns
$t_{w(STROBEHI)}$	STROBE high-time pulse width, STROBE high		20		ns
$t_{w(STROBELO)}$	STROBE low-time pulse width, STROBE low		20		ns

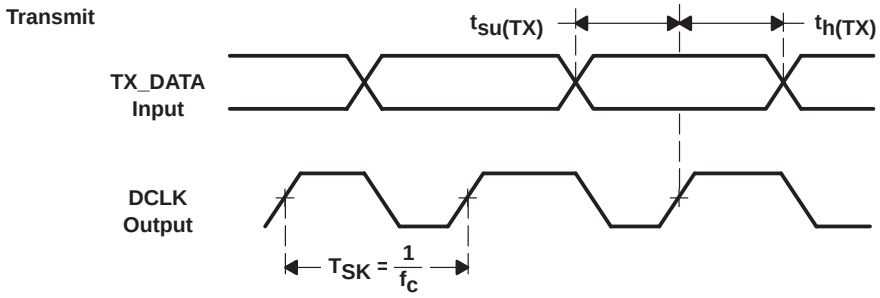


Note: Most significant bit (MSB) clocked in first to the synthesizer.

Figure 2. Timing Data for Serial Interface

timing data for DCLK and TX_DATA

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(TX)}$	Setup time, TX_DATA valid before DCLK ↑	100			ns
$t_{h(TX)}$	Hold time, TX_DATA valid after DCLK ↑	100			ns



NOTE: TX_DATA is latched at the rising edge of DCLK.

Figure 3. Timing Data for DCLK and TX_DATA

If transmit capture mode is selected (by setting bit 15 in word E), the data transitions (high-to-low or low-to-high) on the TXDATA pin is timed to coincide with the falling edge of DCLK. Any microcontroller using the TRF6903 can then latch TXDATA on the rising edge of DCLK. For more details, see the *data clock* section.

detailed description

bit synchronizer and data clock

When enabled, the integrated bit synchronizer and data clock circuitry provide as an output at terminal 16, DET_LD_DCLK, a data clock based on a programmable bit rate. The bit rate is programmable via variables D1, D2, and D3 and is always relative to the master clock (XTAL) frequency, F_X. Table 1 shows common bit rates (kbps) vs selected crystal frequencies (MHz) and the respective settings of D1, D2, and D3.

The preprogrammed bit rate can be calculated based on the following equation:

$$\text{Bit rate (kbps)} = \frac{\text{crystal frequency (kHz)}}{D1 \times D2 \times D3} = \frac{F_X}{D1 \times D2 \times D3} = f_C \text{ (kHz)}$$

where:

D1 = 1, 5, 6, or 8
D2 = 1, 2, 4, 8, 16, 32, 64, or 128
D3 = 15 or 16

The data clock circuit is designed to reset/clear internally with no user action required.

detailed description (continued)

Table 1. Common Bit Rates, Corresponding Crystal Frequencies, and Values of D1, D2, and D3

BIT RATE (kbps)	D1, D2, AND D3 MULTIPLIERS FOR COMMON CRYSTAL VALUES (CRYSTAL FREQUENCIES IN MHZ)					
	9.8304	12.288	14.7456	15.72864	16.384	19.6608
0.6	8x128x16					
0.9			8x128x16			
1		6x128x16			8x128x16	
1.024	5x128x15			8x128x15		
1.2	8x64x16	5x128x16	6x128x16			8x128x16
1.8			8x64x16			
2		6x64x16			8x64x16	
2.048	5x64x15			8x64x15		5x128x15
2.4	8x32x16	5x64x16	6x64x16			8x64x16
3.6			8x32x16			
4		6x32x16			8x32x16	
4.096	5x32x15			8x32x15		5x64x15
4.8	8x16x16	5x32x16	6x32x16			8x32x16
7.2			8x16x16			
8		6x16x16			8x16x16	
8.192	5x16x15			8x16x15		5x32x15
9.6	8x8x16	5x16x16	6x16x16			8x16x16
14.4			8x8x16			
16		6x8x16			8x8x16	
16.384	5x8x15			8x8x15		5x16x15
19.2	8x4x16	5x8x16	6x8x16			8x8x16
28.8			8x4x16			
32		6x4x16			8x4x16	
32.768	5x4x15			8x4x15		5x8x15
38.4	8x2x16	5x4x16	6x4 x16			8x4x16
57.6			8x2x16			
64		6x2x16			8x2x16	
65.536	5x2x15			8x2x15		5x4x15
76.8	8x1x16	5x2x16	6x2x16			8x2x16
115.2			8x1x16			
128		6x1x16			8x1x16	

main divider

The main divider is composed of a 5-bit A-counter and a 9-bit B-counter and a prescaler. The A-counter controls the divider ratio of the prescaler, which divides the VCO signal by either 33 or 32. The prescaler divides by 33 until the A-counter reaches its terminal count and then divides by 32 until the B-counter reaches terminal count, whereupon both counters reset and the cycle repeats. The total divide-by-N operation is related to the 32/33 prescaler by:

$N_{TOTAL} = 33 \times A + 32 \times (B - A)$

where $0 \le A \le 31$ and $31 \le B \le 511$ or, $N_{TOTAL} = A + 32B$

Thus, the N-divider has a range of $992 \le N_{TOTAL} \le 16383$

detailed description (continued)

PLL

The phase-locked loop is the radio frequency synthesizer for the TRF4903. It is used to generate the transmit signal and as the local oscillator for the receive mixer. The signal (F_X) from a reference crystal oscillator (XO) is divided by an integer factor R down to F_R. The minimum frequency resolution, and thus, the minimum channel spacing, is F_R.

$F_R = F_X \div R$ where $1 \le R \le 256$

The phase-locked loop is an integer-N design. The voltage-controlled oscillator (VCO) signal is divided by an integer factor N to get a frequency at the phase detector input.

$F_{PD} = F_{VCO} \div N$

The phase detector compares the divided VCO signal to the divided crystal frequency and implements an error signal from two charge pumps. The error signal corrects the VCO output to the desired frequency.

As is in any integer-N PLLs, the VCO output has spurs at integer multiples of the reference frequency (nF_R). In applications requiring contiguous frequency channels, the reference frequency is often chosen to be equal to the channel spacing, thus, channel spacing = $F_R = F_X \div R$. When enabled and when the PLL is locked, the DET_LD_DCLK terminal is high.

With the addition of an output divider for multiband operation, the actual output frequency, F_{out}, is given by:

$$F_{out} = \frac{F_{VCO}}{P} = \frac{F_X}{R} \times \frac{N}{P} = F_R \times \frac{N}{P} = \frac{A + 32B}{P} \times F_R$$

where $F_R = F_{PD}$ under locked conditions. The actual minimum channel spacing is:

$$\frac{F_R}{P} = \frac{F_X \div R}{P}$$

where P = 1, 2, 3 and is set by A<1:0>.

oscillator circuit and reference divider

The reference divider reduces the frequency of the external crystal (F_X) by an 8-bit programmable integer divisor, R, to an internal reference frequency (F_R) used for the phase-locked loop. The choice of internal reference frequency also has implications for lock time, maximum data rate, noise floor, and loop-filter design. The crystal frequency can be tuned using the F word to control internal trimming capacitors, which are placed in parallel with the crystal. These offset a small frequency error in the crystal. In an FSK application, an additional capacitor is placed in parallel (through terminal 19) with the external capacitor that is connected in series with the crystal, thus, changing the load capacitance as the transmit data switch (TX_DATA, terminal 1) is toggled. The change in load capacitance pulls the crystal off-frequency by the total frequency deviation.

Hence, the 2-FSK frequency, set by the level of TX_DATA and the external capacitor, can be represented as follows:

f_{out1} = TX_DATA Low (XTAL switch closed) f_{out2} = TX_DATA High (XTAL switch open)

Note that the frequencies f_{out1} and f_{out2} are centered about the frequency $f_{center} = (f_{out1} + f_{out2})/2$. When transmitting FSK, f_{center} is considered to be the effective carrier frequency and any receiver local oscillator (LO) should be set to the same f_{center} frequency ± the receiver's IF frequency (f_{IF}) for proper reception and demodulation.

oscillator circuit and reference divider (continued)

For the case of high-side injection, the receiver LO would be set to $f_{LO} = f_{center} + f_{IF}$. Using high-side injection, the received data would be inverted from the transmitted data applied at terminal 1, TX_DATA. Conversely, for low-side injection, the receiver LO would be set to $f_{LO} = f_{center} - f_{IF}$. Using low-side injection, the received data would be the same as the transmitted data.

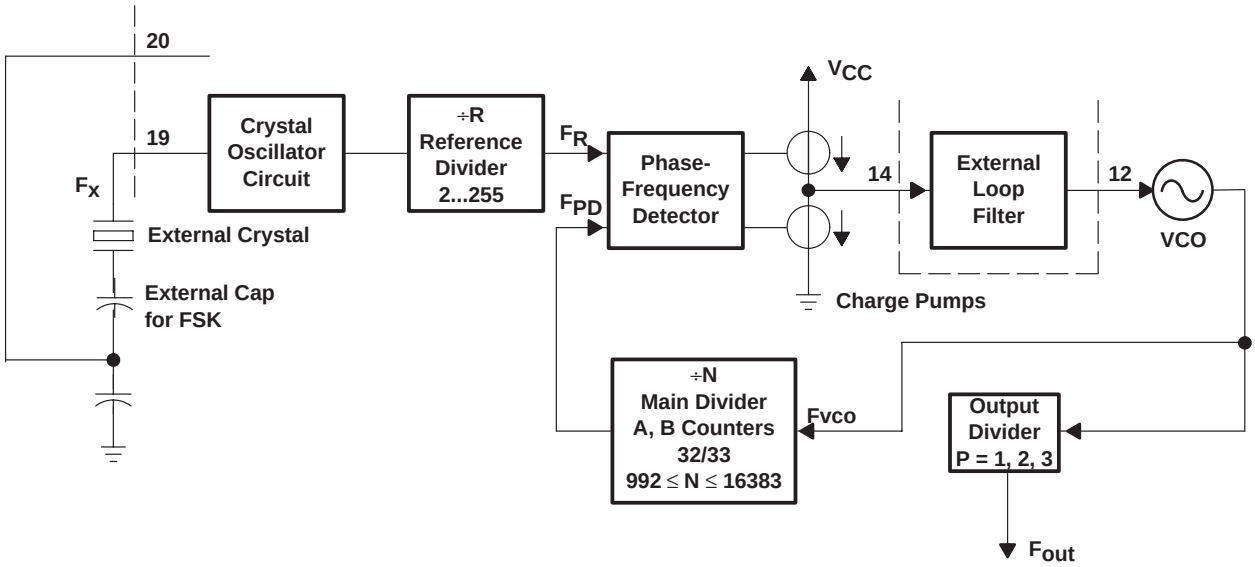


Figure 4. TRF4903 PLL and Output Divider

phase detector and charge pumps

The phase detector is a phase-frequency design. The phase-frequency detector gain is given by:

$$K_P = I_{(CP)}/2\pi$$

where, $I_{(CP)}$ is the peak charge pump current. The peak charge pump current is programmable with A<3:2> in three steps: 250 μA, 500 μA, and 1000 μA.

loop filter

The loop filter must be carefully chosen for proper operation of the TRF4903. The loop filter is typically a second- or third-order passive design, and in FSK operation should have a bandwidth wide enough to allow the PLL to relock quickly as the external crystal frequency is pulled off-center during modulation. The loop filter should also be wider than the data modulation rate. These requirements should be balanced with making the loop narrow enough in consideration of the reference frequency. In OOK the VCO frequency is not changed during data modulation, so the filter bandwidth may be narrower than the modulation bandwidth. Filters can be calculated using standard formulas in reference literature. Some third-order filter examples are shown in Table 2.

loop filter (continued)

$$F(s) = \frac{1 + sC2R2}{s(C1 + C2 + sC1C2R2)} \times \frac{\frac{1}{C3R3}}{s + \frac{1}{C3R3}}$$

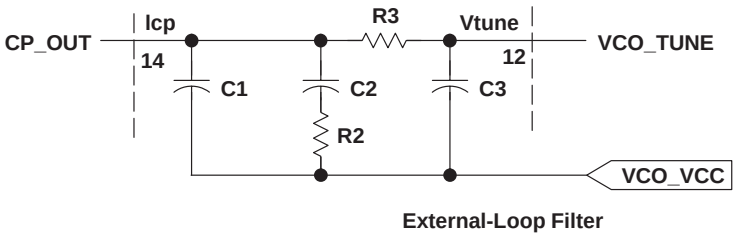


Figure 5. Third-Order Loop Filter and Transfer Function

Table 2. Loop Filter Component Values For Various Data Rates at a Reference Frequency of 409.6 kHz, 0.5-mA Charge Pump Current

Bit rate − kbps	Manchester coding	1.024	2.048	4.096	8.192	16.384	19.2	32.768	65.536
	NRZ coding	2.048	4.096	8.192	16.384	32.768	38.4	65.536	131.072
Data rate − kHz	Fundamental freq of BB	1.024	2.048	4.096	8.192	16.384	19.2	32.768	65.536
Loop filter component (selected to nearest standard value)	C1, nF	47	12	2.7	0.68	0.18	0.12	0.043	0.01
	C2, nF	1800	430	100	27	6.8	5.1	1.8	0.47
	C3, nF	27	6.8	1.5	0.39	0.1	0.075	0.027	0.0068
	R2, kΩ	0.39	0.75	1.5	3	5.7	6.8	12	24
	R3, kΩ	0.75	1.5	3	5.7	12	15	22	47
−3−dB bandwidth, kHz (approximate)		1.28	2.56	5.12	10.24	20.48	24	40.96	81.92

VCO

The voltage-controlled oscillator (VCO) produces an RF output signal with a frequency that is dependent upon the dc-tuning voltage at terminal 12. The tank circuit is passive and has integrated varactor diodes and inductors. The open-loop VCO gain is approximately 100 MHz/V.

A <1:0> is used to set the output divider ratio for operation within the 315-MHz, 433-MHz, 868-MHz, or 915-MHz bands.

When the $\overline{\text{STDBY}}$ terminal is high, the reference, PLL, VCO, and dividers are powered up. When $\overline{\text{STDBY}}$ is low, these blocks are powered down.

power amplifier

The power amplifier has three programmable attenuation states as determined by A<7:6> and B<7:6>: full power (0-dB attenuation), 10-dB attenuation, and 20-dB attenuation. This adjustment feature allows the user to fine-tune the device for optimal output power. The power amplifier can be enabled/disabled during transmit by bit B<3>, PAED. During ASK or OOK operation, the TX_DATA signal turns the output stage of the power amplifier on and off according to the transmit data incident at terminal 1.

power amplifier (continued)

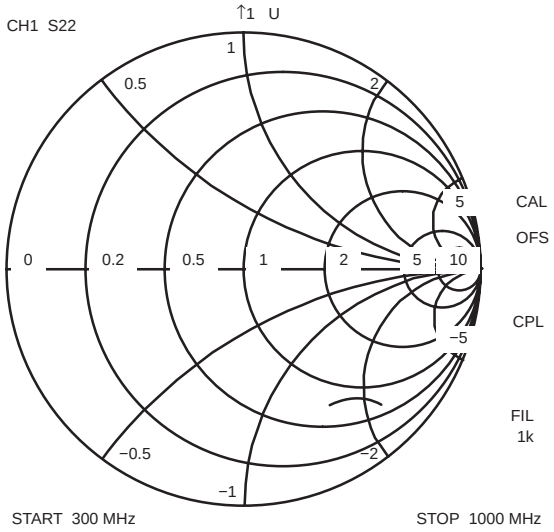


Figure 6. Typical PA Output Impedance (S22) at Device Terminal PA_OUT

brownout detector

The brownout detector provides an output voltage to indicate a low supply voltage. This may be used to signal the need to change transmit power to conserve battery life, or for system power down. The brownout detector threshold is set with the B word. Four different thresholds are available.

serial control interface

The TRF4903 is controlled through a serial interface; there are five 24-bit control words (A, B, C, D, E) which set the device state. The A and B words are almost identical, and provide configuration settings for two modes, designated 0 and 1, which are commonly used to configure the transmit states. Two transmit states can then be rapidly selected using MODE (terminal 2). The C word sets the reference dividers, the power amplifier bias, and contains various reset bits. The E word contains the bit-rate select, data clock control bits, and the power amplifier bias control registers. The D word is used to trim the external crystal frequency and tune the demodulator.

The register address is the composite of bits 23, 22, 1, and 0 of the 24 bits written to the serial interface. For some words, certain bits of the address are don't cares and are noted as XX. This flexible addressing scheme allows compatibility with the TRF6901/TRF6903 and because of this flexibility, the data length of each register varies from 15 bits to 22 bits.

Normal (write) operation of the serial interface is to clock in 24 bits through the CLOCK and DATA terminals. DATA values are clocked into the 24-bit serial interface shift register on the rising edge of CLOCK. The 24-bit value is decoded and written into the appropriate data register on the rising edge of STROBE.

PRINCIPLES OF OPERATION

register description

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	Address																						Address	
A	0	0	Main A-Divider Coefficient (Mode 0)					Main B-Divider Coefficient (Mode 0)									PA0		1	r	CP Acc.		BND	
B	0	1	Main A-Divider Coefficient (Mode 1)					Main B-Divider Coefficient (Mode 1)									PA1		1	FSK/ OOK	PAED	Detector Threshold		Det. Enable
C	1	0	Reference Divider Coefficient								Reserved							r	r	r	r	r	0	0
E	1	0	BRA			BRB		BRC	TXM	0	0	MUX		r	r	r	r	r	r	r	r	r	0	1
D	1	1	r	OOKXS	r	XTAL_Tune			PFD reset	1	1	r	r	r	r	r	r	r	r	r	r	r	r	0

NOTE: r = reserved. All reserved bits should be set low (0) during normal operation.

NOTE: All bits indicated as 1 should be set high (1) during normal operation.

NOTE: All bits indicated as 0 should be set low (0) during normal operation.

ADDRESS	LOCATION	NO. OF BITS	DESCRIPTION	DEFAULT VALUE
00xx	21:17	5	Main A divider coefficient (Mode 0)	00000
00xx	16:8	9	Main B divider coefficient (Mode 0)	001110000
00xx	7:6	2	Controls the PA attenuation (Mode 0)	10
00xx	5	1	Enables transmit path (Mode 0); set to 1	1
00xx	3:2	2	Controls charge pump peak current	00
00xx	1:0	2	Output divider coefficient; band select	10
01xx	21:17	5	Main A divider coefficient (Mode 1)	00000
01xx	16:8	9	Main B divider coefficient (Mode 1)	001110000
01xx	7:6	2	Controls the PA attenuation (Mode 1)	10
01xx	5	1	Enables transmit path (Mode 1); set to 1	1
01xx	4	1	Controls modulation scheme (FSK or OOK)	0
01xx	3	1	Enables or disables the power amplifier	0
01xx	2:1	2	Sets threshold for the brownout detector	00
01xx	0	1	Enables brownout detector	0
1000	21:14	8	Reference divider coefficient	01000000
1001	21:20	2	Bit-rate divider D1	11
1001	19:17	3	Bit-rate divider D2	010
1001	16	1	Bit-rate divider D3	0
1001	15	1	Transmit capture mode select	0
1001	12:11	2	Determines the function of terminal 16, DET_LD_DCLK	00
11x0	20	1	Controls the position of the XTAL switch during OOK operation	0
11x0	18:16	3	Tunes the XTAL frequency by using an internal capacitor bank	000
11x0	15	1	PFD reset	1

NOTE: x = don't care

PRINCIPLES OF OPERATION

At power on/startup, all of the TRF4903 register contents are as per the default values.

Address 00XX (A-Word)

Word A is a 22-bit data register comprising five fields. The main A-divider coefficient (mode 0), A<21:17>, is the 5-bit divider ratio of the A counter when the MODE terminal is low. The main B-divider coefficient (mode 0), A<16:8>, is the 9-bit value of the B counter when the MODE terminal is low. A <21:17> and A <16:8> are unsigned binary values. PA0, A<7:6>, is the 2-bit PA attenuation setting when the MODE terminal is low. CP Acc., A<3:2>, sets the charge pump current. BND, A<1:0>, sets the output divider, which in turn determines the band of operation.

Terminal 2 (MODE) selects bits A<21:5> if low, or B<21:5> if high.

Main divider A<21:17>: 5-bit value for divider ratio of the A counter
Main divider A<16:8>: 9-bit value for divider ratio of the B counter

PA attenuation A<7:6>: 2 bits for setting the PA attenuation

A<7:6>	PA ATTENUATION
00	0 dB
01	10 dB
10	20 dB
11	Not defined

A<5>: 1-bit; set high

A<3:2>: 2 bits for setting the charge pump current

A<3:2>	CP CURRENT
00	0.5 mA
01	1 mA
10	0.25 mA
11	Not defined

A<1:0>: 2-bit value to set the output divider and thus select the band of operation.

A<1:0>	OUTPUT DIVIDER RATIO, P	BAND OF OPERATION
00	3	315 MHz
01	2	433 MHz
10	1	868 MHz or 915 MHz
11	1	868 MHz or 915 MHz

Bit A<4> is reserved and should be set to 0.

Address 01XX (B-Word)

Word B is a 22-bit data register comprising seven fields. The main A-divider coefficient (mode 1), B<21:17>, is the 5-bit divider ratio of the A counter when the MODE terminal is high. The main B-divider coefficient (mode 1), B<16:8>, is the 9-bit value of the B counter when the MODE terminal is high. B<21:17> and B<16:8> are unsigned binary values. PA1, B<7:6>, is the 2-bit PA attenuation setting when the MODE terminal is high. FSK/OOK, B<4>, sets the modulation scheme for TX. Bit B<3> enables/disables the power amplifier while in transmit mode. The detector threshold, B<2:1>, is the 2-bit setting for the threshold voltage of the brownout detector. Det. Enable, B<0>, is the brownout detector enable flag.

Terminal 21 (MODE) selects bits A<21:5> if low, or B<21:5> if high.

Main divider B<21:17>: 5-bit value for divider ratio of the A-counter
Main divider B<16:8>: 9-bit value for divider ratio of the B-counter

PA attenuation B<7:6>: 2 bits for setting the PA attenuation

B<7:6>	PA ATTENUATION
00	0 dB
01	10 dB
10	20 dB
11	Not defined

B<5>: 1-bit; set high

B<4> 1-bit modulation select

B<4>	TX MODULATION
0	OOK
1	FSK

B<3>: 1-bit PA enable/disable

B<3>	PA ENABLE/DISABLE
0	PA disabled
1	PA enabled

B<2:1>: 2-bit value to set the threshold voltage for the brownout detector

B<2:1>	THRESHOLD VOLTAGE
00	2.2 V
01	2.4 V
10	2.6 V
11	2.8 V

B<0>: 1 bit to enable brownout detector

B<0>	BROWNOUT DETECTOR
0	Off
1	On

PRINCIPLES OF OPERATION

Address 1000 (C-Word)

Word C is a 20-bit data register comprising four fields. The reference divider coefficient, C<21:14>, is the 8-bit divider ratio of the reference divider. The allowable reference divider range is 2 (C <21:14> = 00000010) through 255 (C <21:14> = 11111111).

Reference divider C <21:14>: 8-bit value for divider ratio of reference divider. C<21:14> is an unsigned binary value.

Bits C<13> through C<2> are reserved and should be set to 0.

PRINCIPLES OF OPERATION

Address 1001 (E-Word)

Word E is a 20-bit data register comprising five fields. The bit rate or bit frequency, used by the transmit synchronous mode is controlled by the BRA, E<21:20>, BRB, E<19:17>, and BRC, E<16>, fields. These three fields control a sequence of dividers, D1 through D3, that divide the reference (crystal) frequency, F_X.

E<21:20>: 2 bits to set D1 divider setting

E<21:20>	D1
00	1
01	5
10	6
11	8

E<19:17>: 3 bits to set D2 divider setting

E<19:17>	D2
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

E<16>: 1 bit to set D3 divider setting

E<16>	D3
0	16
1	15

TXM, E<15>, sets the transmit capture mode. If TXM is low, the TX_DATA terminal controls the transmit function asynchronously. If TXM is high and the bit-rate clock enabled, the bit-rate clock, DCLK, is output at the DET_LD_DCLK terminal and the transmit data at the TX_DATA terminal is latched on the rising edge of DCLK.

E<12:11>: 2 bits to determine the function of terminal 16

E<12:11>	TERMINAL 16, DET_LD_DCLK, FUNCTION
00	PLL lock detect output (default)
01	Data clock output
10	Brownout detect output
11	Not used

Bits E<14>, E<13> and E<10> through E<2> are reserved and should be set to 0.

PRINCIPLES OF OPERATION

Address 11X0 (D-Word)

Word D is a 21-bit data register comprising two fields. Bit D<20> controls the position of the XTAL switch during OOK operation. XTAL_Tune, D<18:16>, is used to fine tune the crystal frequency by using an internal capacitor bank. PFD reset, D<15>, selects the source of the PFD reset signal.

D<20>: 1-bit value to control the position of the XTAL switch during OOK operation, when B<4>=0.

D<20>	XTAL SWITCH DURING OOK OPERATION	TERMINAL 20
0	Unconnected (open)	High-Z
1	Connected (closed)	Shorted to ground externally

It is recommended that D<20> be set to 0 during OOK operation.

D<18:16>: 3-bit value to fine-tune the XTAL frequency by using an internal capacitor bank

D<18:16>	TYPICAL LOAD CAPACITANCE
000	13.23 pF
001	22.57 pF
010	17.9 pF
011	27.24 pF
100	15.56 pF
101	24.9 pF
110	20.23 pF
111	29.57 pF

D<15>: 1-bit value to select the reset signal for the PFD

D<15>	RESET SIGNAL
0	Derived from XTAL
1	Derived from prescaler

NOTE: The default setting for D<15> is 1.

Bits D<21>, D<19>, and D<12> through D<1> are reserved and should be set to 0.

operating modes

Controlled with terminal 3, $\overline{\text{STDBY}}$

$\overline{\text{STDBY}}$	OPERATING MODE
0	Power down of all blocks—programming mode
1	Operational mode and programming mode

Controlled with terminal 2, MODE

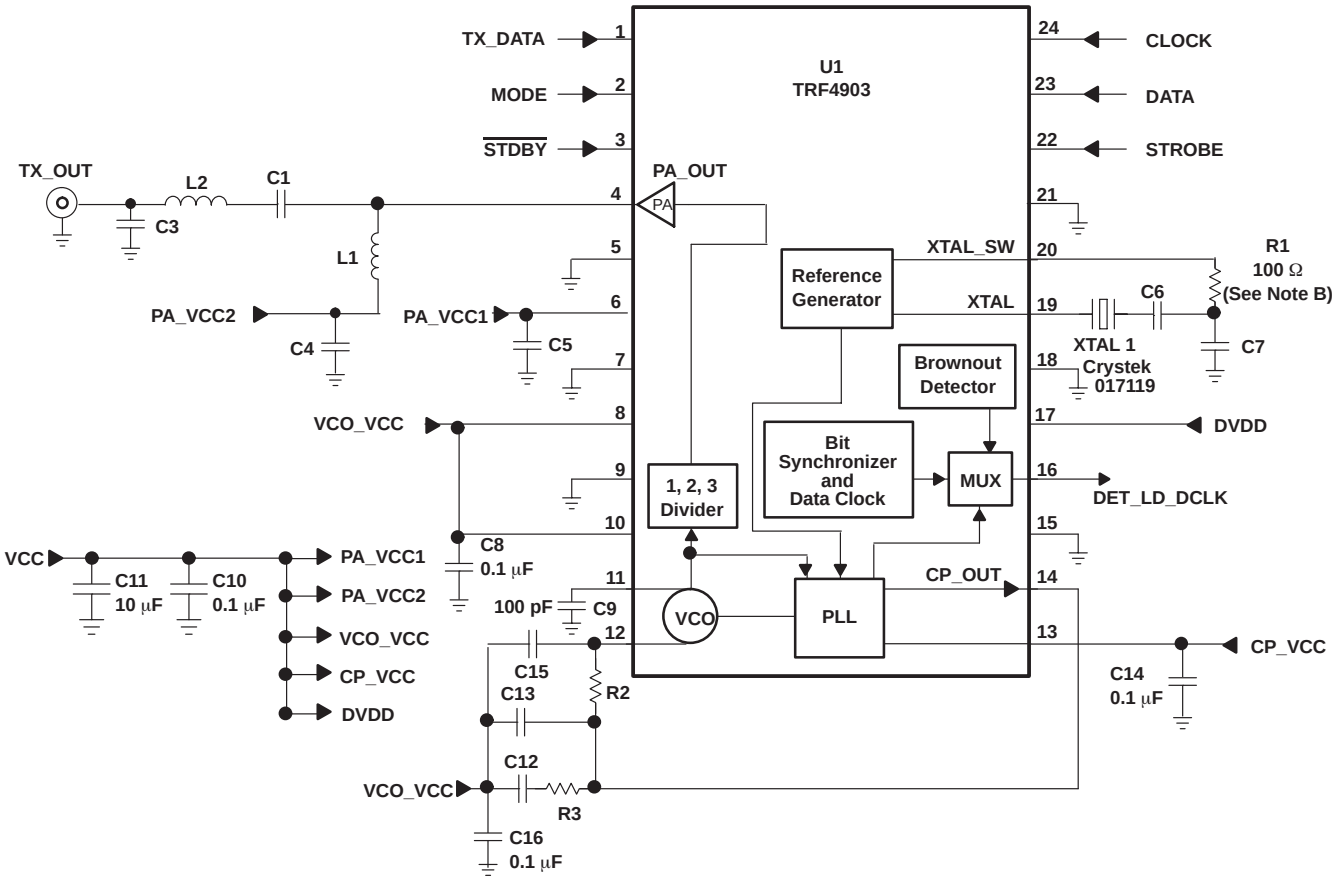
MODE	OPERATING MODE
0	Enable A-word
1	Enable B-word

operating modes (continued)

The transmit mode is controlled by the A<5>, B<5>, and B<3> fields and the MODE and $\overline{\text{STDBY}}$ terminals.

A<5>	B<5>	B<3>	MODE	$\overline{\text{STDBY}}$	OPERATING MODE
X	X	X	X	0	Off, programming mode; SPI enabled
1	X	0	0	1	Transmit mode 0, PA disabled; reference, PLL, VCO, and dividers enabled
1	X	1	0	1	Transmit mode 0, PA enabled; reference, PLL, VCO, and dividers enabled
X	1	0	1	1	Transmit mode 1, PA disabled; reference, PLL, VCO, and dividers enabled
X	1	1	1	1	Transmit mode 1, PA enabled; reference, PLL, VCO, and dividers enabled

APPLICATION INFORMATION

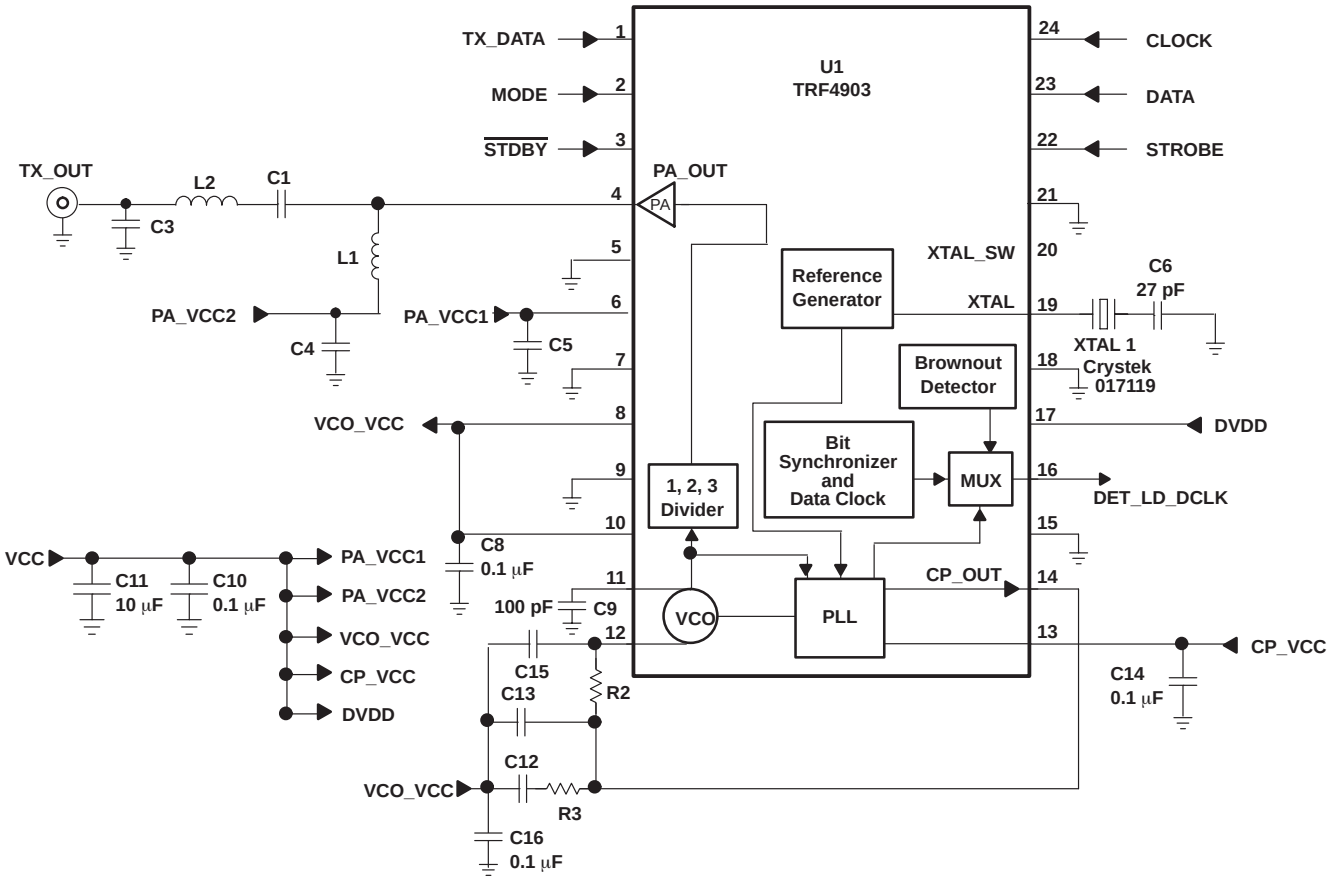


	Component Selection for Band of Operation							
	315 MHz		433 MHz		868 MHz		915 MHz	
	Component	Value	Component	Value	Component	Value	Component	Value
TX PA Matching Network	C1	390 pF	C1	270 pF	C1	43 pF	C1	43 pF
	C3	5.1 pF	C3	4.7 pF	C3	1.5 pF	C3	1.5 pF
	C4	390 pF	C4	270 pF	C4	39 pF	C4	33 pF
	C5	390 pF	C5	270 pF	C5	39 pF	C5	33 pF
	L1	560 nH	L1	470 nH	L1	330 nH	L1	270 nH
	L2	75 nH	L2	43 nH	L2	18 nH	L2	15 nH
PLL Loop Filter	C12	5600 pF	C12	5600 pF	C12	5600 pF	C12	5600 pF
	C13	120 pF	C13	120 pF	C13	120 pF	C13	120 pF
	C15	75 pF	C15	75 pF	C15	75 pF	C15	75 pF
	R2	15 kΩ	R2	15 kΩ	R2	15 kΩ	R2	15 kΩ
	R3	7.5 kΩ	R3	7.5 kΩ	R3	7.5 kΩ	R3	7.5 kΩ
XTAL Switch Capacitors	C6	27 pF	C6	27 pF	C6	27 pF	C6	27 pF
	C7	5.6 pF	C7	9.1 pF	C7	20 pF	C7	22 pF

Figure 7. Typical TRF4903 FSK Application Schematic

NOTES: A. Loop filter components selected for 19.2-kbps Manchester or 38.4-kbps NRZ for each band. I_{CP} = 0.5 mA, Reference Frequency = 409.6 kHz
B. R1 = 100 Ω is optional for operation in the 868-MHz and 915-MHz bands.
C. XTAL switch capacitors selected for the frequency deviation of ±50 kHz.

APPLICATION INFORMATION



	Component Selection for Band of Operation							
	315 MHz		433 MHz		868 MHz		915 MHz	
	Component	Value	Component	Value	Component	Value	Component	Value
TX PA Matching Network	C1	390 pF	C1	270 pF	C1	43 pF	C1	43 pF
	C3	5.1 pF	C3	4.7 pF	C3	1.5 pF	C3	1.5 pF
	C4	390 pF	C4	270 pF	C4	39 pF	C4	33 pF
	C5	390 pF	C5	270 pF	C5	39 pF	C5	33 pF
	L1	560 nH	L1	470 nH	L1	330 nH	L1	270 nH
	L2	75 nH	L2	43 nH	L2	18 nH	L2	15 nH
PLL Loop Filter	C12	5600 pF	C12	5600 pF	C12	5600 pF	C12	5600 pF
	C13	120 pF	C13	120 pF	C13	120 pF	C13	120 pF
	C15	75 pF	C15	75 pF	C15	75 pF	C15	75 pF
	R2	15 kΩ	R2	15 kΩ	R2	15 kΩ	R2	15 kΩ
	R3	7.5 kΩ	R3	7.5 kΩ	R3	7.5 kΩ	R3	7.5 kΩ

Figure 8. Typical TRF4903 OOK Application Schematic

NOTE: Loop filter components selected for 19.2 kbps Manchester or 38.4 kbps NRZ for each band. I_{CP} = 0.5 mA, Reference Frequency = 409.6 kHz

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TRF4903PW	NRND	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85	TRF4903	
TRF4903PWG4	NRND	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
TRF4903PWR	NRND	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85	TRF4903	
TRF4903PWRG4	NRND	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

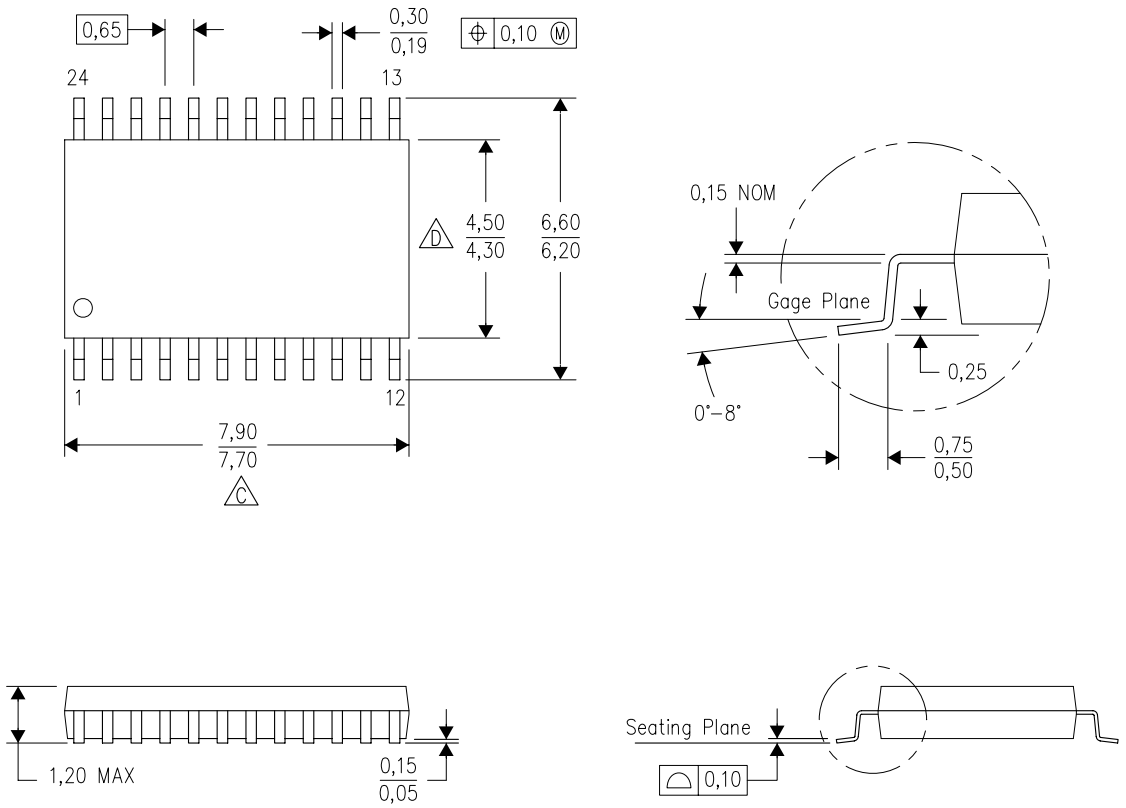
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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