life.augmented

# LSM6DSV

Datasheet

## iNEMO inertial module: always-on 3-axis accelerometer and 3-axis gyroscope




**LGA-14L**
**(2.5 x 3.0 x 0.83 mm) typ.**

| Product status link |
|---|
| LSM6DSV |

| Product summary | | |
|---|---|---|
| **Order code** | LSM6DSV | LSM6DSVTR |
| **Temperature range [°C]** | -40 to +85 | |
| **Package** | LGA-14L (2.5 x 3.0 x 0.83 mm) | |
| **Packing** | Tray | Tape and reel |

| Product resources |
|---|
| TN0018 (Design and soldering) |

| Product label |
|---|
| SUSTAINABLE TECHNOLOGY |

## Features

- Triple core for UI, EIS, and OIS data processing
- Power consumption: 0.65 mA in combo high-performance mode
- “Always-on" experience with low power consumption for both accelerometer and gyroscope
- Smart FIFO up to 4.5 KB
- Android compliant
- ±2/±4/±8/±16 *g* full scale
- ±125/±250/±500/±1000/±2000/±4000 dps full scale
- Analog supply voltage: 1.71 V to 3.6 V
- Independent IO supply (extended range: 1.08 V to 3.6 V)
- Compact footprint: 2.5 mm x 3 mm x 0.83 mm
- SPI / I²C & MIPI I3C® v1.1 serial interface with main processor data synchronization
- Auxiliary SPI for OIS data output for gyroscope and accelerometer
- OIS configurable from aux SPI, primary interface (SPI / I²C & MIPI I3C® v1.1)
- EIS dedicated channel on primary interface with dedicated filtering
- Advanced pedometer, step detector and step counter
- Significant motion detection, tilt detection
- Standard interrupts: free-fall, wake-up, 6D/4D orientation, click and double-click
- Programmable finite state machine for accelerometer, gyroscope and external sensor data processing with high rate @ 960 Hz
- Embedded temperature sensor
- ECOPACK and RoHS compliant

## Applications

- Motion tracking and gesture detection, augmented reality (AR) / virtual reality (VR) / mixed reality (MR) applications
- Wearables
- Indoor navigation
- IoT and connected devices
- Smartphones and handheld devices
- EIS and OIS for camera applications
- Vibration monitoring and compensation

## Description

The LSM6DSV is a system-in-package featuring a 3-axis digital accelerometer and a 3-axis digital gyroscope with a triple core for processing acceleration and angular rate data on three separate channels with dedicated configuration, processing, and filtering.

The LSM6DSV boosts performance at 0.65 mA in high-performance mode and enables always-on low-power features for an optimal motion experience for the consumer. The device embeds advanced dedicated features such as a finite state machine as well as data filtering for OIS, EIS, and motion processing.

# 1 Overview

The LSM6DSV is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

The LSM6DSV delivers best-in-class motion sensing that can detect orientation and gestures in order to empower application developers and consumers with features and capabilities that are more sophisticated than simply orienting their devices to portrait and landscape mode.

The event-detection interrupts enable efficient and reliable motion tracking and contextual awareness, implementing hardware recognition of free-fall events, 6D orientation, click and double-click sensing, activity or inactivity, stationary/motion detection and wake-up events. Finite state machine processing allows moving some algorithms from the application processor to the LSM6DSV sensor, enabling consistent reduction of power consumption.

The LSM6DSV supports main OS requirements, offering real, virtual, and batch mode sensors. In addition, the LSM6DSV can efficiently run the sensor-related features specified in Android, saving power and enabling faster reaction time. In particular, the LSM6DSV has been designed to implement hardware features such as significant motion detection, stationary/motion detection, tilt, pedometer functions, timestamping and to support the data acquisition of external sensors.

The LSM6DSV offers hardware flexibility to connect the pins with different mode connections to external sensors to expand functionalities such as adding a sensor hub, auxiliary SPI, and so forth.

The LSM6DSV offers advanced design flexibility for OIS and EIS applications. Both channels have a dedicated processing path with independent filtering and enhanced EIS channel gyroscope data are read over the primary interfaces I²C/ MIPI I3C® v1.1 / SPI.

Core 1 has been designed for user-interface data processing for motion tracking. Data are available on the primary output of I²C / SPI / I3C® for the accelerometer and gyroscope with independent ODR and FS.

Core 2 has been designed for OIS applications. Data are available on the aux SPI at 7.68 kHz with accelerometer/gyroscope processing with independent FS at ±2 *g* - ±16 *g* (accelerometer) / ±125 dps - ±2000 dps (gyroscope). The accelerometer is also available as standalone with dedicated filtering.

Core 3 has been design for enhanced EIS. Data are available in freerun mode in the output registers or in FIFO with dedicated tag and timestamp.

Up to 4.5 KB of FIFO with compression and dynamic allocation of significant data (that is, external sensors, timestamp, and so forth) allows overall power saving of the system.

Like the entire portfolio of MEMS sensor modules, the LSM6DSV leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit, which is trimmed to better match the characteristics of the sensing element.

The LSM6DSV embeds advanced dedicated features like a finite state machine and data filtering for OIS, EIS, and motion processing.

The LSM6DSV is available in a small plastic land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultra-compact solutions.

# 2 Embedded low-power features

The LSM6DSV has been designed to be fully compliant with Android, featuring the following on-chip functions:

- 4.5 KB FIFO data buffering, data can be compressed two or three times
  - 100% efficiency with flexible configurations and partitioning
  - Possibility to store timestamp
- Event-detection interrupts (fully configurable)
  - Free-fall
  - Wake-up
  - 6D orientation
  - Click and double-click sensing
  - Activity/inactivity recognition
  - Stationary/motion detection
- Specific IP blocks (called "embedded functions") with negligible power consumption and high performance
  - Pedometer functions: step detector and step counters
  - Tilt
  - Significant motion detection
  - Finite state machine (FSM)
- Sensor hub
  - Up to 6 total sensors: 2 internal (accelerometer and gyroscope) and 4 external sensors

## 2.1 Pedometer functions: step detector and step counters

The LSM6DSV embeds an advanced pedometer with an algorithm running in an ultra-low-power domain in order to ensure extensive battery life in battery-constrained applications.

Leveraging on enhanced configurability, the advanced embedded pedometer is suitable for a large range of applications from mobile to wearable devices.

The algorithm processes and analyzes the accelerometer waveform in order to count the user's steps during walking and running activities.

The pedometer works at 30 Hz and it is not affected by the selected device power mode (ultra-low-power, low-power, high-performance), thus guaranteeing an ultra-low-power experience and extreme flexibility in conjunction with other device functionalities.

The accelerometer operating mode can be changed at runtime and is based on user requirements without impacting the performance of the pedometer.

The pedometer output can be batched in the device's FIFO buffer, in order to decrease overall system current consumption.

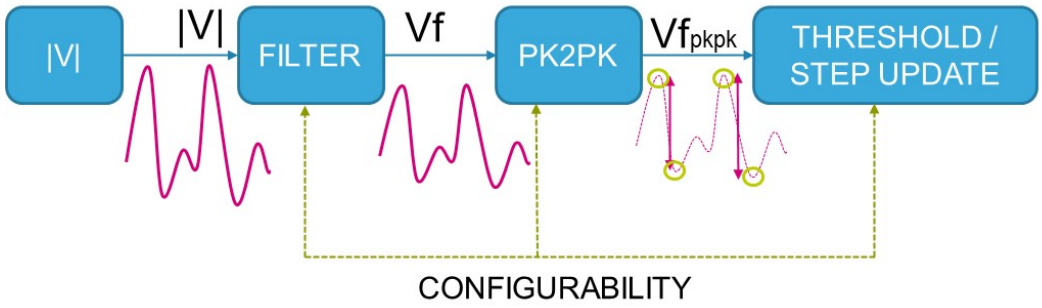
ST freely provides the support and the tools for easily configuring the device and tuning the algorithm configuration for a best-in-class user experience.

## 2.2 Pedometer algorithm

The pedometer algorithm is composed of a cascade of four stages:

1. Computation of the acceleration magnitude signal in order to detect the signal independently from device orientation;
2. FIR filter to extract relevant frequency components and to smooth the signal by cutting off high frequencies;
3. Peak detector to find the maximum and minimum of the waveform and compute the peak-to-peak value;
4. Step count: if the peak-to-peak value is greater than the settled threshold, a step is counted.

**Figure 1. Four-stage pedometer algorithm**




The LSM6DSV embeds a dynamic internal threshold for step detection that is updated after each peak-to-peak evaluation: the internal threshold is increased with a configurable speed if a step is detected or decreased with a configurable speed if a step is not detected.

This approach ensures high accuracy when the user starts to walk and a false peak rejection when the user is walking or running.

An internal configurable debounce algorithm can be also set to filter false walks: indeed, an accelerometer pattern is recognized as a walk or run only if a minimum number of steps are counted.

The LSM6DSV has been designed to reject a false-positive signal inside the algorithm core.

On top of the mechanisms detailed above, the LSM6DSV allows enabling and configuring a dedicated false-positive rejection block to further boost pedometer accuracy.

## 2.3 Tilt detection

The tilt function helps to detect activity change and has been implemented in hardware using only the accelerometer to achieve targets of both ultra-low power consumption and robustness during the short duration of dynamic accelerations.

The tilt function is based on a trigger of an event each time the device's tilt changes and can be used with different scenarios, for example:

- Triggers when phone is in a front pants pocket and the user goes from sitting to standing or standing to sitting;
- Doesn’t trigger when phone is in a front pants pocket and the user is walking, running or going upstairs.

## 2.4 Significant motion detection

The significant motion detection (SMD) function generates an interrupt when a ‘significant motion’, that could be due to a change in user location, is detected. In the LSM6DSV device this function has been implemented in hardware using only the accelerometer.

SMD functionality can be used in location-based applications in order to receive a notification indicating when the user is changing location.

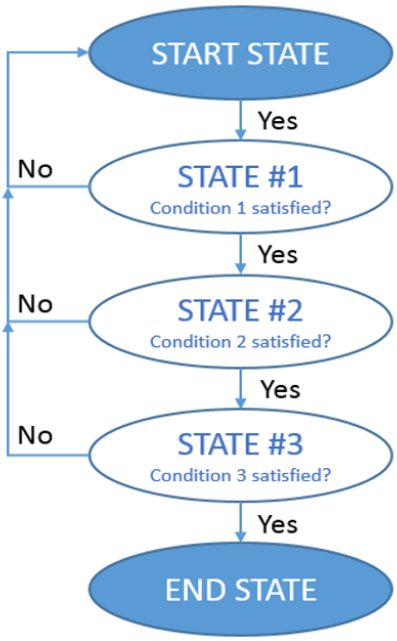
## 2.5 Finite state machine

The LSM6DSV can be configured to generate interrupt signals activated by user-defined motion patterns. To do this, up to 8 embedded finite state machines can be programmed independently for motion detection such as glance gestures, absolute wrist tilt, shake and double-shake detection.

### Definition of finite state machine

A state machine is a mathematical abstraction used to design logic connections. It is a behavioral model composed of a finite number of states and transitions between states, similar to a flow chart in which one can inspect the way logic runs when certain conditions are met. The state machine begins with a start state, goes to different states through transitions dependent on the inputs, and can finally end in a specific state (called stop state). The current state is determined by the past states of the system. The following figure shows a generic state machine.

**Figure 2. Generic state machine**




### Finite state machine in the LSM6DSV

The LSM6DSV works as a combo accelerometer-gyroscope sensor, generating acceleration and angular rate output data. It is also possible to connect an external sensor like a magnetometer or pressure sensor by using the sensor hub feature (mode 2). These data can be used as input of up to 8 programs in the embedded finite state machine (Figure 3. State machine in the LSM6DSV).

All 8 finite state machines are independent: each one has its dedicated memory area and it is independently executed. An interrupt is generated when the end state is reached or when some specific command is performed.

**Figure 3. State machine in the LSM6DSV**

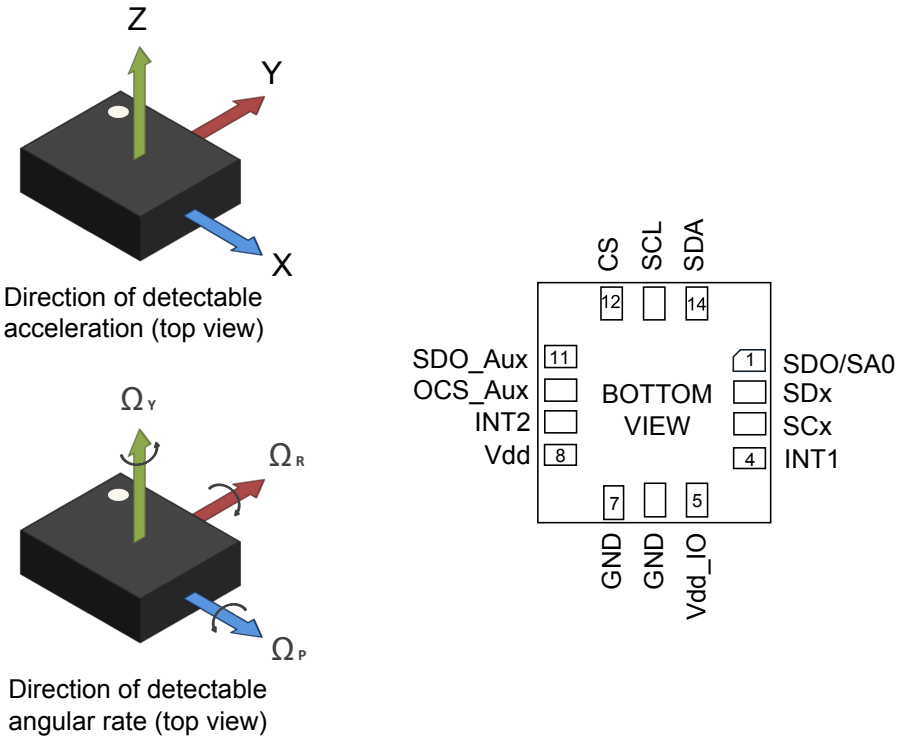


## 2.6 Adaptive self-configuration (ASC)

The LSM6DSV supports the adaptive self-configuration (ASC) feature, which allows the FSM to automatically reconfigure the device in real time based on the detection of a specific motion pattern, without any intervention from the host processor. The FSM can write a subset of the device registers using the SETR command, which allows indicating the register address and the new value to be written in such a register. The access to these device registers is mutually exclusive to the host.

# 3 Pin description

**Figure 4. Pin connections**

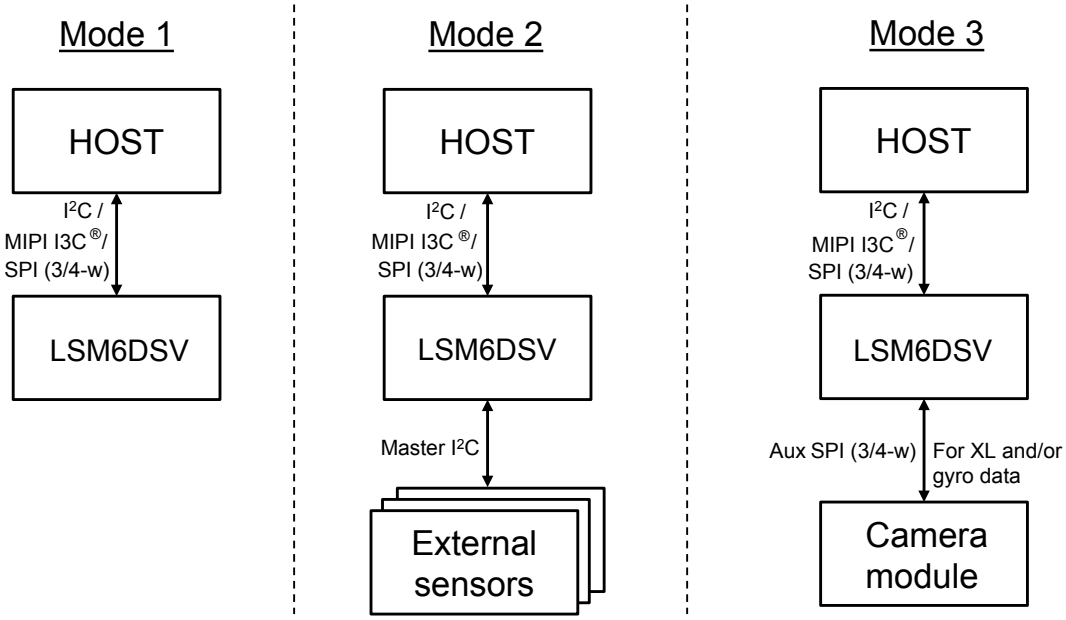


## 3.1 Pin connections

The LSM6DSV offers flexibility to connect the pins in order to have three different mode connections and functionalities. In detail:

- **Mode 1**: I²C / MIPI I3C® slave interface or SPI (3- and 4-wire) serial interface is available.
- **Mode 2**: I²C / MIPI I3C® slave interface or SPI (3- and 4-wire) serial interface and I²C interface master for external sensor connections are available.
- **Mode 3:** I²C / MIPI I3C® slave interface or SPI (3- and 4-wire) serial interface is available for the application processor interface while an auxiliary SPI (3- and 4-wire) serial interface for external sensor connections is available for the accelerometer and gyroscope.

**Figure 5. LSM6DSV connection modes**



In the following table each mode is described for the pin connections and function.

**Table 1. Pin description**

| Pin# | Name | Mode 1 function | Mode 2 function | Mode 3 function |
|---|---|---|---|---|
| 1 | SDO/SA0 | SPI 4-wire interface serial data output (SDO)<br>I²C least significant bit of the device address (SA0) | SPI 4-wire interface serial data output (SDO)<br>I²C least significant bit of the device address (SA0) | SPI 4-wire interface serial data output (SDO)<br>I²C least significant bit of the device address (SA0) |
| 2 | SDx | Connect to Vdd_IO or GND | I²C serial data master (MSDA) | Auxiliary SPI 3/4-wire interface serial data input (SDI)<br>and SPI 3-wire serial data output (SDO) |
| 3 | SCx | Connect to Vdd_IO or GND | I²C serial clock master (MSCL) | Auxiliary SPI 3/4-wire interface serial port clock (SPC_Aux) |
| 4 | INT1 | Programmable interrupt in I²C and SPI | | |
| 5 | Vdd_IO(1) | Power supply for I/O pins | | |
| 6 | GND | 0 V supply | | |
| 7 | GND | 0 V supply | | |
| 8 | Vdd(1) | Power supply | | |
| 9 | INT2 | Programmable interrupt 2<br>(INT2) / Data enable (DEN) | Programmable interrupt 2 (INT2) / Data enable (DEN) /<br>I²C master external synchronization signal (MDRDY) | Programmable interrupt 2 (INT2) / Data enable (DEN) |
| 10 | OCS_Aux | Connect to Vdd_IO or leave unconnected(2) | Connect to Vdd_IO or leave unconnected(2) | Enable auxiliary SPI 3/4-wire interface |
| 11 | SDO_Aux | Connect to Vdd_IO or leave unconnected(2) | Connect to Vdd_IO or leave unconnected(2) | Auxiliary SPI 3-wire interface: leave unconnected(2)<br>Auxiliary SPI 4-wire interface: serial data output (SDO_Aux) |
| 12 | CS | I²C / MIPI I3C® / SPI mode selection<br>(1: SPI idle mode / I²C / MIPI I3C® communication enabled;<br>0: SPI communication mode / I²C / MIPI I3C® disabled) | I²C / MIPI I3C® / SPI mode selection<br>(1: SPI idle mode / I²C / MIPI I3C® communication enabled;<br>0: SPI communication mode / I²C / MIPI I3C® disabled) | I²C / MIPI I3C® / SPI mode selection<br>(1: SPI idle mode / I²C / MIPI I3C® communication enabled;<br>0: SPI communication mode / I²C / MIPI I3C® disabled) |
| 13 | SCL | I²C / MIPI I3C® serial clock (SCL)<br>SPI serial port clock (SPC) | I²C / MIPI I3C® serial clock (SCL)<br>SPI serial port clock (SPC) | I²C / MIPI I3C® serial clock (SCL)<br>SPI serial port clock (SPC) |
| 14 | SDA | I²C / MIPI I3C® serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) | I²C / MIPI I3C® serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) | I²C / MIPI I3C® serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |

1. *Recommended 100 nF filter capacitor.*
2. *Leave pin electrically unconnected and soldered to PCB.*

# 4 Module specifications

## 4.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25 °C, unless otherwise noted.

**Table 2. Mechanical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| LA_FS | Linear acceleration measurement range | | | ±2 | | *g* |
| | | | | ±4 | | |
| | | | | ±8 | | |
| | | | | ±16 | | |
| G_FS | Angular rate measurement range | | | ±125 | | dps |
| | | | | ±250 | | |
| | | | | ±500 | | |
| | | | | ±1000 | | |
| | | | | ±2000 | | |
| | | | | ±4000 | | |
| LA_So | Linear acceleration sensitivity(2) | FS = ±2 *g* | | 0.061 | | mg/LSB |
| | | FS = ±4 *g* | | 0.122 | | |
| | | FS = ±8 *g* | | 0.244 | | |
| | | FS = ±16 *g* | | 0.488 | | |
| G_So | Angular rate sensitivity(2) | FS = ±125 dps | | 4.375 | | mdps/LSB |
| | | FS = ±250 dps | | 8.75 | | |
| | | FS = ±500 dps | | 17.50 | | |
| | | FS = ±1000 dps | | 35 | | |
| | | FS = ±2000 dps | | 70 | | |
| | | FS = ±4000 dps | | 140 | | |
| G_So% | Sensitivity tolerance(3) | at component level | | ±0.3 | | % |
| LA_SoDr | Linear acceleration sensitivity change vs. temperature(4) | from -40° to +85° | | ±0.01 | | %/°C |
| G_SoDr | Angular rate sensitivity change vs. temperature(4) | from -40° to +85° | | ±0.007 | | %/°C |
| LA_TyOff | Linear acceleration zero-*g* level offset accuracy(3) | | | ±12 | | mg |
| G_TyOff | Angular rate zero-rate level(3) | | | ±1 | | dps |
| LA_OffDr | Linear acceleration zero-*g* level change vs. temperature(4) | | | ±0.07 | | mg/°C |
| G_OffDr | Angular rate typical zero-rate level change vs. temperature(4) | | | ±0.006 | | dps/°C |
| Rn | Rate noise density in high-performance mode(5) | | | 2.8 | | mdps/√Hz |
| RnRMS | Gyroscope RMS noise in low-power mode(6) | | | 60 | | mdps RMS |
| An | Acceleration noise density in high-performance mode(7) | FS = ±2 *g* - ±16 *g* | | 60 | | µg/√Hz |
| | Acceleration noise density in normal mode(8)(9) | FS = ±2 *g* - ±16 *g* | | 100 | | |
| RMS | Accelerometer RMS noise in low-power mode | LPM1 | | 2.3 | | mg RMS |
| | | LPM2 | | 1.8 | | |
| | | LPM3 | | 1.2 | | |

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| LA_ODR | Linear acceleration output data rate | | | 1.875(10)<br>7.5<br>15<br>30<br>60<br>120<br>240<br>480<br>960<br>1.92 k<br>3.84 k<br>7.68 k | | Hz |
| G_ODR | Angular rate output data rate | | | 7.5<br>15<br>30<br>60<br>120<br>240<br>480<br>960<br>1.92 k<br>3.84 k<br>7.68 k | | |
| HAODR | ODR variation over temperature and supply range in high-accuracy mode(11) | Gyro on | | | ±1 | % |
| | | Gyro off | | | ±3 | |
| Vst | Linear acceleration self-test output change(12)(13)(14) | | 50 | | 1700 | mg |
| | Angular rate self-test output change(15)(16) | FS = ±250 dps | 20 | | 80 | dps |
| | | FS = ±2000 dps | 150 | | 700 | dps |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. *Typical specifications are not guaranteed.*
2. *Sensitivity values after factory calibration test and trimming.*
3. *Value after calibration.*
4. *Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples. Not measured during final test for production.*
5. *Gyroscope rate noise density in high-performance mode is independent of the ODR and FS setting.*
6. *Gyroscope RMS noise in low-power mode is independent of the ODR and FS setting.*
7. *Accelerometer noise density in high-performance mode is independent of the selected ODR and FS. Valid when XL_DualC_EN = 0 in register CTRL8 (17h) .*
8. *Accelerometer noise density in normal mode is independent of the ODR and FS setting. Valid when XL_DualC_EN = 0 in register CTRL8 (17h).*
9. *Noise RMS related to BW = ODR/2.*
10. *This ODR is available when the accelerometer is in low-power mode.*
11. *Values specified by design.*
12. *The sign of the linear acceleration self-test output change is defined by the ST_XL_[1:0] bits in a dedicated register for all axes.*
13. *The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 0.061 mg at ±2 g full scale.*
14. *Accelerometer self-test limits are full-scale independent.*

15. *The sign of the angular rate self-test output change is defined by the ST_G_[1:0] bits in a dedicated register for all axes.*
16. *The angular rate self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 70 mdps at ±2000 dps full scale.*

## 4.2 Electrical characteristics

@ Vdd = 1.8 V, T = 25 °C, unless otherwise noted.

**Table 3. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | | 1.71 | 1.8 | 3.6 | V |
| Vdd_IO | Power supply for I/O | | 1.08 | | 3.6 | V |
| IddHP | Gyroscope and accelerometer current consumption in high-performance mode | | | 0.65 | | mA |
| LA_IddHP | Accelerometer current consumption in high-performance mode | | | 190 | | µA |
| LA_IddNM | Accelerometer current consumption in normal mode | | | 100 | | µA |
| LA_IddLPM2 | Accelerometer current consumption in low-power mode (LPM2) | ODR = 60 Hz<br>ODR = 1.875 Hz | | 20<br>4.2 | | µA |
| LA_IddLPM1 | Accelerometer current consumption in low-power mode (LPM1) | ODR = 60 Hz<br>ODR = 1.875 Hz | | 17<br>4.0 | | µA |
| IddPD | Gyroscope and accelerometer current consumption during power-down | | | 2.6 | | µA |
| Ton | Turn-on time - gyroscope | | | 30 | | ms |
| $V_{IH}$ | Digital high-level input voltage | | 0.7 * Vdd_IO | | | V |
| $V_{IL}$ | Digital low-level input voltage | | | | 0.3 * Vdd_IO | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 4 mA(2) | Vdd_IO - 0.2 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA(2) | | | 0.2 | V |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. *Typical specifications are not guaranteed.*
2. *4 mA is the maximum driving capability, that is, the maximum DC current that can be sourced/sunk by the digital pin in order to guarantee the correct digital output voltage levels $V_{OH}$ and $V_{OL}$.*

## 4.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

**Table 4. Temperature sensor characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. (1) | Max. | Unit |
|---|---|---|---|---|---|---|
| TODR(2) | Temperature refresh rate | | | 60 | | Hz |
| Toff | Temperature offset(3) | | -15 | | +15 | °C |
| TSen | Temperature sensitivity | | | 256 | | LSB/°C |
| TST | Temperature stabilization time(4) | | | | 500 | µs |
| T_ADC_res | Temperature ADC resolution | | | 16 | | bit |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. *Typical specifications are not guaranteed*
2. *When the accelerometer is in low-power mode and the gyroscope part is turned off, the TODR value is equal to the accelerometer ODR.*
3. *The output of the temperature sensor is 0 LSB (typ.) at 25 °C.*
4. *Time from power ON to valid data based on characterization data.*

## 4.4 Communication interface characteristics

### 4.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top. @ Vdd_IO = 1.8 V, T = 25 °C unless otherwise noted.

**Table 5. SPI slave timing values**

| Symbol | Parameter | Value(1) | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $f_{c(SPC)}$ | SPI clock frequency | | | 10 | MHz |
| $t_{c(SPC)}$ | SPI clock period | 100 | | | ns |
| $t_{high(SPC)}$ | SPI clock high | 45 | | | |
| $t_{low(SPC)}$ | SPI clock low | 45 | | | |
| $t_{su(CS)}$ | CS setup time (mode 3) | 5 | | | |
| | CS setup time (mode 0) | 20 | | | |
| $t_{h(CS)}$ | CS hold time (mode 3) | 20 | | | |
| | CS hold time (mode 0) | 20 | | | |
| $t_{su(SI)}$ | SDI input setup time | 5 | | | |
| $t_{h(SI)}$ | SDI input hold time | 15 | | | |
| $t_{v(SO)}$ | SDO valid output time | | 15 | 25 | |
| $t_{dis(SO)}$ | SDO output disable time | | | 50 | |
| $C_{load}$ | Bus capacitance | | | 100 | pF |

1. *Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production*

**Figure 6. SPI slave timing in mode 0**

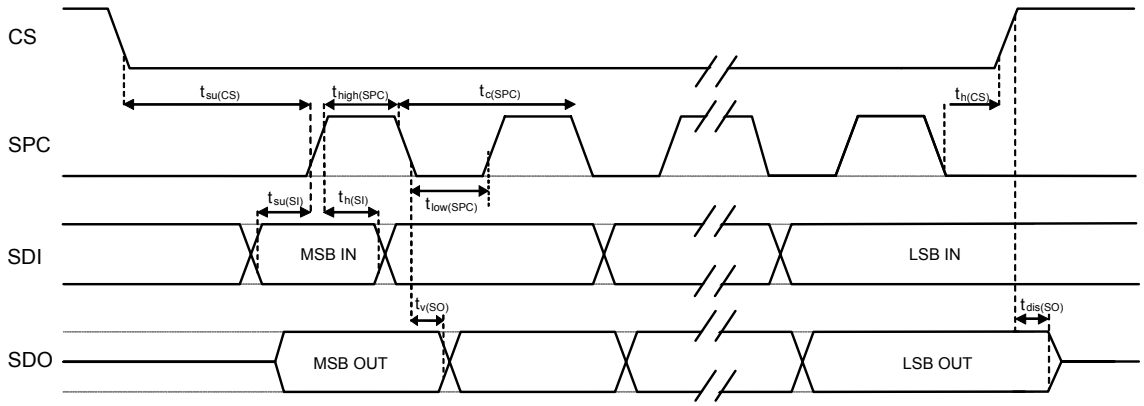
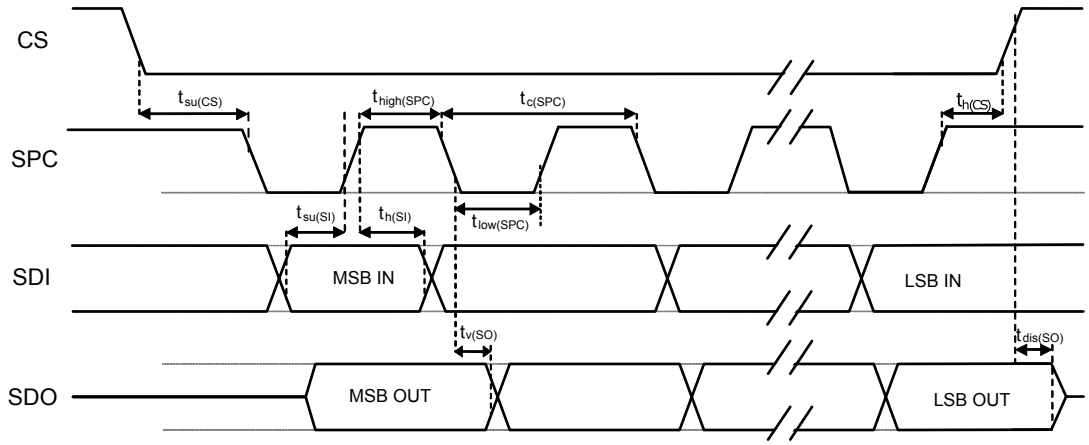


**Figure 7. SPI slave timing in mode 3**




*Note: Measurement points are done at 0.3·Vdd_IO and 0.7·Vdd_IO for both input and output ports.*

### 4.4.2 I²C - inter-IC control interface

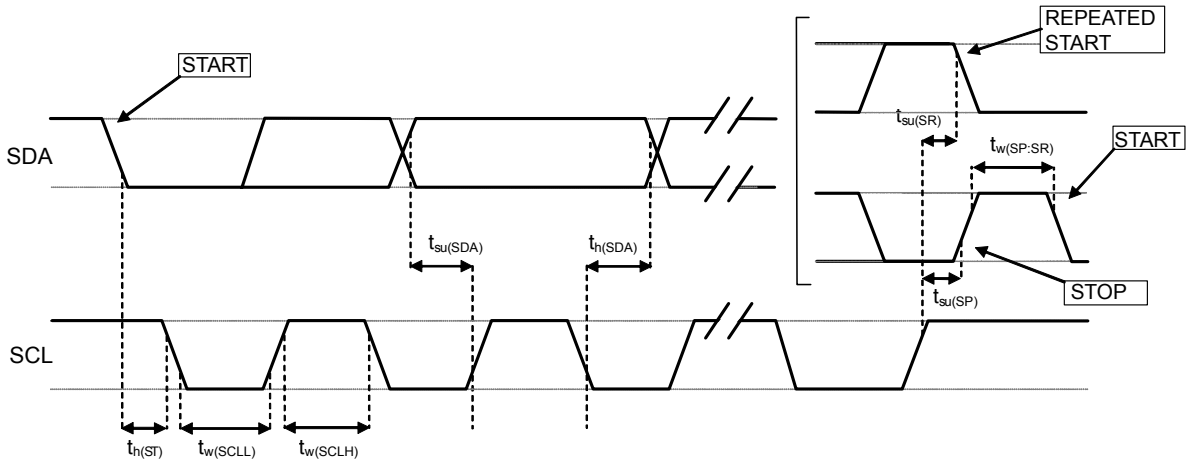
Subject to general operating conditions for Vdd and Top.

**Table 6. I²C slave timing values**

| Symbol | Parameter | I²C fast mode(1)(2) | | I²C fast mode +(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{(SCL)}$ | SCL clock frequency | 0 | 400 | 0 | 1000 | kHz |
| $t_{w(SCLL)}$ | SCL clock low time | 1.3 | | 0.5 | | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 0.6 | | 0.26 | | |
| $t_{su(SDA)}$ | SDA setup time | 100 | | 50 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | 0.9 | 0 | | µs |
| $t_{h(ST)}$ | START/REPEATED START condition hold time | 0.6 | | 0.26 | | |
| $t_{su(SR)}$ | REPEATED START condition setup time | 0.6 | | 0.26 | | |
| $t_{su(SP)}$ | STOP condition setup time | 0.6 | | 0.26 | | |
| $t_{w(SP:SR)}$ | Bus free time between STOP and START condition | 1.3 | | 0.5 | | |
| | Data valid time | | 0.9 | | 0.45 | |
| | Data valid acknowledge time | | 0.9 | | 0.45 | |
| $C_B$ | Capacitive load for each bus line | | 400 | | 550 | pF |

1. *Data based on standard I²C protocol requirement, not tested in production.*
2. *Data for I²C fast mode and I²C fast mode + have been validated by characterization, not tested in production.*

**Figure 8. I²C slave timing diagram**




*Note: Measurement points are done at 0.3·Vdd_IO and 0.7·Vdd_IO for both ports.*

## 4.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 7. Absolute maximum ratings**

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| Vdd | Supply voltage | -0.3 to 4.8 | V |
| $T_{STG}$ | Storage temperature range | -40 to +125 | °C |
| Sg | Acceleration *g* for 0.2 ms | 20,000 | *g* |
| ESD | Electrostatic discharge protection (HBM) | 2 | kV |
| Vin | Input voltage on any control pin<br>(including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0) | -0.3 to Vdd_IO +0.3 | V |

*Note: Supply voltage on any pin should never exceed 4.8 V.*



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 4.6 Terminology

### 4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see Table 2).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see Table 2).

### 4.6.2 Zero-*g* and zero-rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0 *g* on both the X-axis and Y-axis, whereas the Z-axis measures 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see “Linear acceleration zero-*g* level change vs. temperature” in Table 2. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see Table 2).

# 5 Digital interfaces

## 5.1 I²C/SPI interface

The registers embedded inside the LSM6DSV may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped to the same pins. To select/exploit the I²C interface, the CS line must be tied high (i.e connected to Vdd_IO).

**Table 8. Serial interface pin description**

| Pin name | Pin description |
|---|---|
| CS | Enables SPI<br>I²C/SPI mode selection<br>(1: SPI idle mode / I²C communication enabled;<br>0: SPI communication mode / I²C disabled) |
| SCL/SPC | I²C serial clock (SCL)<br>SPI serial port clock (SPC) |
| SDA/SDI/SDO | I²C serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| SDO/SA0 | SPI serial data output (SDO)<br>I²C less significant bit of the device address |

### 5.1.1 I²C serial interface

The LSM6DSV I²C is a bus slave. The I²C is employed to write the data to the registers, whose content can also be read back.

The relevant I²C terminology is provided in the table below.

**Table 9. I²C terminology**

| Term | Description |
|---|---|
| Transmitter | The device that sends data to the bus |
| Receiver | The device that receives data from the bus |
| Master | The device that initiates a transfer, generates clock signals, and terminates a transfer |
| Slave | The device addressed by the master |

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both the lines are high.

The I²C interface is implemented with fast mode (400 kHz) I²C standards as well as with fast mode plus (1000 kHz).

In order to disable the I²C block, I2C_I3C_disable = 1 must be written in IF_CFG (03h).

### 5.1.2 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LSM6DSV is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is 1 (address 1101011b); else if the SDO/SA0 pin is connected to ground, the LSb value is 0 (address 1101010b). This solution permits to connect and address two different inertial modules to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver that has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM6DSV behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit subaddress (SUB) is transmitted. The increment of the address is configured by the CTRL3 (12h) (IF_INC).

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the master transmits to the slave with direction unchanged. Table 10 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 10. SAD+read/write patterns**

| Command | SAD[6:1] | SAD[0] = SA0 | R/W | SAD+R/W |
|---|---|---|---|---|
| Read | 110101 | 0 | 1 | 11010101 (D5h) |
| Write | 110101 | 0 | 0 | 11010100 (D4h) |
| Read | 110101 | 1 | 1 | 11010111 (D7h) |
| Write | 110101 | 1 | 0 | 11010110 (D6h) |

**Table 11. Transfer when master is writing one byte to slave**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | |

**Table 12. Transfer when master is writing multiple bytes to slave**

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | DATA | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | | SAK | |

**Table 13. Transfer when master is receiving (reading) one byte of data from slave**

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | SR | SAD + R | | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | |

**Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave**

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD+ W | | SUB | | SR | SAD+ R | | | MAK | | MAK | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | DATA | | DATA | | |

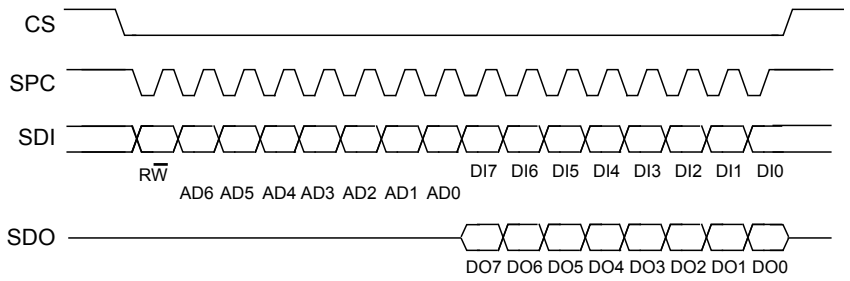
Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a slave receiver does not acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

In the presented communication format, MAK is master acknowledge and NMAK is no master acknowledge.

### 5.1.3 SPI bus interface

The SPI on the LSM6DSV is a bus slave which allows writing and reading the registers of the device.

**Figure 9. Read and write protocol (in mode 3)**




**CS** enables the serial port and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

**bit 0**: $\overline{RW}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip drives **SDO** at the start of bit 8.

**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

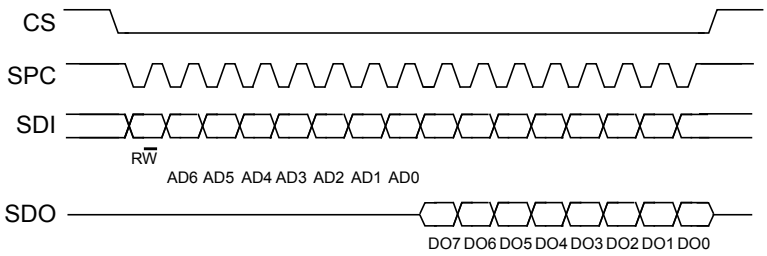
**bit 8-15**: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the CTRL3 (12h) (IF_INC) bit is 0, the address used to read/write data remains the same for every block. When the CTRL3 (12h) (IF_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

#### 5.1.3.1 SPI read

Figure 10. **SPI read protocol (in mode 3)**




The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

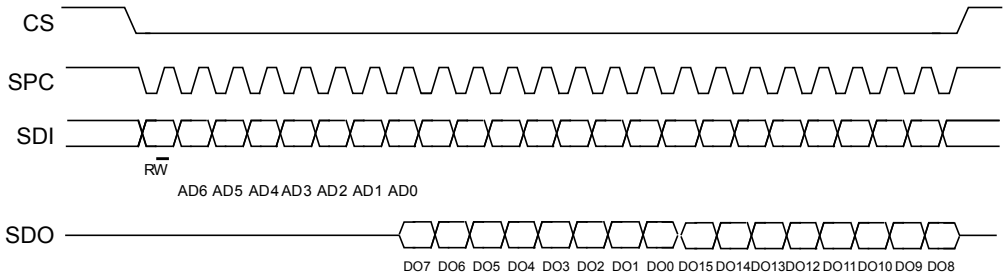
**bit 0**: READ bit. The value is 1.

**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

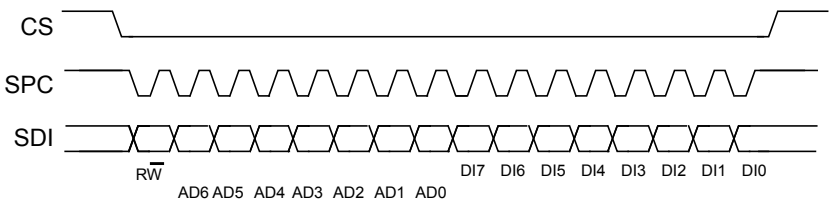
**bit 16-...**: data DO(...-8). Further data in multiple byte reads.

Figure 11. **Multiple byte SPI read protocol (2-byte example) (in mode 3)**



#### 5.1.3.2 SPI write

**Figure 12. SPI write protocol (in mode 3)**




The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

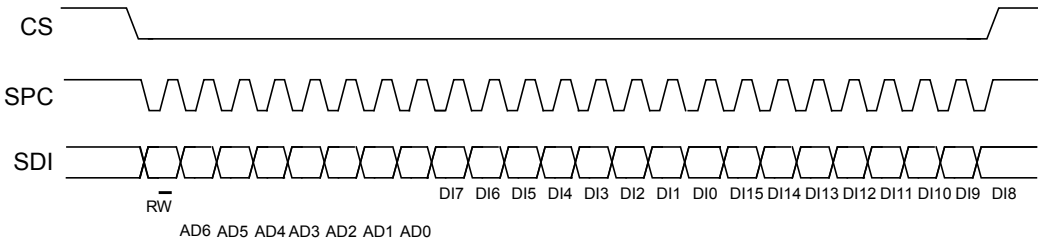
**bit 0**: WRITE bit. The value is 0.

**bit 1 -7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writes.

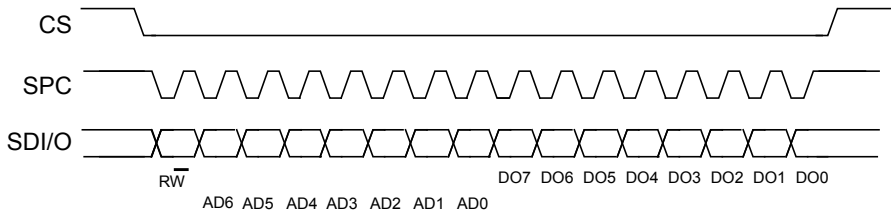
**Figure 13. Multiple byte SPI write protocol (2-byte example) (in mode 3)**




#### 5.1.3.3 SPI read in 3-wire mode

3-wire mode is entered by setting the IF_CFG (03h) (SIM) bit equal to 1 (SPI serial interface mode selection).

**Figure 14. SPI read protocol in 3-wire mode (in mode 3)**




The SPI read command is performed with 16 clock pulses:

**bit 0**: READ bit. The value is 1.

**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

## 5.2 MIPI I3C® interface

### 5.2.1 MIPI I3C® slave interface

The LSM6DSV interface includes an MIPI I3C® SDR only slave interface (compliant with release 1.1 of the specification) with MIPI I3C® SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- In-band interrupt request
- Slave reset pattern
- Group address
- Full range Vdd_IO support
- Asynchronous modes 0 and 1
- Synchronous mode
- Error detection and recovery methods (S0-S6)

In order to disable the MIPI I3C® block, I2C_I3C_disable = 1 must be written in IF_CFG (03h).

### 5.2.2 MIPI I3C® CCC supported commands

The list of MIPI I3C® CCC commands supported by the device is detailed in the following table.

**Table 15. MIPI I3C® CCC commands**

| Command | Command code | Default | Description |
|---|---|---|---|
| ENTDAA | 0x07 | | DAA procedure |
| SETDASA | 0x87 | | Assign dynamic address using static address 0x6B/0x6A depending on SDO pin |
| ENEC | 0x80 / 0x00 | | Slave activity control (direct and broadcast) |
| DISEC | 0x81/ 0x01 | | Slave activity control (direct and broadcast) |
| ENTAS0 | 0x82 / 0x02 | | Enter activity state (direct and broadcast) |
| SETXTIME | 0x98 / 0x28 | | Timing information exchange |
| GETXTIME | 0x99 | 0x07<br>0x00<br>0x05<br>0x92 | Timing information exchange |
| RSTDAA | 0x06 | | Reset the assigned dynamic address (broadcast only) |
| SETMWL | 0x89 / 0x08 | | Define maximum write length during private write (direct and broadcast) |
| SETMRL | 0x8A / 0x09 | | Define maximum read length during private read (direct and broadcast) |
| SETNEWDA | 0x88 | | Change dynamic address |
| GETMWL | 0x8B | 0x00<br>0x08<br>(2 byte) | Get maximum write length during private write |
| GETMRL | 0x8C | 0x00<br>0x10<br>0x09<br>(3 byte) | Get maximum read length during private read |
| GETPID | 0x8D | 0x02<br>0x08<br>0x00<br>0x70<br>0x92<br>0x0B | SDO = 1 |
| | | 0x02<br>0x08<br>0x00<br>0x70<br>0x12<br>0x0B | SDO = 0 |
| GETBCR | 0x8E | 0x07<br>(1 byte) | Bus characteristics register |
| GETDCR | 0x8F | 0x44 default | MIPI I3C® device characteristics register |
| GETSTATUS | 0x90 | 0x00<br>0x00<br>(2 byte) | Status register |
| GETMXDS | 0x94 | 0x08<br>0x60 | Return max write and read speed |

| Command | Command code | Default | Description |
|---|---|---|---|
| GETCAPS | 0x95 | 0x00<br>0x11<br>0x18<br>0x00 | Provide information about device capabilities and supported extended features |
| SETGRPA | 0x9B | | Group address assignment command |
| RSTGRPA | 0x2C / 0x9C | | Reset the group address |
| RSTACT | 0x9A / 0x2A | | Configure slave reset action |

### 5.2.3 Overview of anti-spike filter management

The device acts as a standard I²C target as long as it has an I²C static address. The device is capable of detecting and disabling the I²C anti-spike filter after detecting the broadcast address (7'h7E/W). In order to guarantee proper behavior of the device, the I3C master must emit the first START, 7'h7E/W at open-drain speed using I²C fast mode plus reference timing.

After detecting the broadcast address, the device can receive the I3C dynamic address following the I3C push-pull timing. If the device is not assigned a dynamic address, then the device continues to operate as an I²C device with no anti-spike filter. For the case in which the host decides to keep the device as I²C with anti-spike filter, there is a configuration required to keep the anti-spike filter active. This configuration is done by writing the ASF_CTRL bit to 1 in the IF_CFG (03h) register. This configuration forces the anti-spike filter to always be turned on instead of being managed by the communication on the bus.

## 5.3 Master I²C interface

If the LSM6DSV is configured in mode 2, a master I²C line is available. The master serial interface is mapped to the following dedicated pins.

**Table 16. Master I²C pin details**

| Pin name | Pin description |
|---|---|
| MSCL | I²C serial clock master |
| MSDA | I²C serial data master |
| MDRDY | I²C master external synchronization signal |

## 5.4 Auxiliary SPI interface

If the LSM6DSV is configured in mode 3, the auxiliary SPI is available. The auxiliary SPI interface is mapped to the following dedicated pins.

**Table 17. Auxiliary SPI pin details**

| Pin name | Pin description |
|---|---|
| OCS_Aux | Enables auxiliary SPI 3/4-wire |
| SDx | Auxiliary SPI 3/4-wire data input (SDI_Aux) and SPI 3-wire data output (SDO_Aux) |
| SCx | Auxiliary SPI 3/4-wire interface serial port clock |
| SDO_Aux | Auxiliary SPI 4-wire data output (SDO_Aux) |

When the LSM6DSV is configured in mode 3, the auxiliary SPI can be connected to a camera module for OIS support.

# 6 Functionality

## 6.1 Operating modes

In the LSM6DSV, the accelerometer and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

The LSM6DSV has three operating modes available:

- only accelerometer active and gyroscope in power-down
- only gyroscope active and accelerometer in power-down
- both accelerometer and gyroscope sensors active with independent ODR and power mode

The accelerometer is activated from power-down by writing ODR_XL_[3:0] in CTRL1 (10h) while the gyroscope is activated from power-down by writing ODR_G_[3:0] in CTRL2 (11h). For combo mode the ODRs are totally independent.

## 6.2 Accelerometer power modes

In the LSM6DSV, the accelerometer can be configured in five different operating modes: power-down mode, low-power mode (1, 2, 3), normal mode, high-performance mode and high-accuracy ODR mode.

The operating mode selected depends on the value of the OP_MODE_XL_[2:0] bits in CTRL1 (10h).

If the value of the OP_MODE_XL_[2:0] bits is 000 (default), high-performance mode is valid for all ODRs (from 7.5 Hz up to 7.68 kHz).

Normal mode is available for ODR values from 7.5 Hz to 1.92 kHz and it is enabled by setting the OP_MODE_XL_[2:0] bits to 111. Normal mode cannot be used in mode 3 connection mode.

In high-performance mode and in normal mode the analog anti-aliasing filter is active.

Low-power mode is available for lower ODRs (1.875 Hz, 15 Hz, 30 Hz, 60 Hz, 120 Hz, 240 Hz). The three low-power modes are enabled by setting OP_MODE_XL_[2:0] to 100 (LPM1), 101 (LPM2), 110 (LPM3).

High-accuracy ODR mode is available for ODR values from 15 Hz up to 7.68 kHz and it is enabled by setting the OP_MODE_XL_[2:0] bits to 001. Refer to Section 6.5 High-accuracy ODR mode for more details.

The embedded functions based on accelerometer data (free-fall, 6D/4D, tap/double-tap, wake-up, activity/inactivity, stationary/motion, step counter, step detection, significant motion, tilt) and the FIFO batching functionality are supported in all modes.

## 6.3 Accelerometer dual-channel mode

The LSM6DSV accelerometer block has a dual-channel architecture able to work with two different full scales simultaneously. By default, the device operates in single-channel mode supporting FS scale values from ±2 *g* through ±16 *g* and different power modes, as described in Section 6.2 Accelerometer power modes. The block diagrams in the following figures show the configuration of acceleration data processing in the two different modes.

**Figure 15. Single-channel mode (XL_DualC_EN = 0)**

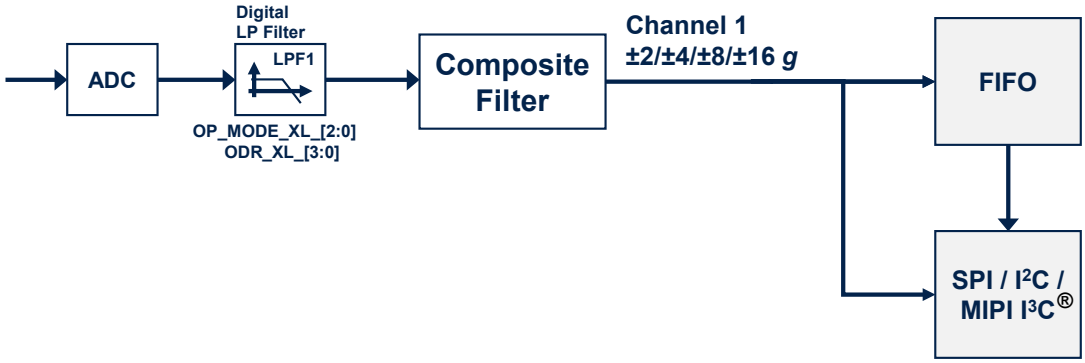
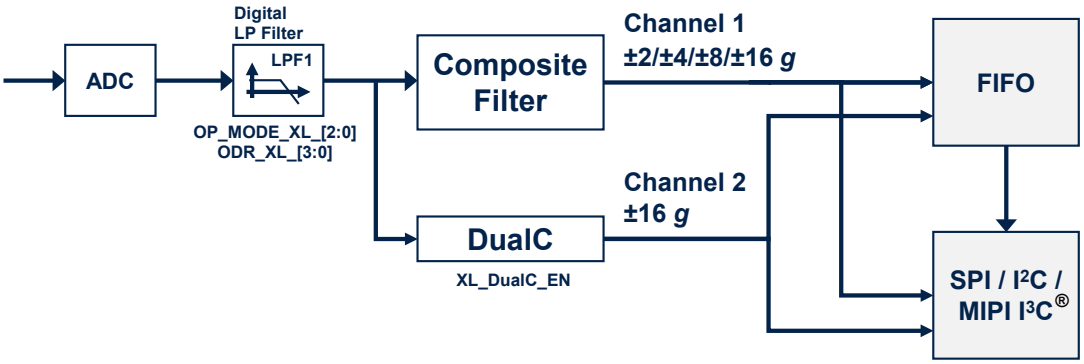



**Figure 16. Dual-channel mode (XL_DualC_EN = 1)**




The dual-channel functionality can be enabled/disabled by configuring the bit XL_DualC_EN to 1 (enable) or to 0 (disable) in CTRL8 (17h).

Referring to Figure 16. Dual-channel mode (XL_DualC_EN = 1), when the dual-channel mode has been activated:

1. Channel 1 supports user-selectable full-scale acceleration range of ±2/±4/±8/±16 *g* based on the value of the FS_XL_[1:0] bits in the CTRL8 (17h) register.
2. Channel 2 full scale is set to ±16 *g*. Acceleration data are available in the output registers from UI_OUTX_L_A_OIS_DualC (34h) and UI_OUTX_H_A_OIS_DualC (35h) through UI_OUTZ_L_A_OIS_DualC (38h) and UI_OUTZ_H_A_OIS_DualC (39h)).

## 6.4 Gyroscope power modes

In the LSM6DSV, the gyroscope can be configured in five different operating modes: power-down mode, sleep mode, low-power mode, high-performance mode and high-accuracy ODR mode.

The operating mode selected depends on the value of the OP_MODE_G_[2:0] bits in CTRL2 (11h).

If the value of the OP_MODE_G_[2:0] bits is 000 (default), high-performance mode is valid for all ODRs (from 7.5 Hz up to 7.68 kHz).

Low-power mode is available for lower ODRs (7.5 Hz, 15 Hz, 30 Hz, 60 Hz, 120 Hz, 240 Hz) and it is enabled by setting the the OP_MODE_G_[2:0] bits to 101.

High-accuracy ODR mode is available for ODR values from 15 Hz up to 7.68 kHz and it is enabled by setting the OP_MODE_G_[2:0] bits to 001. Refer to Section 6.5 High-accuracy ODR mode for more details.

## 6.5 High-accuracy ODR mode

High-accuracy ODR (HAODR) mode can be enabled to reduce the part-to-part output data rate variation. It supports accelerometer only, gyroscope only and combo (accelerometer and gyroscope) modes. When this mode is intended to be used for one sensor (accelerometer or gyroscope), the other sensor also has to be configured in high-accuracy ODR (HAODR) mode.

The main high-accuracy ODR features are:

- Noise level is aligned with high-performance mode
- Power consumption increase of 20 µA (typical) vs. the corresponding high-performance mode configuration selected
- As for high-performance mode, on-the-fly changes of the sensor output data rate, full scale and bandwidth are supported. The UI channel bandwidth can be selected through the gyroscope LPF1 and accelerometer HPF/LPF2 filters.
- When HAODR mode is enabled, it is applied to the UI accelerometer, UI gyroscope, EIS gyroscope, and temperature. It's not applied to OIS accelerometer/gyroscope channels.

*Note: HAODR mode has to be enabled / disabled when the device is in power-down mode.*

When HAODR mode is enabled, the set of the supported ODRs is aligned to nominal high-performance mode ODRs, as shown in the table below.

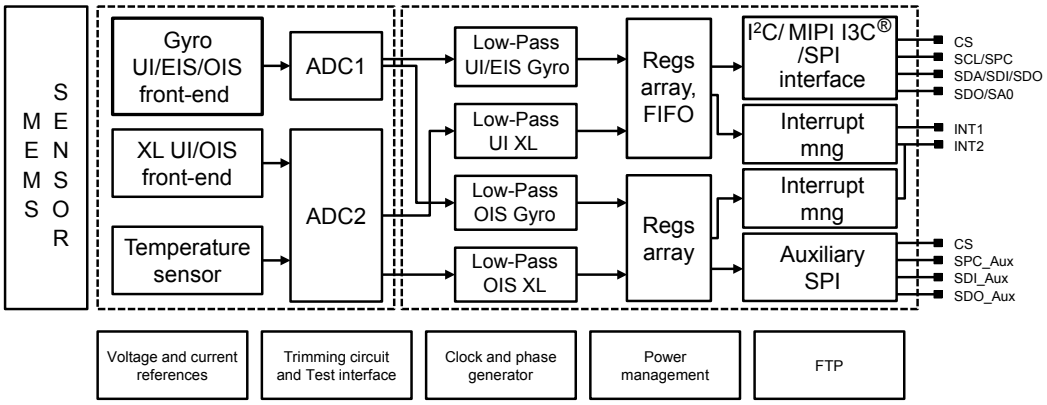
*Note: High-accuracy ODR mode is not compatible with the activity/inactivity functionality (motion/stationary can be used).*

**Table 18. Accelerometer and gyroscope ODR selection in high-accuracy ODR mode**

| ODR_XL_ [3:0]<br>ODR_G_[3:0] | ODR [Hz] |
|---|---|
| 0000 | Power-down |
| 0001 | Reserved |
| 0010 | Reserved |
| 0011 | 15 |
| 0100 | 30 |
| 0101 | 60 |
| 0110 | 120 |
| 0111 | 240 |
| 1000 | 480 |
| 1001 | 960 |
| 1010 | 1.92 kHz |
| 1011 | 3.84 kHz |
| 1100 | 7.68 kHz |
| Others | Reserved |

## 6.6 Block diagram of filters

Figure 17. **Block diagram of filters**



### 6.6.1 Block diagrams of the accelerometer filters

In the LSM6DSV, the filtering chain for the accelerometer part is composed of the following:

- Digital filter (LPF1)
- Composite filter

Details of the block diagram appear in the following figure.

**Figure 18. Accelerometer UI chain**

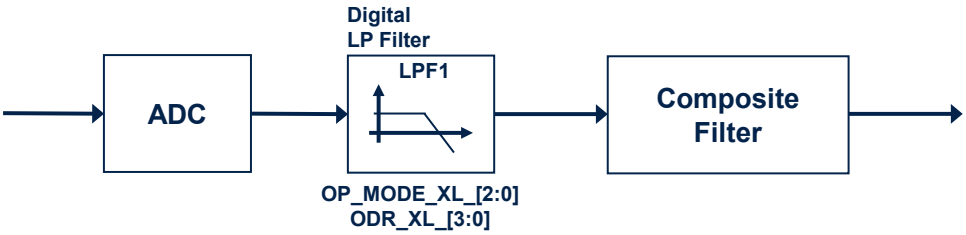
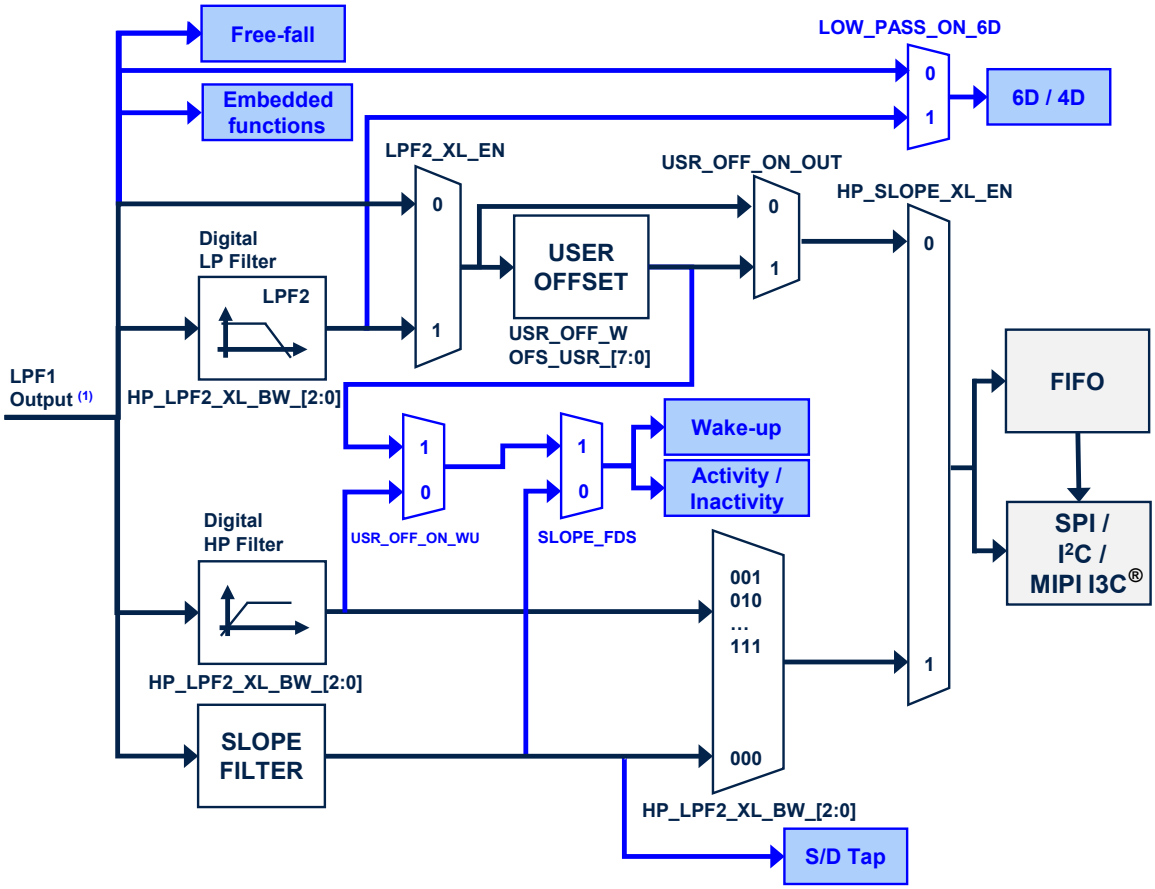



**Figure 19. Accelerometer composite filter**

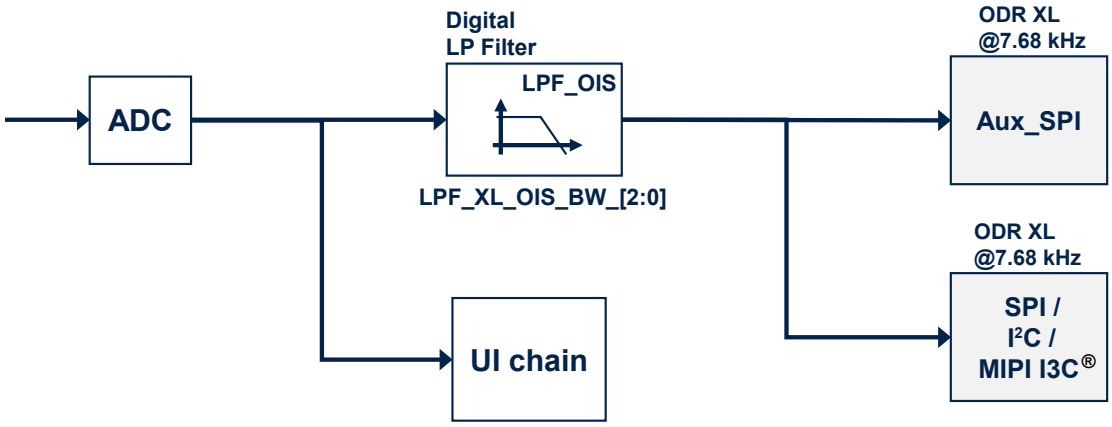



1. *The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode, high-accuracy ODR mode or normal mode. This value is equal to 2300 Hz when the accelerometer is in low-power mode 1 (2 mean), 912 Hz in low-power mode 2 (4 mean) or 431 Hz in low-power mode 3 (8 mean).*

*Note: Embedded functions include the finite state machine, pedometer, step detector and step counter, significant motion detection, and tilt functions.*

The accelerometer filtering chain when mode 3 is enabled is illustrated in the following figure.

**Figure 20. Accelerometer chain with mode 3 enabled**




*Note: The accelerometer OIS chain is enabled by setting the OIS_XL_EN bit to 1 in the UI_CTRL1_OIS (70h) / SPI2_CTRL1_OIS (70h) register.*

*The configuration of the accelerometer UI chain is not affected by enabling/disabling the accelerometer OIS chain, with one exception: accelerometer normal operating mode (OP_MODE_XL_[2:0] = 111 in the CTRL1 (10h) register) cannot be used when the accelerometer OIS chain is enabled.*

Accelerometer output values are available in the following registers with ODR at 7.68 kHz:

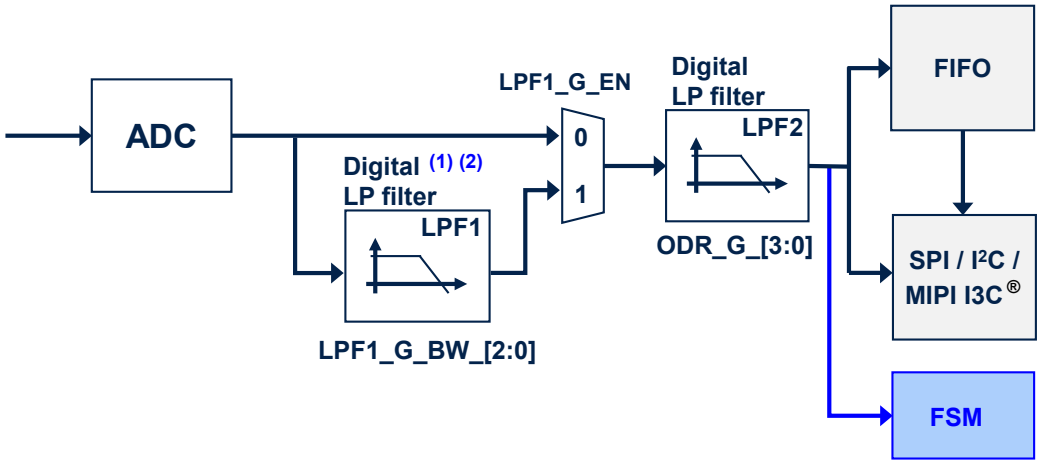
- UI_OUTX_L_A_OIS_DualC (34h) and UI_OUTX_H_A_OIS_DualC (35h) through UI_OUTZ_L_A_OIS_DualC (38h) and UI_OUTZ_H_A_OIS_DualC (39h)
- SPI2_OUTX_L_A_OIS (28h) and SPI2_OUTX_H_A_OIS (29h) through SPI2_OUTZ_L_A_OIS (2Ch) and SPI2_OUTZ_H_A_OIS (2Dh)

### 6.6.2 Block diagrams of the gyroscope filters

In the LSM6DSV, the gyroscope filtering chain depends on the mode configuration:

- Mode 1 (for user interface (UI) and electronic image stabilization (EIS) functionality through primary interface) and mode 2

**Figure 21. Gyroscope digital chain - mode 1 (UI/EIS) and mode 2**




1. *When the gyroscope OIS or EIS chain is enabled, the LPF1 filter is not available in the gyroscope UI chain. It is recommended to avoid using the LPF1 filter in the gyroscope UI chain when the gyroscope OIS or EIS is intended to be used.*
2. *The LPF1 filter is available in high-performance mode only. If the gyroscope is configured in low-power mode, the LPF1 filter is bypassed.*

In this configuration, the gyroscope ODR is selectable from 7.5 Hz up to 7.68 kHz. A low-pass filter (LPF1) is available, for more details about the filter characteristics see Table 60. Gyroscope LPF1 bandwidth selection.

The digital LPF2 filter's cutoff frequency depends on the selected gyroscope ODR, as indicated in the following table.

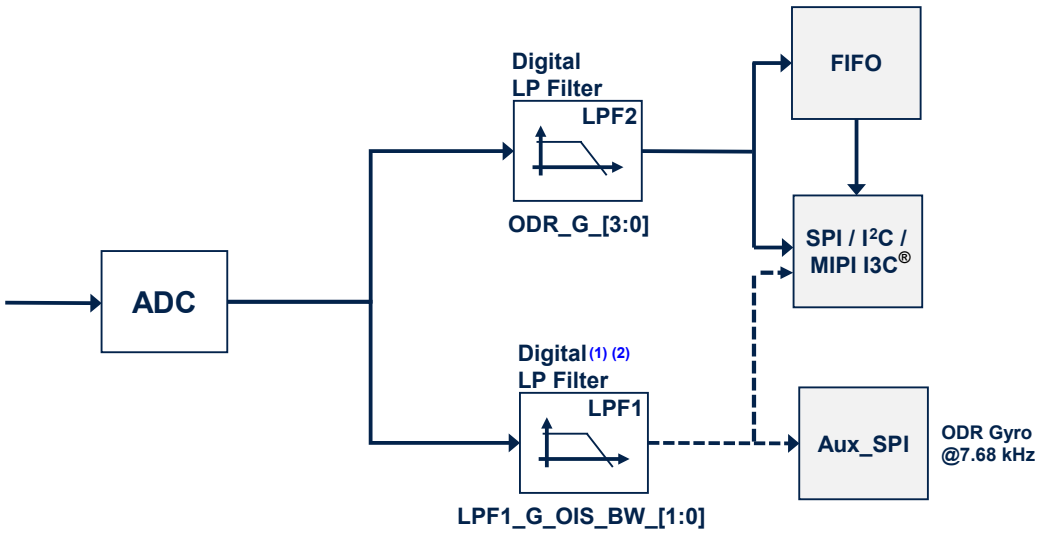
**Table 19. Gyroscope LPF2 bandwidth selection**

| Gyroscope ODR [Hz] | LPF2 cutoff [Hz] |
|---|---|
| 7.5 | 3.4 |
| 15 | 6.6 |
| 30 | 13.0 |
| 60 | 24.6 |
| 120 | 49 |
| 240 | 96 |
| 480 | 185 |
| 960 | 353 |
| 1.92 kHz | 491 |
| 3.84 kHz | 528 |
| 7.68 kHz | 537 |

*Note: Data can be acquired from the output registers and FIFO over the primary I²C/MIPI I3C®/SPI interface.*

- Mode 3 (for OIS functionality)

**Figure 22. Gyroscope digital chain - mode 3 (OIS)**




1. *When the gyroscope OIS or EIS chain is enabled, the LPF1 filter is not available in the gyroscope UI chain.*
2. *It is recommended to avoid using the LPF1 filter in mode1/2 when the gyroscope OIS or EIS chain is intended to be used.*

The auxiliary interface needs to be enabled in UI_CTRL1_OIS (70h) / SPI2_CTRL1_OIS (70h).

In mode 3 configuration, there are two paths:

- the chain for user interface (UI) where the ODR is selectable from 7.5 Hz up to 7.68 kHz
- the chain for OIS where the ODR is at 7.68 kHz and the LPF1 is available. The LPF1 configuration depends on the setting of the LPF1_G_OIS_BW_[1:0] bits in register UI_CTRL2_OIS (71h) / SPI2_CTRL2_OIS (71h); for more details about the filter characteristics see UI_CTRL2_OIS (71h). Gyroscope output values are in registers 22h to 27h if read from the Auxi_SPI or in registers 2Eh to 33h if read from the primary interface with the selected full scale FS_G_OIS_[1:0] bits in UI_CTRL2_OIS (71h) / SPI2_CTRL2_OIS (71h)).

## 6.7 Enhanced EIS

The LSM6DSV offers advanced design flexibility for EIS applications: enhanced EIS functionality has a dedicated channel and processing with independent filtering.

Enhanced EIS main features:

- Enhanced EIS channel gyroscope data can be read over the primary interfaces through I²C / MIPI I3C® / SPI;
- EIS data are available in free-run mode in the output registers (UI_OUTX_L_G_OIS_EIS (2Eh) and UI_OUTX_H_G_OIS_EIS (2Fh) through UI_OUTZ_L_G_OIS_EIS (32h) and UI_OUTZ_H_G_OIS_EIS (33h)) by setting the G_EIS_ON_G_OIS_OUT_REG bit to 1 in the CTRL_EIS (6Bh) register or in FIFO (by setting the G_EIS_FIFO_EN bit to 1 in the FIFO_CTRL4 (0Ah) register) with dedicated TAG and timestamp configurable using FIFO_CTRL4 (0Ah);
- Enhanced EIS option is compatible with mode 3 selection. When EIS data-out are intended to be read from the output registers (setting G_EIS_ON_G_OIS_OUT_REG bit), data from the gyroscope OIS chain can be only read from the auxiliary SPI interface.

**Figure 23. LSM6DSV supports UI, enhanced EIS and OIS processing simultaneously**

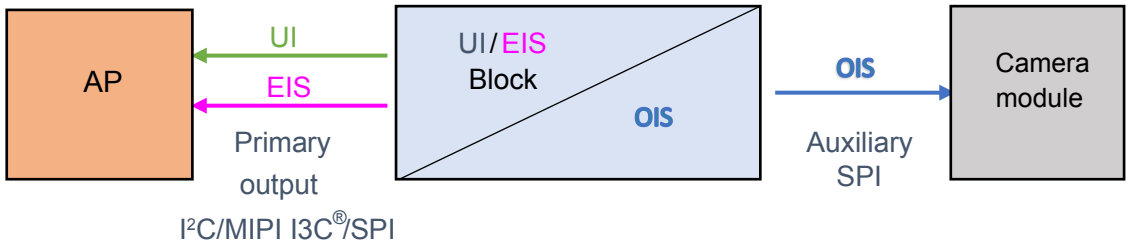
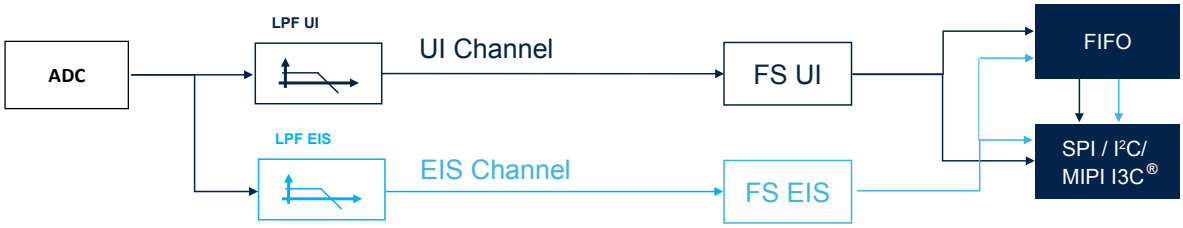



**Figure 24. Gyroscope enhanced EIS and UI block diagram**




When enhanced EIS mode is activated through the ODR_EIS_[1:0] bits in the CTRL_EIS (6Bh) register:

- Gyroscope UI can be configured only in power-down mode or high-performance mode;
- Gyroscope EIS full scale can be selected by using the FS_G_EIS_[2:0] bits in the CTRL_EIS (6Bh) register;
- Gyroscope EIS data rate selectable at 1.92 kHz or 960 Hz configurable through the ODR_G_EIS_[1:0] bits in the CTRL_EIS (6Bh) register;
- LPF_EIS low-pass filter (refer to Figure 24) bandwidth selection can be configured through the LPF_G_EIS_BW bit in the CTRL_EIS (6Bh) register.

## 6.8 OIS

This paragraph describes OIS functionality. There is a dedicated gyroscope and accelerometer DSP for OIS.

The device also supports self-test functionality on the OIS side.

### 6.8.1 Enabling OIS functionality and connection schemes

There are two different ways in order to enable and configure OIS functionality:

- **Auxiliary SPI full control**: Enabling and configuration done from the auxiliary SPI
- **Primary interface full control**: Enabling and configuration done from the primary interface

The configurations that allow selecting these two different options are done using the OIS_CTRL_FROM_UI bit in the FUNC_CFG_ACCESS (01h) register as described in the following table.

**Table 20. OIS configurations**

| OIS_CTRL_FROM_UI | OIS configuration option |
|---|---|
| 0 | Auxiliary SPI full control |
| 1 | Primary interface full control |

#### 6.8.1.1 *Auxiliary SPI full control*

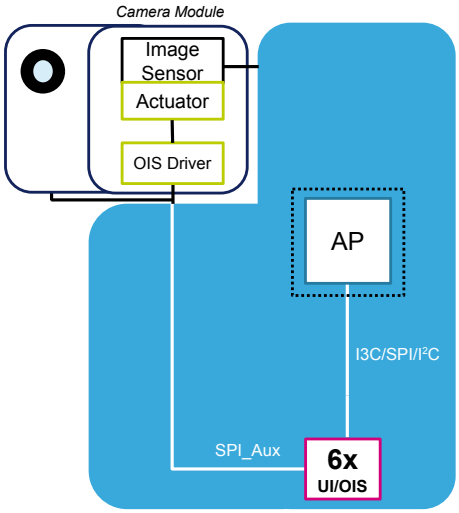
This is the default condition of the device. The camera module is completely independent from the application processor as shown in Figure 25.

The auxiliary SPI can configure OIS functionality through SPI2_INT_OIS (6Fh), SPI2_CTRL1_OIS (70h), SPI2_CTRL2_OIS (71h), SPI2_CTRL3_OIS (72h).

Reading from the auxiliary SPI is enabled only when the SPI2_READ_EN bit in the SPI2_CTRL1_OIS (70h) register is set to 1.

The primary interface can access the OIS control registers (UI_INT_OIS (6Fh), UI_CTRL1_OIS (70h), UI_CTRL2_OIS (71h), UI_CTRL3_OIS (72h)) in read mode.

**Figure 25. Auxiliary SPI full control**

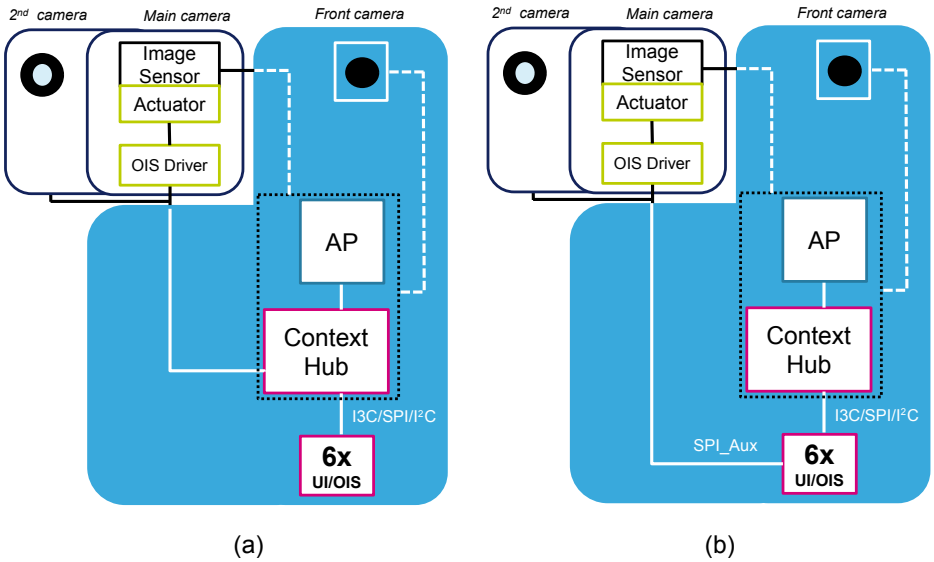


#### 6.8.1.2 *Primary interface full control*

This option allows the application processor to configure all OIS functionalities from the primary interface. This option allows using embedded OIS data for both the main and front camera, connecting them to the application processor (eventually adding a context hub) as shown in Figure 26: the AP can also do some processing on the data before sending them to the cameras.

In order to place the device in this mode, the OIS_CTRL_FROM_UI bit in the FUNC_CFG_ACCESS (01h) register must be set to 1 from the primary interface.

**Figure 26. OIS Primary interface full control**




Then, the AP can configure OIS functionalities through UI_INT_OIS (6Fh), UI_CTRL1_OIS (70h), UI_CTRL2_OIS (71h), UI_CTRL3_OIS (72h).

Reading from the auxiliary SPI can be enabled by setting the SPI2_ READ_EN bit in the UI_CTRL1_OIS (70h) register to 1 in order to directly read OIS data (as shown in Figure 26 (b)). The auxiliary SPI can access the SPI2_INT_OIS (6Fh), SPI2_CTRL1_OIS (70h), SPI2_CTRL2_OIS (71h), and SPI2_CTRL3_OIS (72h) registers in read-only mode.

*Note: The OIS_CTRL_FROM_UI bit is reset by the software reset procedure.*

## 6.9 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but It can wake up only when needed and burst the significant data out from the FIFO.

The LSM6DSV embeds 1.5 KB of data in FIFO (up to 4.5 KB with the compression feature enabled) to store the following data:

- Gyroscope
- Accelerometer
- External sensors (up to 4)
- Step counter
- Timestamp
- Temperature

Writing data in the FIFO can be configured to be triggered by the:

- Accelerometer / gyroscope data-ready signal
- Sensor hub data-ready signal
- Step detection signal

The applications have maximum flexibility in choosing the rate of batching for physical sensors with FIFO-dedicated configurations: accelerometer, gyroscope and temperature sensor batch rates can be selected by the user. External sensor writing in FIFO can be triggered by the accelerometer data-ready signal or by an external sensor interrupt. The step counter can be stored in FIFO with associated timestamp each time a step is detected. It is possible to select decimation for timestamp batching in FIFO with a factor of 1, 8, or 32.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO_DATA_OUT_TAG byte that allows recognizing the meaning of a word in FIFO.

FIFO allows correct reconstruction of the timestamp information for each sensor stored in FIFO. If a change in the ODR or BDR (batch data rate) configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

Finally, FIFO embeds a compression algorithm that the user can enable in order to have up to 4.5 KB data stored in FIFO and take advantage of interface communication length for FIFO flushing and communication power consumption.

The programmable FIFO watermark threshold can be set using the WTM[7:0] bits in the FIFO_CTRL1 (07h) register. To monitor the FIFO status, dedicated registers (FIFO_STATUS1 (1Bh), FIFO_STATUS2 (1Ch)) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO watermark status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pins of these status events, the configuration can be set in INT1_CTRL (0Dh) and INT2_CTRL (0Eh).

The FIFO buffer can be configured according to seven different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- ContinuousWTM-to-full mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

Each mode is selected by the FIFO_MODE_[2:0] bits in the FIFO_CTRL4 (0Ah) register.

### 6.9.1 Bypass mode

In bypass mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 000), the FIFO is not operational and it remains empty. Bypass mode is also used to reset the FIFO when in FIFO mode.

### 6.9.2 FIFO mode

In FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, bypass mode should be selected by writing FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0]) to 000. After this reset command, it is possible to restart FIFO mode by writing FIFO_CTRL4 (0Ah) (FIFO_MODE_[2:0]) to 001.

The FIFO buffer memorizes up to 4.5 KB of data (with compression enabled) but the depth of the FIFO can be resized by setting the WTM[7:0] bits in FIFO_CTRL1 (07h). If the STOP_ON_WTM bit in FIFO_CTRL2 (08h) is set to 1, FIFO depth is limited up to the WTM[7:0] bits in the FIFO_CTRL1 (07h) register.

### 6.9.3 Continuous mode

Continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag FIFO_STATUS2 (1Ch)(FIFO_WTM_IA) is asserted when the number of unread samples in FIFO is greater than or equal to FIFO_CTRL1 (07h) (WTM[7:0]).

It is possible to route the FIFO_WTM_IA flag to the INT1 pin by writing in register INT1_CTRL (0Dh) (INT1_FIFO_TH) = 1 or to the INT2 pin by writing in register INT2_CTRL (0Eh)(INT2_FIFO_TH) = 1.

A full-flag interrupt can be enabled, INT1_CTRL (0Dh)(INT1_FIFO_FULL) = 1 or INT2_CTRL (0Eh) (INT2_FIFO_FULL) = 1, in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the FIFO_OVR_IA flag in FIFO_STATUS2 (1Ch) is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in FIFO_STATUS1 (1Bh) and FIFO_STATUS2 (1Ch)(DIFF_FIFO_[8:0]).

### 6.9.4 Continuous-to-FIFO mode

In continuous-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to 1, FIFO operates in FIFO mode.

When the selected trigger bit is equal to 0, FIFO operates in continuous mode.

### 6.9.5 ContinuousWTM-to-full mode

In continuousWTM-to-full mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 010), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to 0, FIFO operates in continuous mode with the FIFO size limited to the FIFO watermark level (defined by the WTM[7:0] bits in the FIFO_CTRL1 (07h) register).

When the selected trigger bit is equal to 1, FIFO continues to store data until it is full.

### 6.9.6 Bypass-to-continuous mode

In bypass-to-continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 100), data measurement storage inside FIFO operates in Continuous mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

### 6.9.7 Bypass-to-FIFO mode

In bypass-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 111), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

### 6.9.8 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (FIFO_DATA_OUT_TAG (78h), in order to identify the sensor, and 6 bytes of fixed data (FIFO_DATA_OUT registers from (79h) to (7Eh)).

The DIFF_FIFO_[8:0] field in the FIFO_STATUS1 (1Bh) and FIFO_STATUS2 (1Ch) registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

In addition, it is possible to configure a counter of the batch events of accelerometer or gyroscope sensors. The flag COUNTER_BDR_IA in FIFO_STATUS2 (1Ch) alerts that the counter reaches a selectable threshold (CNT_BDR_TH_[9:0] field in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch)). This allows triggering the reading of FIFO with the desired latency of one single sensor. The sensor is selectable using the TRIG_COUNTER_BDR_[1:0] bits in COUNTER_BDR_REG1 (0Bh). As for the other FIFO status events, the flag COUNTER_BDR_IA can be routed on the INT1 or INT2 pins by asserting the corresponding bits (INT1_CNT_BDR of INT1_CTRL (0Dh) and INT2_CNT_BDR of INT2_CTRL (0Eh)).

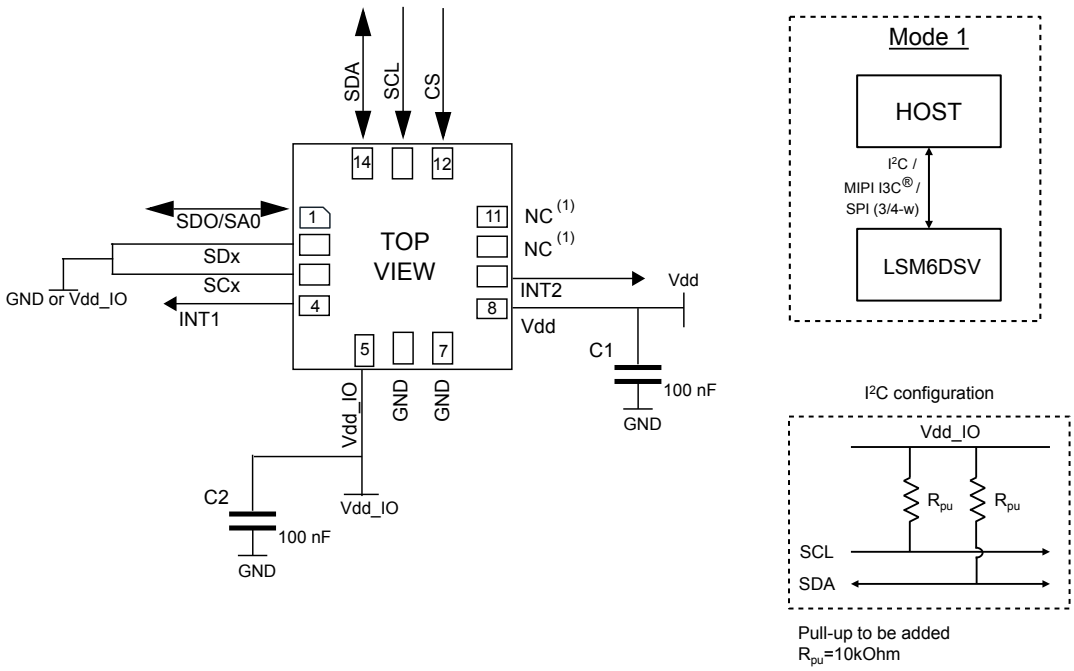
In order to maximize the amount of accelerometer and gyroscope data in FIFO, the user can enable the compression algorithm by setting to 1 both the FIFO_COMPR_EN bit in EMB_FUNC_EN_B (05h) (embedded functions registers bank) and the FIFO_COMPR_RT_EN bit in FIFO_CTRL2 (08h). When compression is enabled, it is also possible to force writing noncompressed data at a selectable rate using the UNCOMPR_RATE_[1:0] field in FIFO_CTRL2 (08h).

Meta information about accelerometer and gyroscope sensor configuration changes can be managed by enabling the ODR_CHG_EN bit in FIFO_CTRL2 (08h).

# 7 Application hints

## 7.1 LSM6DSV electrical connections in mode 1

Figure 27. **LSM6DSV electrical connections in mode 1**




1. *Leave pin electrically unconnected and soldered to PCB.*

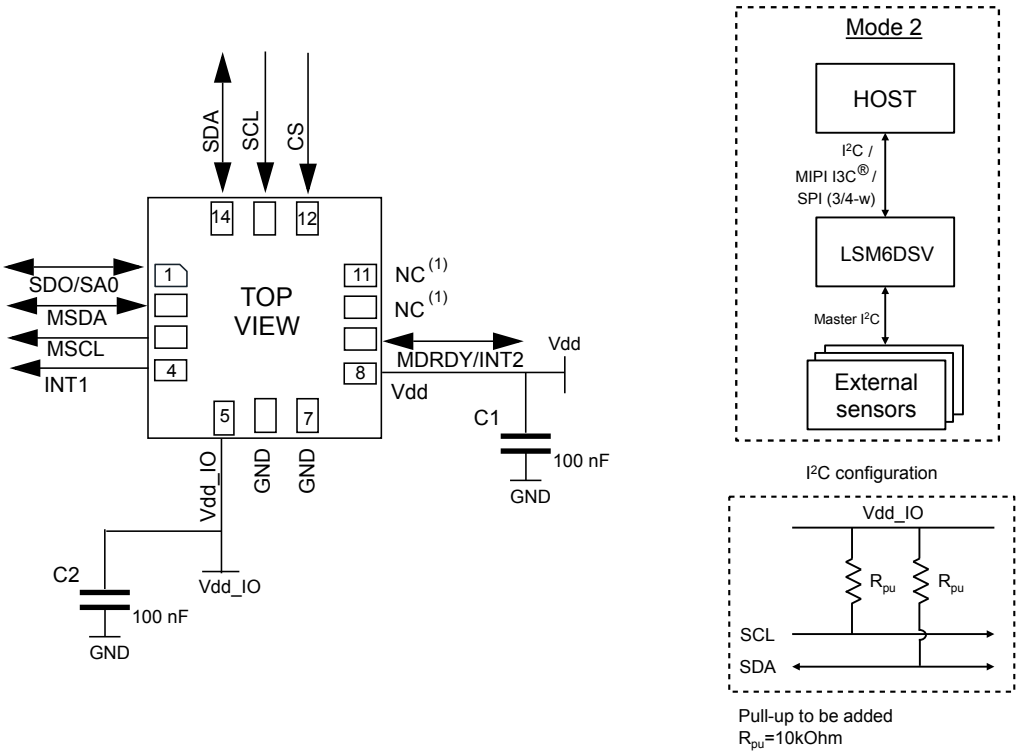
The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C® interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C® interface.

## 7.2 LSM6DSV electrical connections in mode 2

Figure 28. **LSM6DSV electrical connections in mode 2**




1. *Leave pin electrically unconnected and soldered to PCB.*

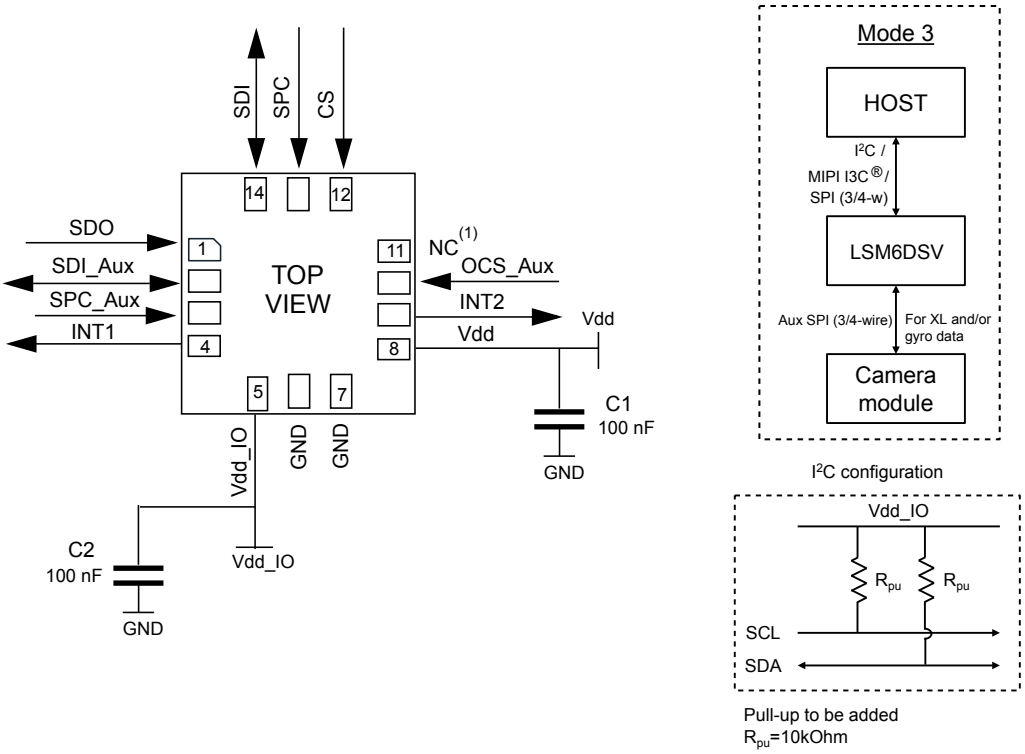
The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C® primary interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C® primary interface.

## 7.3 LSM6DSV electrical connections in mode 3

**Figure 29. LSM6DSV electrical connections in mode 3 (auxiliary 3/4-wire SPI)**




1. *Leave pin electrically unconnected and soldered to PCB.*

*Note: When mode 3 is used, the pull-up on pins 10 and 11 can be disabled (refer to Table 21. Internal pin status). To avoid leakage current, it is recommended to not leave the SPI lines floating (also when the OIS system is off).*

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device is selectable and accessible through the SPI/I²C/MIPI I3C® primary interface.

Measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C® primary interface and auxiliary SPI.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C® interface.

**Table 21. Internal pin status**

| pin# | Name | Mode 1 function | Mode 2 function | Mode 3 function | Pin status mode 1 | Pin status mode 2 | Pin status mode 3[1] |
|---|---|---|---|---|---|---|---|
| 1 | SDO | SPI 4-wire interface serial data output (SDO) | SPI 4-wire interface serial data output (SDO) | SPI 4-wire interface serial data output (SDO) | Default: input without pull-up.<br>Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h). | Default: input without pull-up.<br>Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h). | Default: Input without pull-up.<br>Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h). |
| | SA0 | I²C least significant bit of the device address (SA0)<br>MIPI I3C® least significant bit of the static address (SA0) | I²C least significant bit of the device address (SA0)<br>MIPI I3C® least significant bit of the static address (SA0) | I²C least significant bit of the device address (SA0)<br>MIPI I3C® least significant bit of the static address (SA0) | | | |
| 2 | SDx | Connect to Vdd_IO or GND | I²C serial data master (MSDA) | Auxiliary SPI 3/4-wire interface serial data input (SDI) and SPI 3-wire serial data output (SDO) | Default: input without pull-up.<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in register IF_CFG (03h). | Default: input without pull-up.<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in register IF_CFG (03h). | Default: input without pull-up.<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in register IF_CFG (03h). |
| 3 | SCx | Connect to Vdd_IO or GND | I²C serial clock master (MSCL) | Auxiliary SPI 3/4-wire interface serial port clock (SPC_Aux) | Default: input without pull-up.<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in register IF_CFG (03h). | Default: input without pull-up.<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in register IF_CFG (03h). | Default: input without pull-up.<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in register IF_CFG (03h). |
| 4 | INT1 | Programmable interrupt 1 | Programmable interrupt 1 | Programmable interrupt 1 | Default: output forced to ground | Default: output forced to ground | Default: output forced to ground |
| 5 | Vdd_IO | Power supply for I/O pins | Power supply for I/O pins | Power supply for I/O pins | | | |
| 6 | GND | 0 V supply | 0 V supply | 0 V supply | | | |
| 7 | GND | 0 V supply | 0 V supply | 0 V supply | | | |
| 8 | Vdd | Power supply | Power supply | Power supply | | | |
| 9 | INT2 | Programmable interrupt 2 (INT2) / Data enabled (DEN) | Programmable interrupt 2 (INT2) / Data enabled (DEN) / I²C master external synchronization signal (MDRDY) | Programmable interrupt 2 (INT2) / Data enabled (DEN) | Default: output forced to ground | Default: output forced to ground | Default: output forced to ground |
| 10 | OCS_Aux | Connect to Vdd_IO or leave unconnected | Connect to Vdd_IO or leave unconnected | Auxiliary SPI 3/4-wire interface enabled | Default: input with pull-up.<br>Pull-up is disabled if bit OIS_PU_DIS = 1 in register PIN_CTRL (02h). | Default: input with pull-up.<br>Pull-up is disabled if bit OIS_PU_DIS = 1 in PIN_CTRL (02h). | Default: input without pull-up (regardless of the value of bit OIS_PU_DIS in register PIN_CTRL (02h)). |
| 11 | SDO_Aux | Connect to Vdd_IO or leave unconnected | Connect to Vdd_IO or leave unconnected | Auxiliary SPI 3-wire interface: leave unconnected / Auxiliary SPI 4-wire interface: serial data output (SDO_Aux) | Default: input with pull-up.<br>Pull-up is disabled if bit OIS_PU_DIS = 1 in register PIN_CTRL (02h). | Default: input with pull-up.<br>Pull-up is disabled if bit OIS_PU_DIS = 1 in register PIN_CTRL (02h). | Default: input without pull-up.<br>Pull-up is enabled if bit SIM_OIS = 1 (Aux_SPI 3-wire) in reg 70h and bit OIS_PU_DIS = 0 in register PIN_CTRL (02h). |
| 12 | CS | I²C/SPI mode selection<br>(1:SPI idle mode / I²C communication enabled;<br>0: SPI communication mode / I²C disabled) | I²C/SPI mode selection<br>(1:SPI idle mode / I²C communication enabled;<br>0: SPI communication mode / I²C disabled) | I²C/SPI mode selection<br>(1:SPI idle mode / I²C communication enabled;<br>0: SPI communication mode / I²C disabled) | Default: input with pull-up.<br>Pull-up is disabled if bit I2C_I3C_disable = 1 in register IF_CFG (03h). | Default: input with pull-up.<br>Pull-up is disabled if bit I2C_I3C_disable = 1 in register IF_CFG (03h). | Default: input with pull-up.<br>Pull-up is disabled if bit I2C_I3C_disable = 1 in register IF_CFG (03h). |
| 13 | SCL | I²C/MIPI I3C® serial clock (SCL) / SPI serial port clock (SPC) | I²C/MIPI I3C® serial clock (SCL) / SPI serial port clock (SPC) | I²C/MIPI I3C® serial clock (SCL) / SPI serial port clock (SPC) | Default: input without pull-up | Default: input without pull-up | Default: input without pull-up |

| pin# | Name | Mode 1 function | Mode 2 function | Mode 3 function | Pin status mode 1 | Pin status mode 2 | Pin status mode 3[1] |
|---|---|---|---|---|---|---|---|
| 14 | SDA | I²C/MIPI I3C® serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO) | I²C/MIPI I3C® serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO) | I²C/MIPI I3C® serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO) | Default: input without pull-up. Pull-up is enabled if bit SDA_PU_EN = 1 in register IF_CFG (03h). | Default: input without pull-up. Pull-up is enabled if bit SDA_PU_EN = 1 in register IF_CFG (03h). | Default:input without pull-up. Pull-up is enabled if bit SDA_PU_EN = 1 in register IF_CFG (03h). |

1. *Mode 3 is enabled when the OIS_XL_EN bit or the OIS_G_EN bit in the UI_CTRL1_OIS (70h) / SPI2_CTRL1_OIS (70h) registers is set to 1.*

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on Vdd_IO.

# 8 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

All these registers are accessible from the primary SPI/I²C/MIPI I3C® interface only.

**Table 22. Registers address map**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| FUNC_CFG_ACCESS | R/W | 01 | 00000001 | 00000000 | |
| PIN_CTRL | R/W | 02 | 00000010 | 00100011 | |
| IF_CFG | R/W | 03 | 00000011 | 00000000 | |
| RESERVED | - | 04-07 | | | |
| FIFO_CTRL1 | R/W | 07 | 00000111 | 00000000 | |
| FIFO_CTRL2 | R/W | 08 | 00001000 | 00000000 | |
| FIFO_CTRL3 | R/W | 09 | 00001001 | 00000000 | |
| FIFO_CTRL4 | R/W | 0A | 00001010 | 00000000 | |
| COUNTER_BDR_REG1 | R/W | 0B | 00001011 | 00000000 | |
| COUNTER_BDR_REG2 | R/W | 0C | 00001100 | 00000000 | |
| INT1_CTRL | R/W | 0D | 00001101 | 00000000 | |
| INT2_CTRL | R/W | 0E | 00001110 | 00000000 | |
| WHO_AM_I | R | 0F | 00001111 | 01110000 | R (SPI2) |
| CTRL1 | R/W | 10 | 00010000 | 00000000 | R (SPI2) |
| CTRL2 | R/W | 11 | 00010001 | 00000000 | R (SPI2) |
| CTRL3 | R/W | 12 | 00010010 | 01000100 | R (SPI2) |
| CTRL4 | R/W | 13 | 00010011 | 00000000 | R (SPI2) |
| CTRL5 | R/W | 14 | 00010100 | 00000000 | R (SPI2) |
| CTRL6 | R/W | 15 | 00010101 | 00000000 | R (SPI2) |
| CTRL7 | R/W | 16 | 00010110 | 00000000 | R (SPI2) |
| CTRL8 | R/W | 17 | 0001 0111 | 00000000 | R (SPI2) |
| CTRL9 | R/W | 18 | 00011000 | 00000000 | R (SPI2) |
| CTRL10 | R/W | 19 | 00011001 | 00000000 | R (SPI2) |
| CTRL_STATUS | R | 1A | 00011010 | output | |
| FIFO_STATUS1 | R | 1B | 00011011 | output | |
| FIFO_STATUS2 | R | 1C | 00011100 | output | |
| ALL_INT_SRC | R | 1D | 00011101 | output | |
| STATUS_REG | R | 1E | 00011110 | output | |
| RESERVED | - | 1F | | | |
| OUT_TEMP_L | R | 20 | 00100000 | output | |
| OUT_TEMP_H | R | 21 | 00100001 | output | |
| OUTX_L_G | R | 22 | 00100010 | output | |
| OUTX_H_G | R | 23 | 00100011 | output | |
| OUTY_L_G | R | 24 | 00100100 | output | |

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| OUTY_H_G | R | 25 | 00100101 | output | |
| OUTZ_L_G | R | 26 | 00100110 | output | |
| OUTZ_H_G | R | 27 | 00100111 | output | |
| OUTX_L_A | R | 28 | 00101000 | output | |
| OUTX_H_A | R | 29 | 00101001 | output | |
| OUTY_L_A | R | 2A | 00101010 | output | |
| OUTY_H_A | R | 2B | 00101011 | output | |
| OUTZ_L_A | R | 2C | 00101100 | output | |
| OUTZ_H_A | R | 2D | 00101101 | output | |
| UI_OUTX_L_G_OIS_EIS | R | 2E | 00101110 | output | |
| UI_OUTX_H_G_OIS_EIS | R | 2F | 00101111 | output | |
| UI_OUTY_L_G_OIS_EIS | R | 30 | 00110000 | output | |
| UI_OUTY_H_G_OIS_EIS | R | 31 | 00110001 | output | |
| UI_OUTZ_L_G_OIS_EIS | R | 32 | 00110010 | output | |
| UI_OUTZ_H_G_OIS_EIS | R | 33 | 00110011 | output | |
| UI_OUTX_L_A_OIS_DualC | R | 34 | 00110100 | output | |
| UI_OUTX_H_A_OIS_DualC | R | 35 | 00110101 | output | |
| UI_OUTY_L_A_OIS_DualC | R | 36 | 00110110 | output | |
| UI_OUTY_H_A_OIS_DualC | R | 37 | 00110111 | output | |
| UI_OUTZ_L_A_OIS_DualC | R | 38 | 00111000 | output | |
| UI_OUTZ_H_A_OIS_DualC | R | 39 | 00111001 | output | |
| RESERVED | - | 3A-3F | | | |
| TIMESTAMP0 | R | 40 | 01000000 | output | R (SPI2) |
| TIMESTAMP1 | R | 41 | 01000001 | output | R (SPI2) |
| TIMESTAMP2 | R | 42 | 01000010 | output | R (SPI2) |
| TIMESTAMP3 | R | 43 | 01000011 | output | R (SPI2) |
| UI_STATUS_REG_OIS | R | 44 | 01000100 | output | |
| WAKE_UP_SRC | R | 45 | 01000101 | output | |
| TAP_SRC | R | 46 | 01000110 | output | |
| D6D_SRC | R | 47 | 01000111 | output | |
| STATUS_MASTER_ MAINPAGE | R | 48 | 01001000 | output | |
| EMB_FUNC_STATUS_ MAINPAGE | R | 49 | 01001001 | output | |
| FSM_STATUS_MAINPAGE | R | 4A | 01001010 | output | |
| RESERVED | - | 4B-4E | | | |
| INTERNAL_FREQ_FINE | R | 4F | 01001111 | output | |
| FUNCTIONS_ENABLE | RW | 50 | 01010000 | 00000000 | |
| DEN | R/W | 51 | 01010001 | 00001110 | |
| INACTIVITY_DUR | R/W | 54 | 01010100 | 00000100 | |
| INACTIVITY_THS | R/W | 55 | 01010101 | 00000000 | |

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| TAP_CFG0 | R/W | 56 | 01010110 | 00000000 | |
| TAP_CFG1 | R/W | 57 | 01010111 | 00000000 | |
| TAP_CFG2 | R/W | 58 | 01011000 | 00000000 | |
| TAP_THS_6D | R/W | 59 | 01011001 | 00000000 | |
| TAP_DUR | R/W | 5A | 01011010 | 00000000 | |
| WAKE_UP_THS | R/W | 5B | 01011011 | 00000000 | |
| WAKE_UP_DUR | R/W | 5C | 01011100 | 00000000 | |
| FREE_FALL | R/W | 5D | 01011101 | 00000000 | |
| MD1_CFG | R/W | 5E | 01011110 | 00000000 | |
| MD2_CFG | R/W | 5F | 01011111 | 00000000 | |
| RESERVED | - | 60-62 | | | |
| EMB_FUNC_CFG | R/W | 63 | 01100011 | 00000000 | |
| UI_HANDSHAKE_CTRL | R/W | 64 | 01100100 | 00000000 | |
| UI_SPI2_SHARED_0 | R/W | 65 | 01100101 | 00000000 | |
| UI_SPI2_SHARED_1 | R/W | 66 | 01100110 | 00000000 | |
| UI_SPI2_SHARED_2 | R/W | 67 | 01100111 | 00000000 | |
| UI_SPI2_SHARED_3 | R/W | 68 | 01101000 | 00000000 | |
| UI_SPI2_SHARED_4 | R/W | 69 | 01101001 | 00000000 | |
| UI_SPI2_SHARED_5 | R/W | 6A | 01101010 | 00000000 | |
| CTRL_EIS | R/W | 6B | 01101011 | 00000000 | |
| RESERVED | - | 6C - 6E | | | |
| UI_INT_OIS | R (SPI2 full-control mode)<br>R/W (primary IF full-control mode) | 6F | 01101111 | 00000000 | |
| UI_CTRL1_OIS | R (SPI2 full-control mode)<br>R/W (primary IF full-control mode) | 70 | 01110000 | 00000000 | |
| UI_CTRL2_OIS | R (SPI2 full-control mode)<br>R/W (primary IF full-control mode) | 71 | 01110001 | 00000000 | |
| UI_CTRL3_OIS | R (SPI2 full-control mode)<br>R/W (primary IF full-control mode) | 72 | 01110010 | 00000000 | |
| X_OFS_USR | R/W | 73 | 01110011 | 00000000 | |
| Y_OFS_USR | R/W | 74 | 01110100 | 00000000 | |
| Z_OFS_USR | R/W | 75 | 01110101 | 00000000 | |
| RESERVED | - | 76-77 | | | |
| FIFO_DATA_OUT_TAG | R | 78 | 01111000 | output | |
| FIFO_DATA_OUT_X_L | R | 79 | 01111001 | output | |
| FIFO_DATA_OUT_X_H | R | 7A | 01111010 | output | |
| FIFO_DATA_OUT_Y_L | R | 7B | 01111011 | output | |
| FIFO_DATA_OUT_Y_H | R | 7C | 01111100 | output | |
| FIFO_DATA_OUT_Z_L | R | 7D | 01111101 | output | |
| FIFO_DATA_OUT_Z_H | R | 7E | 01111110 | output | |

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

# 9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate, and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

## 9.1 FUNC_CFG_ACCESS (01h)

Enable embedded functions register (R/W)

**Table 23. FUNC_CFG_ACCESS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EMB_FUNC_ REG_ACCESS | SHUB_REG _ACCESS | 0(1) | 0(1) | FSM_WR_ CTRL_EN | SW_POR | SPI2_RESET | OIS_CTRL _FROM_UI |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 24. FUNC_CFG_ACCESS register description**

| | |
|---|---|
| EMB_FUNC_REG_ACCESS | Enables access to the embedded functions configuration registers. (1)<br>Default value: 0 |
| SHUB_REG_ACCESS | Enables access to the sensor hub (I²C master) configuration registers. (2)<br>Default value: 0 |
| FSM_WR_CTRL_EN | Enables the control of the CTRL registers to FSM (FSM can change some configurations of the device autonomously). Default value: 0<br>(0: disabled; 1: enabled) |
| SW_POR | Global reset of the device. Default value: 0 |
| SPI2_RESET | Resets the control registers of SPI2 from the primary interface. This bit must be set to 1 and then back to 0 (this bit is not automatically cleared). Default value: 0 |
| OIS_CTRL_FROM_UI | Enables the full control of OIS configurations from the primary interface. Default value: 0<br>(0: OIS chain full control from primary interface disabled;<br>1: OIS chain full control from primary interface enabled) |

1. *Details concerning the embedded functions configuration registers are available in Section 12 Embedded functions register mapping and Section 13 Embedded functions register description.*
2. *Details concerning the sensor hub registers are available in Section 16 Sensor hub register mapping and Section 17 Sensor hub register description.*

## 9.2 PIN_CTRL (02h)

SDO, OCS_Aux, SDO_Aux pins pull-up register (R/W). This register is not reset during the software reset procedure (see bit 0 of the CTRL3 (12h) register).

**Table 25. PIN_CTRL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| OIS_ PU_DIS | SDO_ PU_EN | IBHR_ POR_EN | 0(1) | 0(1) | 0(1) | 1(2) | 1(2) |

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

**Table 26. PIN_CTRL register description**

| | |
|---|---|
| OIS_PU_DIS | Disables pull-up on both OCS_Aux and SDO_Aux pins. Default value: 0<br>(0: OCS_Aux and SDO_Aux pins with pull-up;<br>1: OCS_Aux and SDO_Aux pins pull-up disconnected) |
| SDO_PU_EN | Enables pull-up on SDO pin. Default value: 0<br>(0: SDO pin pull-up disconnected; 1: SDO pin with pull-up) |
| IBHR_POR_EN | Selects the action the device performs after "reset whole chip" I3C pattern. Default value: 1<br>(0: configuration reset (SW reset + dynamic address reset);<br>(1: global reset (POR reset)) |

## 9.3 IF_CFG (03h)

Interface configuration register (R/W). This register is not reset during the software reset procedure (see bit 0 of the CTRL3 (12h) register).

**Table 27. IF_CFG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SDA_PU_EN | SHUB_ PU_EN | ASF_CTRL | H_LACTIVE | PP_OD | SIM | 0(1) | I2C_I3C_ disable |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 28. IF_CFG register description**

| | |
|---|---|
| SDA_PU_EN | Enables pull-up on SDA pin. Default value: 0<br>(0: SDA pin pull-up disconnected;<br>1: SDA pin with pull-up) |
| SHUB_PU_EN | Enables master I²C pull-up. Default value: 0<br>(0: internal pull-up on auxiliary I²C line disabled;<br>1: internal pull-up on auxiliary I²C line enabled) |
| ASF_CTRL | Enables anti-spike filters. Default value: 0<br>(0: anti-spike filters are managed by the protocol and turned off after the broadcast address;<br>1: anti-spike filters on SCL and SDA lines are always enabled) |
| H_LACTIVE | Interrupt activation level. Default value: 0<br>(0: interrupt output pins active high;<br>1: interrupt output pins active low) |
| PP_OD | Push-pull/open-drain selection on INT1 and INT2 pins. Default value: 0<br>(0: push-pull mode;<br>1: open-drain mode) |
| SIM | SPI serial interface mode selection. Default value: 0<br>(0: 4-wire interface;<br>1: 3-wire interface) |
| I2C_I3C_disable | Disables I²C and MIPI I3C® interfaces. Default value: 0<br>(0: SPI, I²C and MIPI I3C® interfaces enabled;<br>1: I²C and MIPI I3C® interfaces disabled) |

## 9.4 FIFO_CTRL1 (07h)

FIFO control register 1 (R/W)

**Table 29. FIFO_CTRL1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| WTM_7 | WTM_6 | WTM_5 | WTM_4 | WTM_3 | WTM_2 | WTM_1 | WTM_0 |

**Table 30. FIFO_CTRL1 register description**

| | |
|---|---|
| WTM_[7:0] | FIFO watermark threshold: 1 LSB = TAG (1 byte) + 1 sensor (6 bytes) written in FIFO.<br>Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level. |

## 9.5 FIFO_CTRL2 (08h)

FIFO control register 2 (R/W)

**Table 31. FIFO_CTRL2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| STOP_ON_WTM | FIFO_COMPR_RT_EN | 0(1) | ODR_CHG_EN | 0(1) | UNCOMPR_RATE_1 | UNCOMPR_RATE_0 | XL_DualC_BATCH_FROM_FSM |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 32. FIFO_CTRL2 register description**

| | |
|---|---|
| STOP_ON_WTM | Sensing chain FIFO stop values memorization at threshold level. Default value: 0<br>(0: FIFO depth is not limited;<br>1: FIFO depth is limited to threshold level, defined in FIFO_CTRL1 (07h)) |
| FIFO_COMPR_RT_EN(1) | Enables/disables compression algorithm runtime. Default value: 0<br>(0: FIFO compression algorithm disabled;<br>1: FIFO compression algorithm enabled) |
| ODR_CHG_EN | Enables ODR CHANGE virtual sensor to be batched in FIFO. Default value: 0<br>(0: ODR CHANGE virtual sensor not batched in FIFO;<br>1: ODR CHANGE virtual sensor batched in FIFO) |
| UNCOMPR_RATE_[1:0] | This field configures the compression algorithm to write uncompressed data at each rate.<br>(0: uncompressed data writing is not forced (default);<br>1: uncompressed data every 8 batch data rate;<br>2: uncompressed data every 16 batch data rate;<br>3: uncompressed data every 32 batch data rate) |
| XL_DualC_BATCH_FROM_FSM | When dual-channel mode is enabled, this bit enables FSM-triggered batching in FIFO of accelerometer channel 2. Default value: 0<br>(0: disabled; 1: enabled) |

1. *This bit is activated if the FIFO_COMPR_EN bit of EMB_FUNC_EN_B (05h) is set to 1.*

## 9.6 FIFO_CTRL3 (09h)

FIFO control register 3 (R/W)

**Table 33. FIFO_CTRL3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BDR_GY_3 | BDR_GY_2 | BDR_GY_1 | BDR_GY_0 | BDR_XL_3 | BDR_XL_2 | BDR_XL_1 | BDR_XL_0 |

**Table 34. FIFO_CTRL3 register description**

| | |
|---|---|
| BDR_GY_[3:0] | Selects batch data rate (write frequency in FIFO) for gyroscope data.<br>(0000: gyroscope not batched in FIFO (default);<br>0001: 1.875 Hz;<br>0010: 7.5 Hz;<br>0011: 15 Hz;<br>0100: 30 Hz;<br>0101: 60 Hz;<br>0110: 120 Hz;<br>0111: 240 Hz;<br>1000: 480 Hz;<br>1001: 960 Hz;<br>1010: 1.92 kHz;<br>1011: 3.84 kHz;<br>1100: 7.68 kHz<br>1101-1111: reserved) |
| BDR_XL_[3:0] | Selects batch data rate (write frequency in FIFO) for accelerometer data.<br>(0000: accelerometer not batched in FIFO (default);<br>0001: 1.875 Hz;<br>0010: 7.5 Hz;<br>0011: 15 Hz;<br>0100: 30 Hz;<br>0101: 60 Hz;<br>0110: 120 Hz;<br>0111: 240 Hz;<br>1000: 480 Hz;<br>1001: 960 Hz;<br>1010: 1.92 kHz;<br>1011: 3.84 kHz;<br>1100: 7.68 kHz<br>1101-1111: reserved) |

## 9.7 FIFO_CTRL4 (0Ah)

FIFO control register 4 (R/W)

**Table 35. FIFO_CTRL4 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DEC_TS_ BATCH_1 | DEC_TS_ BATCH_0 | ODR_T_ BATCH_1 | ODR_T_ BATCH_0 | G_EIS_ FIFO_EN | FIFO_ MODE_2 | FIFO_ MODE_1 | FIFO_ MODE_0 |

**Table 36. FIFO_CTRL4 register description**

| | |
|---|---|
| DEC_TS_BATCH_[1:0] | Selects decimation for timestamp batching in FIFO. Write rate is the maximum rate between the accelerometer and gyroscope BDR divided by decimation decoder.<br>(00: timestamp not batched in FIFO (default);<br>01: decimation 1: max(BDR_XL[Hz],BDR_GY[Hz]) [Hz];<br>10: decimation 8: max(BDR_XL[Hz],BDR_GY[Hz])/8 [Hz];<br>11: decimation 32: max(BDR_XL[Hz],BDR_GY[Hz])/32 [Hz]) |
| ODR_T_BATCH_[1:0] | Selects batch data rate (write frequency in FIFO) for temperature data<br>(00: temperature not batched in FIFO (default);<br>01: 1.875 Hz;<br>10: 15 Hz;<br>11: 60 Hz) |
| G_EIS_FIFO_EN | Enables FIFO batching of enhanced EIS gyroscope output values. Default value: 0<br>(0: disabled; 1: enabled) |
| FIFO_MODE_[2:0] | FIFO mode selection<br>(000: bypass mode: FIFO disabled (default);<br>001: FIFO mode: stops collecting data when FIFO is full;<br>010: continuousWTM-to-full mode: continuous mode with FIFO watermark size until trigger is deasserted, then data are stored in FIFO until the buffer is full;<br>011: continuous-to-FIFO mode: continuous mode until trigger is deasserted, then FIFO mode;<br>100: bypass-to-continuous mode: bypass mode until trigger is deasserted, then continuous mode;<br>101: reserved;<br>110: continuous mode: if the FIFO is full, the new sample overwrites the older one;<br>111: bypass-to-FIFO mode: bypass mode until trigger is deasserted, then FIFO mode.) |

## 9.8 COUNTER_BDR_REG1 (0Bh)

Counter batch data rate register 1 (R/W)

**Table 37. COUNTER_BDR_REG1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | TRIG_COUNTER_BDR_1 | TRIG_COUNTER_BDR_0 | 0(1) | 0(1) | 0(1) | CNT_BDR_TH_9 | CNT_BDR_TH_8 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 38. COUNTER_BDR_REG1 register description**

| | |
|---|---|
| TRIG_COUNTER_BDR_[1:0] | Selects the trigger for the internal counter of batch events between the accelerometer, gyroscope and EIS gyroscope.<br>(00: accelerometer batch event;<br>01: gyroscope batch event;<br>10 – 11: gyroscope EIS batch event) |
| CNT_BDR_TH_[9:8] | In conjunction with CNT_BDR_TH_[7:0] in COUNTER_BDR_REG2 (0Ch), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (1Ch) is set to 1. |

## 9.9 COUNTER_BDR_REG2 (0Ch)

Counter batch data rate register 2 (R/W)

**Table 39. COUNTER_BDR_REG2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CNT_BDR_TH_7 | CNT_BDR_TH_6 | CNT_BDR_TH_5 | CNT_BDR_TH_4 | CNT_BDR_TH_3 | CNT_BDR_TH_2 | CNT_BDR_TH_1 | CNT_BDR_TH_0 |

**Table 40. COUNTER_BDR_REG2 register description**

| | |
|---|---|
| CNT_BDR_TH_[7:0] | In conjunction with CNT_BDR_TH_[9:8] in COUNTER_BDR_REG1 (0Bh), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (1Ch) is set to 1. |

## 9.10 INT1_CTRL (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1 when the MIPI I3C® dynamic address is not assigned (I²C or SPI is used). Some bits can be also used to trigger an IBI (in-band interrupt) when the MIPI I3C® interface is used. The output of the pin is the OR combination of the signals selected here and in MD1_CFG (5Eh).

**Table 41. INT1_CTRL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | INT1_ CNT_BDR | INT1_ FIFO_FULL | INT1_ FIFO_OVR | INT1_ FIFO_TH | 0(1) | INT1_ DRDY_G | INT1_ DRDY_XL |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 42. INT1_CTRL register description**

| | |
|---|---|
| INT1_CNT_BDR | Enables COUNTER_BDR_IA interrupt on INT1 pin. Default value: 0 |
| INT1_FIFO_FULL | Enables FIFO full flag interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0 |
| INT1_FIFO_OVR | Enables FIFO overrun interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0 |
| INT1_FIFO_TH | Enables FIFO threshold interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0 |
| INT1_DRDY_G | Enables gyroscope data-ready interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0 |
| INT1_DRDY_XL | Enables accelerometer data-ready interrupt on INT1 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used. Default value: 0 |

## 9.11 INT2_CTRL (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2 when the MIPI I3C® dynamic address is not assigned (I²C or SPI is used). Some bits can be also used to trigger an IBI when the MIPI I3C® interface is used. The output of the pin is the OR combination of the signals selected here and in MD2_CFG (5Fh).

**Table 43. INT2_CTRL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_EMB_FUNC_ENDOP | INT2_CNT_BDR | INT2_FIFO_FULL | INT2_FIFO_OVR | INT2_FIFO_TH | INT2_DRDY_G_EIS | INT2_DRDY_G | INT2_DRDY_XL |

**Table 44. INT2_CTRL register description**

| | |
|---|---|
| INT2_EMB_FUNC_ENDOP | Enables routing the embedded functions end of operations signal to the INT2 pin. Default value: 0 |
| INT2_CNT_BDR | Enables COUNTER_BDR_IA interrupt on INT2. Default value: 0 |
| INT2_FIFO_FULL | Enables FIFO full flag interrupt on INT2 pin.Default value: 0 |
| INT2_FIFO_OVR | Enables FIFO overrun interrupt on INT2 pin. Default value: 0 |
| INT2_FIFO_TH | Enables FIFO threshold interrupt on INT2 pin. Default value: 0 |
| INT2_DRDY_G_EIS | Enables gyroscope EIS data-ready interrupt on INT2 pin. Default value: 0 |
| INT2_DRDY_G | Gyroscope data-ready interrupt on INT2 pin. Default value: 0 |
| INT2_DRDY_XL | Accelerometer data-ready interrupt on INT2 pin. Default value: 0 |

## 9.12 WHO_AM_I (0Fh)

WHO_AM_I register (R). This is a read-only register. Its value is fixed at 70h.

**Table 45. WhoAmI register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

## 9.13 CTRL1 (10h)

Accelerometer control register 1 (R/W)

**Table 46. CTRL1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | OP_MODE_XL_2 | OP_MODE_XL_1 | OP_MODE_XL_0 | ODR_XL_3 | ODR_XL_2 | ODR_XL_1 | ODR_XL_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 47. CTRL1 register description**

| | |
|---|---|
| OP_MODE_XL_[2:0] | Accelerometer operating mode selection.<br>(000: high-performance mode (default);<br>001: high-accuracy ODR mode;<br>010: reserved;<br>011: reserved;<br>100: low-power mode 1 (2 mean);<br>101: low-power mode 2 (4 mean);<br>110: low-power mode 3 (8 mean);<br>111: normal mode) |
| ODR_XL_[3:0] | Accelerometer ODR selection (see Table 48) |

**Table 48. Accelerometer ODR selection**

| ODR_XL_3 | ODR_XL_2 | ODR_XL_1 | ODR_XL_0 | ODR selection [Hz] |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Power-down (default) |
| 0 | 0 | 0 | 1 | 1.875 Hz (low-power mode) |
| 0 | 0 | 1 | 0 | 7.5 Hz (high-performance, normal mode) |
| 0 | 0 | 1 | 1 | 15 Hz (low-power, high-performance, normal mode) |
| 0 | 1 | 0 | 0 | 30 Hz (low-power, high-performance, normal mode) |
| 0 | 1 | 0 | 1 | 60 Hz (low-power, high-performance, normal mode) |
| 0 | 1 | 1 | 0 | 120 Hz (low-power, high-performance, normal mode) |
| 0 | 1 | 1 | 1 | 240 Hz (low-power, high-performance, normal mode) |
| 1 | 0 | 0 | 0 | 480 Hz (high-performance, normal mode) |
| 1 | 0 | 0 | 1 | 960 Hz (high-performance, normal mode) |
| 1 | 0 | 1 | 0 | 1.92 kHz (high-performance, normal mode) |
| 1 | 0 | 1 | 1 | 3.84 kHz (high-performance mode) |
| 1 | 1 | 0 | 0 | 7.68 kHz (high-performance mode) |
| Others | | | | Reserved |

## 9.14 CTRL2 (11h)

Gyroscope control register 2 (R/W)

**Table 49. CTRL2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | OP_MODE_G_2 | OP_MODE_G_1 | OP_MODE_G_0 | ODR_G_3 | ODR_G_2 | ODR_G_1 | ODR_G_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 50. CTRL2 register description**

| | |
|---|---|
| OP_MODE_G_[2:0] | Gyroscope operating mode selection.<br>(000: high-performance mode (default);<br>001: high-accuracy ODR mode;<br>010: reserved;<br>011: reserved;<br>100: sleep mode;<br>101: low-power mode;<br>110-111: reserved) |
| ODR_G_[3:0] | Gyroscope output data rate selection.<br>(See Table 51) |

**Table 51. Gyroscope ODR selection**

| ODR_G_3 | ODR_G_2 | ODR_G_1 | ODR_G_0 | ODR [Hz] |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Power-down (default) |
| 0 | 0 | 1 | 0 | 7.5 Hz (low-power, high-performance mode) |
| 0 | 0 | 1 | 1 | 15 Hz (low-power, high-performance mode) |
| 0 | 1 | 0 | 0 | 30 Hz (low-power, high-performance mode) |
| 0 | 1 | 0 | 1 | 60 Hz (low-power, high-performance mode) |
| 0 | 1 | 1 | 0 | 120 Hz (low-power, high-performance mode) |
| 0 | 1 | 1 | 1 | 240 Hz (low-power, high-performance mode) |
| 1 | 0 | 0 | 0 | 480 Hz (high-performance mode) |
| 1 | 0 | 0 | 1 | 960 Hz (high-performance mode) |
| 1 | 0 | 1 | 0 | 1.92 kHz (high-performance mode) |
| 1 | 0 | 1 | 1 | 3.84 kHz (high-performance mode) |
| 1 | 1 | 0 | 0 | 7.68 kHz (high-performance mode) |
| Others | | | | Reserved |

## 9.15 CTRL3 (12h)

Control register 3 (R/W)

**Table 52. CTRL3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BOOT | BDU | 0(1) | 0(1) | 0(1) | IF_INC | 0(1) | SW_RESET |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 53. CTRL3 register description**

| | |
|---|---|
| BOOT | Reboots memory content (the accelerometer must not be in power-down mode). This bit is automatically cleared. Default value: 0<br>(0: normal mode; 1: reboot memory content)<br>This bit is automatically cleared. |
| BDU | Block data update. Default value: 1<br>(0: continuous update;<br>1: output registers are not updated until LSB and MSB have been read) |
| IF_INC | Register address automatically incremented during a multiple byte access with a serial interface (I²C, MIPI I3C, or SPI). Default value: 1<br>(0: disabled; 1: enabled) |
| SW_RESET | Software reset, resets all control registers to their default value. This bit is automatically cleared. Default value: 0<br>(0: normal mode; 1: reset device) |

## 9.16 CTRL4 (13h)

Control register 4 (R/W)

**Table 54. CTRL4 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | INT2_on_INT1 | DRDY_MASK | INT2_DRDY_TEMP | DRDY_PULSED | INT2_IN_LH |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 55. CTRL4 register description**

| | |
|---|---|
| INT2_on_INT1 | Enables routing the embedded functions interrupt signals to the INT1 pin. Default value: 0<br>• The corresponding bits in the INT2 control registers need to be enabled.<br>• These interrupts are in OR with those enabled on the INT1 pin.<br>• They are not fed to the INT2 pin.<br>• The movable interrupts are:<br>– INT2_DRDY_G_EIS and INT2_EMB_FUNC_ENDOP, enabled through INT2_CTRL (0Eh)<br>– INT2_TIMESTAMP enabled through MD2_CFG (5Fh)<br>– INT2_DRDY_TEMP enabled through CTRL4 (13h) |
| DRDY_MASK | Enables / masks data-ready signal. Default value: 0<br>(0: disabled;<br>1: masks DRDY on pin (both accelerometer and gyroscope) until filter settling ends (accelerometer and gyroscope independently masked)) |
| INT2_DRDY_TEMP | Enables temperature sensor data-ready interrupt on the INT2 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used and INT2_ON_INT1 = 1 in CTRL4_C (13h). Default value: 0<br>(0: disabled; 1: enabled) |
| DRDY_PULSED | Enables pulsed data-ready mode. Default value: 0<br>(0: data-ready latched mode (returns to 0 only after the higher part of the associated output register has been read);<br>1: data-ready pulsed mode (the data-ready pulses are 65 µs long)) |
| INT2_IN_LH | Set to 1 in order to change the polarity of the INT2 pin input trigger for DEN or embedded functions. Default value: 0<br>(0: trigger for DEN and embedded functions pin is active low;<br>1: trigger for DEN and embedded functions pin is active high) |

## 9.17 CTRL5 (14h)

Control register 5 (R/W)

**Table 56. CTRL5 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | BUS_ACT_SEL_1 | BUS_ACT_SEL_0 | INT_EN_I3C |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 57. CTRL5 register description**

| | |
|---|---|
| BUS_ACT_SEL_[1:0] | Bus available time selection for IBI (in-band interrupt):<br>00: 2 µs;<br>01: 50 µs (default);<br>10: 1 ms;<br>11: 25 ms) |
| INT_EN_I3C | Enables INT pin when I3C is enabled. Default value: 0<br>(0: disabled; 1: enabled) |

## 9.18 CTRL6 (15h)

Control register 6 (R/W)

**Table 58. CTRL6 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | LPF1_G_BW_2 | LPF1_G_BW_1 | LPF1_G_BW_0 | FS_G_3 | FS_G_2 | FS_G_1 | FS_G_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 59. CTRL6 register description**

| | |
|---|---|
| LPF1_G_BW_[2:0] | Gyroscope low-pass filter (LPF1) bandwidth selection<br>Table 60 shows the selectable bandwidth values (available if OIS and/or EIS are disabled). |
| FS_G_[3:0] | Gyroscope UI chain full-scale selection:<br>(0000: ±125 dps (default);<br>0001: ±250 dps;<br>0010: ±500 dps;<br>0011: ±1000 dps;<br>0100: ±2000 dps;<br>1100: ±4000 dps(1)<br>Others: reserved) |

1. *When FS = ±4000 dps is selected, the OIS chain must be disabled (OIS_XL_EN, OIS_G_EN and SPI2_READ_EN bits of UI_CTRL1_OIS (70h) / SPI2_CTRL1_OIS (70h) must be set to 0).*

Table 60. **Gyroscope LPF1 bandwidth selection**

| LPF1_G_BW_[2:0] | 60 Hz | 120 Hz | 240 Hz | 480 Hz | 960 Hz | 1.92 kHz | 3.84 kHz | 7.68 kHz |
|---|---|---|---|---|---|---|---|---|
| 000 | N.A. | N.A. | N.A. | 174 | 353 | 273 | 280 | 282 |
| 001 | N.A. | N.A. | N.A. | 157 | 194 | 209 | 211 | 212 |
| 010 | N.A. | N.A. | N.A. | 131 | 148 | 154 | 156 | 156 |
| 011 | N.A. | N.A. | N.A. | 186 | 313 | 405 | 428 | 434 |
| 100 | N.A. | N.A. | 78 | 94 | 99 | 101 | 102 | 102 |
| 101 | N.A. | 43 | 53 | 57 | 58 | 58 | 58 | 58 |
| 110 | 18.0 | 24.2 | 27.3 | 28.4 | 28.7 | 28.8 | N.A. | N.A. |
| 111 | 12.1 | 13.7 | 14.2 | 14.3 | 14.4 | 14.4 | N.A. | N.A. |

## 9.19 CTRL7 (16h)

Control register 7 (R/W)

Table 61. **CTRL7 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | LPF1_G_EN |

1. *This bit must be set to 0 for the correct operation of the device.*

Table 62. **CTRL7 register description**

| | |
|---|---|
| LPF1_G_EN | Enables the gyroscope digital LPF1 filter. If the OIS chain is disabled, the bandwidth can be selected through LPF1_G_BW_[2:0] in CTRL6 (15h) |

## 9.20 CTRL8 (17h)

Control register 8 (R/W)

**Table 63. CTRL8 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| HP_LPF2_XL_BW_2 | HP_LPF2_XL_BW_1 | HP_LPF2_XL_BW_0 | 0(1) | XL_DualC_EN | 0(1) | FS_XL_1 | FS_XL_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 64. CTRL8 register description**

| | |
|---|---|
| HP_LPF2_XL_BW_[2:0] | Accelerometer LPF2 and HP filter configuration and cutoff setting. Refer to Table 65. |
| XL_DualC_EN | Enables dual-channel mode. When this bit is set to 1, data with the maximum full scale are sent to the output registers at addresses 34h to 39h. The UI processing chain is used. Default value: 0<br>(0: disabled; 1: enabled) |
| FS_XL_[1:0] | Accelerometer full-scale selection:<br>(00: ±2 *g*;<br>01: ±4 *g*;<br>10: ±8 *g*;<br>11: ±16 *g*) |

**Table 65. Accelerometer bandwidth configurations**

| Filter type | HP_SLOPE_XL_EN | LPF2_XL_EN | HP_LPF2_XL_BW_[2:0] | Bandwidth |
|---|---|---|---|---|
| Low pass | 0 | 0 | - | ODR/2(1) |
| | | 1 | 000 | ODR/4 |
| | | | 001 | ODR/10 |
| | | | 010 | ODR/20 |
| | | | 011 | ODR/45 |
| | | | 100 | ODR/100 |
| | | | 101 | ODR/200 |
| | | | 110 | ODR/400 |
| | | | 111 | ODR/800 |
| High pass | 1 | - | 000 | SLOPE (ODR/4) |
| | | | 001 | ODR/10 |
| | | | 010 | ODR/20 |
| | | | 011 | ODR/45 |
| | | | 100 | ODR/100 |
| | | | 101 | ODR/200 |
| | | | 110 | ODR/400 |
| | | | 111 | ODR/800 |

1. *This value is ODR/2 when the accelerometer is in high-performance mode, high-accuracy ODR mode and normal mode. It is equal to 2300 Hz when the accelerometer is in low-power mode 1 (2 mean), 912 Hz in low-power mode 2 (4 mean) and 431 Hz in low-power mode 3 (8 mean).*

## 9.21 CTRL9 (18h)

Control register 9 (R/W)

**Table 66. CTRL9 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | HP_REF_MODE_XL | XL_FASTSETTL_MODE | HP_SLOPE_XL_EN | LPF2_XL_EN | 0(1) | USR_OFF_W | USR_OFF_ON_OUT |

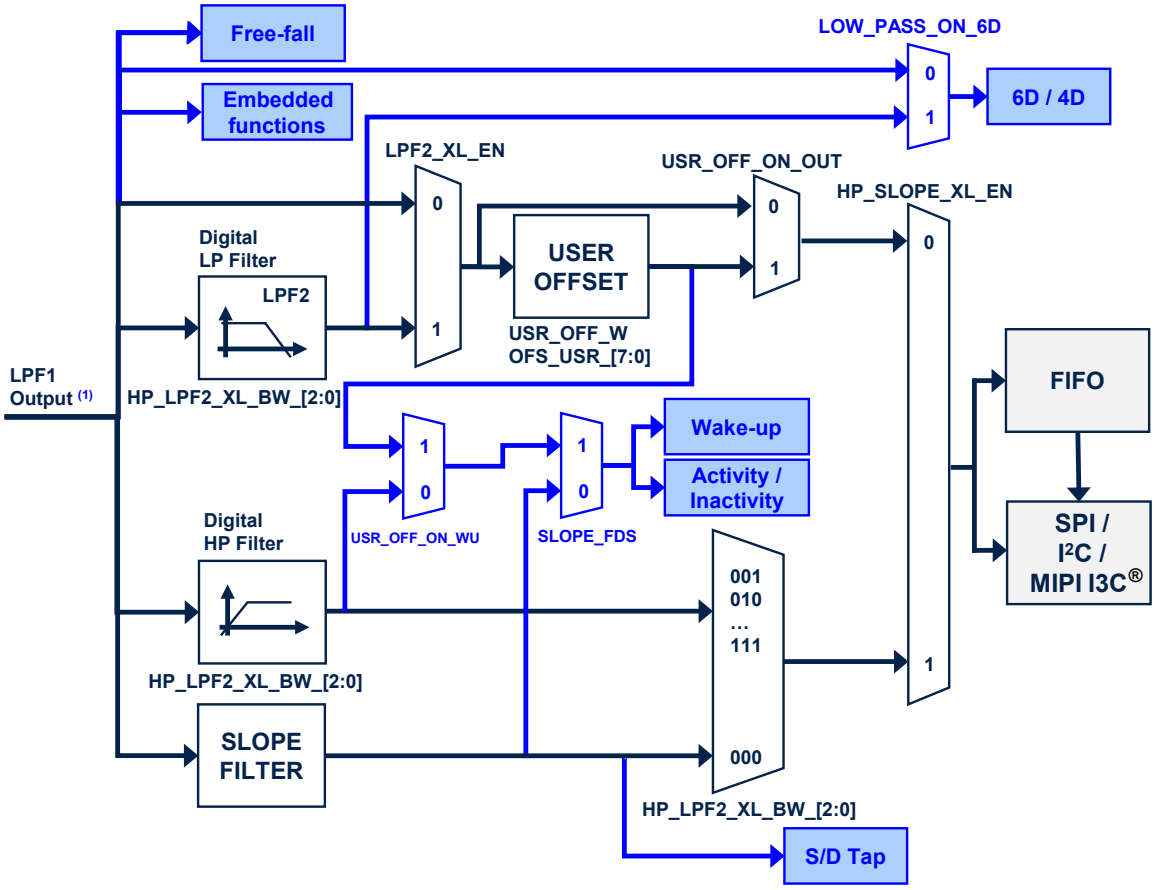
1. *This bit must be set to 0 for the correct operation of the device.*

**Table 67. CTRL9 register description**

| | |
|---|---|
| HP_REF_MODE_XL | Enables accelerometer high-pass filter reference mode (valid for high-pass path - HP_SLOPE_XL_EN bit must be 1). Default value: 0<br>(0: disabled, 1: enabled)(1) |
| XL_FASTSETTL_MODE | Enables accelerometer LPF2 and HPF fast-settling mode. The filter sets the first sample after writing this bit. Active only during device exit from power-down mode. Default value: 0<br>(0: disabled, 1: enabled) |
| HP_SLOPE_XL_EN | Accelerometer slope filter / high-pass filter selection. Refer to Figure 30. Default value: 0<br>(0: low-pass filter path selected;<br>1: high-pass filter path selected) |
| LPF2_XL_EN | Accelerometer high-resolution selection. Refer to Figure 30. Default value: 0<br>(0: output from first stage digital filtering selected;<br>1: output from LPF2 second filtering stage selected) |
| USR_OFF_W | Weight of XL user offset bits of registers X_OFS_USR (73h), Y_OFS_USR (74h), Z_OFS_USR (75h). Default value: 0<br>(0: $2^{-10}$ *g*/LSB;<br>1: $2^{-6}$ *g*/LSB) |
| USR_OFF_ON_OUT | Enables accelerometer user offset correction block; it is valid for the low-pass path. Refer to Figure 30. Default value: 0<br>(0: accelerometer user offset correction block bypassed;<br>1: accelerometer user offset correction block enabled) |

1. *When enabled, the first output data has to be discarded.*

Figure 30. **Accelerometer block diagram**




1. *The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode, high-accuracy ODR mode or normal mode. This value is equal to 2300 Hz when the accelerometer is in low-power mode 1 (2 mean), 912 Hz in low-power mode 2 (4 mean) or 431 Hz in low-power mode 3 (8 mean).*

## 9.22 CTRL10 (19h)

Control register 10 (R/W)

**Table 68. CTRL10 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | EMB_FUNC_DEBUG | 0(1) | 0(1) | ST_G_1 | ST_G_0 | ST_XL_1 | ST_XL_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 69. CTRL10 register description**

| | |
|---|---|
| EMB_FUNC_DEBUG | Enables debug mode for the embedded functions.<br>(0: disabled; 1: enabled) |
| ST_G_[1:0] | Gyroscope self-test selection<br>(00: normal mode (default);<br>01: positive sign self-test;<br>10: negative sign self-test;<br>11: reserved) |
| ST_XL_[1:0] | Accelerometer self-test selection<br>(00: normal mode (default);<br>01: positive sign self-test;<br>10: negative sign self-test;<br>11: reserved) |

## 9.23 CTRL_STATUS (1Ah)

(R)

**Table 70. CTRL_STATUS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | FSM_WR_CTRL_STATUS | - | 0 |

**Table 71. CTRL_STATUS register description**

| | |
|---|---|
| FSM_WR_CTRL_STATUS | This flag indicates the current controller of the device configuration registers. This flag must be used as an acknowledge flag when the value of the FSM_WR_CTRL_EN bit in the FUNC_CFG_ACCESS (01h) register is changed. Default value: 0<br>(0: all registers and configurations are writable from the standard interface;<br>1: some registers and configurations are under FSM control and are in read-only mode from the standard interface). |

## 9.24 FIFO_STATUS1 (1Bh)

FIFO status register 1 (R)

**Table 72. FIFO_STATUS1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DIFF_ FIFO_7 | DIFF_ FIFO_6 | DIFF_ FIFO_5 | DIFF_ FIFO_4 | DIFF_ FIFO_3 | DIFF_ FIFO_2 | DIFF_ FIFO_1 | DIFF_ FIFO_0 |

**Table 73. FIFO_STATUS1 register description**

| | |
|---|---|
| DIFF_FIFO_[7:0] | Number of unread sensor data (TAG + 6 bytes) stored in FIFO<br>In conjunction with DIFF_FIFO_8 in FIFO_STATUS2 (1Ch). |

## 9.25 FIFO_STATUS2 (1Ch)

FIFO status register 2 (R)

**Table 74. FIFO_STATUS2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FIFO_ WTM_IA | FIFO_ OVR_IA | FIFO_ FULL_IA | COUNTER_ BDR_IA | FIFO_OVR_ LATCHED | 0 | 0 | DIFF_ FIFO_8 |

**Table 75. FIFO_STATUS2 register description**

| | |
|---|---|
| FIFO_WTM_IA | FIFO watermark status. Default value: 0<br>(0: FIFO filling is lower than WTM;<br>1: FIFO filling is equal to or greater than WTM)<br>Watermark is set through bits WTM[7:0] in FIFO_CTRL2 (08h) and FIFO_CTRL1 (07h). |
| FIFO_OVR_IA | FIFO overrun status. Default value: 0<br>(0: FIFO is not completely filled; 1: FIFO is completely filled) |
| FIFO_FULL_IA | Smart FIFO full status. Default value: 0<br>(0: FIFO is not full; 1: FIFO will be full at the next ODR) |
| COUNTER_BDR_IA | Counter BDR reaches the CNT_BDR_TH_[10:0] threshold set in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch). Default value: 0<br>This bit is reset when these registers are read. |
| FIFO_OVR_LATCHED | Latched FIFO overrun status. Default value: 0<br>This bit is reset when this register is read. |
| DIFF_FIFO_8 | Number of unread sensor data (TAG + 6 bytes) stored in FIFO. Default value: 00<br>In conjunction with DIFF_FIFO[7:0] in FIFO_STATUS1 (1Bh) |

## 9.26 ALL_INT_SRC (1Dh)

Source register for all interrupts (R)

**Table 76. ALL_INT_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EMB_ FUNC_IA | SHUB_IA | SLEEP_ CHANGE_IA | D6D_IA | 0 | TAP_IA | WU_IA | FF_IA |

**Table 77. ALL_INT_SRC register description**

| | |
|---|---|
| EMB_FUNC_IA | Embedded functions interrupt status. Default value: 0<br>(0: embedded functions event not detected;<br>1: embedded functions event detected) |
| SHUB_IA | Sensor hub (I²C master) interrupt status. Default value: 0<br>(0: sensor hub interrupt not generated;<br>1: sensor hub interrupt generated) |
| SLEEP_CHANGE_IA | Detects change event in activity/inactivity status. Default value: 0<br>(0: change status not detected; 1: change status detected) |
| D6D_IA | Interrupt active for change in position of portrait, landscape, face-up, face-down. Default value: 0<br>(0: change in position not detected; 1: change in position detected) |
| TAP_IA | Single or double-tap event detection status depending on SINGLE_DOUBLE_TAP_bit value (see WAKE_UP_THS (5Bh) register). Default value: 0<br>(0: tap event not detected; 1: tap event detected) |
| WU_IA | Wake-up event status. Default value: 0<br>(0: event not detected, 1: event detected) |
| FF_IA | Free-fall event status. Default value: 0<br>(0: event not detected, 1: event detected) |

## 9.27 STATUS_REG (1Eh)

The STATUS_REG register is read by the primary interface SPI/I²C & MIPI I3C® (R).

**Table 78. STATUS_REG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TIMESTAMP_ ENDCOUNT | 0 | OIS_DRDY | GDA_EIS | 0 | TDA | GDA | XLDA |

**Table 79. STATUS_REG register description**

| | |
|---|---|
| TIMESTAMP_ENDCOUNT | Alerts timestamp overflow within 5.6 ms |
| OIS_DRDY | Accelerometer OIS or gyroscope OIS new output data available. Default value: 0<br>(0: no set of data (accelerometer or gyroscope) available on OIS chain;<br>1: a new set of data (accelerometer or gyroscope) is available on OIS chain) |
| GDA_EIS | Enhanced EIS gyroscope new data available. Default value: 0<br>(0: no set of data available at gyroscope output;<br>1: a new set of data is available at gyroscope output) |
| TDA | Temperature new data available. Default: 0<br>(0: no set of data is available at temperature sensor output;<br>1: a new set of data is available at temperature sensor output) |
| GDA | Gyroscope new data available. Default value: 0<br>(0: no set of data available at gyroscope output;<br>1: a new set of data is available at gyroscope output) |
| XLDA | Accelerometer new data available. Default value: 0<br>(0: no set of data available at accelerometer output;<br>1: a new set of data is available at accelerometer output) |

## 9.28 OUT_TEMP_L (20h), OUT_TEMP_H (21h)

Temperature data output register (R). L and H registers together express a 16-bit word in two's complement.

**Table 80. OUT_TEMP_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Temp7 | Temp6 | Temp5 | Temp4 | Temp3 | Temp2 | Temp1 | Temp0 |

**Table 81. OUT_TEMP_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Temp15 | Temp14 | Temp13 | Temp12 | Temp11 | Temp10 | Temp9 | Temp8 |

**Table 82. OUT_TEMP register description**

| | |
|---|---|
| Temp[15:0] | Temperature sensor output data<br>The value is expressed in two's complement. |

## 9.29 OUTX_L_G (22h) and OUTX_H_G (23h)

Angular rate sensor pitch axis (X) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL6 (15h)) and ODR settings (CTRL2 (11h)) of the gyroscope user interface.

**Table 83. OUTX_L_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 84. OUTX_H_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 85. OUTX_G register description**

| | |
|---|---|
| D[15:0] | Gyroscope UI chain pitch axis (X) angular rate output value |

## 9.30 OUTY_L_G (24h) and OUTY_H_G (25h)

Angular rate sensor roll axis (Y) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL6 (15h)) and ODR settings (CTRL2 (11h)) of the gyroscope user interface.

**Table 86. OUTY_L_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 87. OUTY_H_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 88. OUTY_G register description**

| | |
|---|---|
| D[15:0] | Gyroscope UI chain roll axis (Y) angular rate output value |

## 9.31 OUTZ_L_G (26h) and OUTZ_H_G (27h)

Angular rate sensor yaw axis (Z) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL6 (15h)) and ODR settings (CTRL2 (11h)) of the gyroscope user interface.

**Table 89. OUTZ_L_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 90. OUTZ_H_G register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 91. OUTZ_H_G register description**

| | |
|---|---|
| D[15:0] | Gyroscope UI chain yaw axis (Z) angular rate output value |

## 9.32 OUTX_L_A (28h) and OUTX_H_A (29h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL8 (17h)) and ODR settings (CTRL1 (10h)) of the accelerometer user interface.

**Table 92. OUTX_L_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 93. OUTX_H_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 94. OUTX_A register description**

| | |
|---|---|
| D[15:0] | Accelerometer UI chain X-axis linear acceleration output value |

## 9.33 OUTY_L_A (2Ah) and OUTY_H_A (2Bh)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL8 (17h)) and ODR settings (CTRL1 (10h)) of the accelerometer user interface.

**Table 95. OUTY_L_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 96. OUTY_H_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 97. OUTY_A register description**

| | |
|---|---|
| D[15:0] | Accelerometer UI chain Y-axis linear acceleration output value |

## 9.34 OUTZ_L_A (2Ch) and OUTZ_H_A (2Dh)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale (CTRL8 (17h)) and ODR settings (CTRL1 (10h)) of the accelerometer user interface.

**Table 98. OUTZ_L_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 99. OUTZ_H_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 100. OUTZ_A register description**

| | |
|---|---|
| D[15:0] | Accelerometer UI chain Z-axis linear acceleration output value |

## 9.35 UI_OUTX_L_G_OIS_EIS (2Eh) and UI_OUTX_H_G_OIS_EIS (2Fh)

Angular rate sensor pitch axis (X) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the gyroscope full-scale and ODR settings of the OIS gyroscope or the EIS gyroscope channel.

**Table 101. UI_OUTX_L_G_OIS_EIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 102. UI_OUTX_H_G_OIS_EIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 103. UI_OUTX_G_OIS_EIS register description**

| | |
|---|---|
| D[15:0] | Gyroscope pitch axis OIS/EIS output expressed in two's complement |

## 9.36 UI_OUTY_L_G_OIS_EIS (30h) and UI_OUTY_H_G_OIS_EIS (31h)

Angular rate sensor roll axis (Y) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the gyroscope full-scale and ODR settings of the OIS gyroscope or the EIS gyroscope channel.

**Table 104. UI_OUTY_L_G_OIS_EIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 105. UI_OUTY_H_G_OIS_EIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 106. UI_OUTY_G_OIS_EIS register description**

| | |
|---|---|
| D[15:0] | Gyroscope roll axis OIS/EIS output expressed in two's complement |

## 9.37 UI_OUTZ_L_G_OIS_EIS (32h) and UI_OUTZ_H_G_OIS_EIS (33h)

Angular rate sensor yaw axis (Z) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the gyroscope full-scale and ODR settings of the OIS gyroscope or the EIS gyroscope channel.

**Table 107. UI_OUTZ_L_G_OIS_EIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 108. UI_OUTZ_H_G_OIS_EIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 109. UI_OUTZ_G_OIS_EIS register description**

| | |
|---|---|
| D[15:0] | Gyroscope yaw axis OIS/EIS output expressed in two's complement |

## 9.38 UI_OUTX_L_A_OIS_DualC (34h) and UI_OUTX_H_A_OIS_DualC (35h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the accelerometer full-scale and ODR settings of the OIS accelerometer or according to the accelerometer dual-channel mode configuration.

**Table 110. UI_OUTX_L_A_OIS_DualC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 111. UI_OUTX_H_A_OIS_DualC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 112. UI_OUTX_A_OIS_DualC register description**

| | |
|---|---|
| D[15:0] | Accelerometer X-axis OIS/DualC output expressed in two's complement |

## 9.39 UI_OUTY_L_A_OIS_DualC (36h) and UI_OUTY_H_A_OIS_DualC (37h)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the accelerometer full-scale and ODR settings of the OIS accelerometer or according to the accelerometer dual-channel mode configuration.

**Table 113. UI_OUTY_L_A_OIS_DualC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 114. UI_OUTY_H_A_OIS_DualC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 115. UI_OUTY_A_OIS_DualC register description**

| | |
|---|---|
| D[15:0] | Accelerometer Y-axis OIS/DualC output expressed in two's complement |

## 9.40 UI_OUTZ_L_A_OIS_DualC (38h) and UI_OUTZ_H_A_OIS_DualC (39h)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the accelerometer full-scale and ODR settings of the OIS accelerometer or according to the accelerometer dual-channel mode configuration.

**Table 116. UI_OUTZ_L_A_OIS_DualC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 117. UI_OUTZ_H_A_OIS_DualC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 118. UI_OUTZ_A_OIS_DualC register description**

| | |
|---|---|
| D[15:0] | Accelerometer Z-axis OIS/DualC output expressed in two's complement |

## 9.41 TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)

Timestamp first data output register (R). The value is expressed as a 32-bit word and the bit resolution is 21.75 µs (typical).

**Table 119. TIMESTAMP output registers**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 120. TIMESTAMP output register description**

| | |
|---|---|
| D[31:0] | Timestamp output registers: 1LSB = 21.75 µs (typical) |

## 9.42 UI_STATUS_REG_OIS (44h)

**Table 121. UI_STATUS_REG_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | GYRO_ SETTLING | GDA_OIS | XLDA_OIS |

**Table 122. UI_STATUS_REG_OIS register description**

| | |
|---|---|
| GYRO_SETTLING | High when the gyroscope output is in the settling phase |
| GDA_OIS | Gyroscope OIS data available (reset when one of the high parts of the output data is read).<br>Default value: 0<br>(0: no set of data available at gyroscope OIS output;<br>1: a new set of data is available at gyroscope output) |
| XLDA_OIS | Accelerometer OIS data available (reset when one of the high parts of the output data is read).<br>Default value: 0<br>(0: no set of data available at gyroscope OIS output;<br>1: a new set of data is available at gyroscope output) |

## 9.43 WAKE_UP_SRC (45h)

Wake-up interrupt source register (R)

**Table 123. WAKE_UP_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | SLEEP_ CHANGE_IA | FF_IA | SLEEP_ STATE | WU_IA | X_WU | Y_WU | Z_WU |

**Table 124. WAKE_UP_SRC register description**

| | |
|---|---|
| SLEEP_CHANGE_IA | Detects change event in activity/inactivity status. Default value: 0<br>(0: change status not detected; 1: change status detected) |
| FF_IA | Free-fall event detection status. Default: 0<br>(0: free-fall event not detected; 1: free-fall event detected) |
| SLEEP_STATE | Sleep status bit. Default value: 0<br>(0: Activity status; 1: Inactivity status) |
| WU_IA | Wake-up event detection status. Default value: 0<br>(0: wake-up event not detected; 1: wake-up event detected.) |
| X_WU | Wake-up event detection status on X-axis. Default value: 0<br>(0: wake-up event on X-axis not detected; 1: wake-up event on X-axis detected) |
| Y_WU | Wake-up event detection status on Y-axis. Default value: 0<br>(0: wake-up event on Y-axis not detected; 1: wake-up event on Y-axis detected) |
| Z_WU | Wake-up event detection status on Z-axis. Default value: 0<br>(0: wake-up event on Z-axis not detected; 1: wake-up event on Z-axis detected) |

## 9.44 TAP_SRC (46h)

Tap source register (R)

**Table 125. TAP_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | TAP_IA | SINGLE_ TAP | DOUBLE_ TAP | TAP_SIGN | X_TAP | Y_TAP | Z_TAP |

**Table 126. TAP_SRC register description**

| | |
|---|---|
| TAP_IA | Tap event detection status. Default: 0<br>(0: tap event not detected; 1: tap event detected) |
| SINGLE_TAP | Single-tap event status. Default value: 0<br>(0: single tap event not detected; 1: single tap event detected) |
| DOUBLE_TAP | Double-tap event detection status. Default value: 0<br>(0: double-tap event not detected; 1: double-tap event detected.) |
| TAP_SIGN | Sign of acceleration detected by tap event. Default: 0<br>(0: positive sign of acceleration detected by tap event;<br>1: negative sign of acceleration detected by tap event) |
| X_TAP | Tap event detection status on X-axis. Default value: 0<br>(0: tap event on X-axis not detected; 1: tap event on X-axis detected) |
| Y_TAP | Tap event detection status on Y-axis. Default value: 0<br>(0: tap event on Y-axis not detected; 1: tap event on Y-axis detected) |
| Z_TAP | Tap event detection status on Z-axis. Default value: 0<br>(0: tap event on Z-axis not detected; 1: tap event on Z-axis detected) |

## 9.45 D6D_SRC (47h)

Portrait, landscape, face-up and face-down source register (R)

**Table 127. D6D_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | D6D_IA | ZH | ZL | YH | YL | XH | XL |

**Table 128. D6D_SRC register description**

| | |
|---|---|
| D6D_IA | Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0<br>(0: change position not detected; 1: change position detected) |
| ZH | Z-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over threshold) detected) |
| ZL | Z-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected) |
| YH | Y-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over-threshold) detected) |
| YL | Y-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected) |
| XH | X-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over threshold) detected) |
| XL | X-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected) |

## 9.46 EMB_FUNC_STATUS_MAINPAGE (49h)

Embedded function status register (R)

**Table 129. EMB_FUNC_STATUS_MAINPAGE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_FSM_LC | 0 | IS_ SIGMOT | IS_TILT | IS_ STEP_DET | 0 | 0 | 0 |

**Table 130. EMB_FUNC_STATUS_MAINPAGE register description**

| | |
|---|---|
| IS_FSM_LC | Interrupt status bit for FSM long counter timeout interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_SIGMOT | Interrupt status bit for significant motion detection<br>(1: interrupt detected; 0: no interrupt) |
| IS_TILT | Interrupt status bit for tilt detection<br>(1: interrupt detected; 0: no interrupt) |
| IS_STEP_DET | Interrupt status bit for step detection<br>(1: interrupt detected; 0: no interrupt) |

## 9.47 FSM_STATUS_MAINPAGE (4Ah)

Finite state machine status register (R)

**Table 131. FSM_STATUS_MAINPAGE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_FSM8 | IS_FSM7 | IS_FSM6 | IS_FSM5 | IS_FSM4 | IS_FSM3 | IS_FSM2 | IS_FSM1 |

**Table 132. FSM_STATUS_MAINPAGE register description**

| | |
|---|---|
| IS_FSM8 | Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM7 | Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM6 | Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM5 | Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM4 | Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM3 | Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM2 | Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM1 | Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt) |

## 9.48 INTERNAL_FREQ_FINE (4Fh)

Internal frequency register (R)

**Table 133. INTERNAL_FREQ_FINE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FREQ_ FINE_7 | FREQ_ FINE_6 | FREQ_ FINE_5 | FREQ_ FINE_4 | FREQ_ FINE_3 | FREQ_ FINE_2 | FREQ_ FINE_1 | FREQ_ FINE_0 |

**Table 134. INTERNAL_FREQ_FINE register description**

| | |
|---|---|
| FREQ_FINE_[7:0] | Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.13%. 8-bit format, two's complement. |

The actual timestamp resolution and the actual output data rate can be calculated using the following formulas:

$$t_{actual}[s] = \frac{1}{46080 \cdot (1 + 0.0013 \cdot FREQ_FINE)}$$

$$ODR_{actual}[Hz] = \frac{7680 \cdot (1 + 0.0013 \cdot FREQ_FINE)}{ODR_{coeff}}$$

**Table 135. $ODR_{coeff}$ values**

| Selected ODR [Hz] | ODRcoeff |
|---|---|
| 7.5 | 1024 |
| 15 | 512 |
| 30 | 256 |
| 60 | 128 |
| 120 | 64 |
| 240 | 32 |
| 480 | 16 |
| 960 | 8 |
| 1.92 kHz | 4 |
| 3.84 kHz | 2 |
| 7.68 kHz | 1 |

## 9.49 FUNCTIONS_ENABLE (50h)

Enable interrupt functions register (R/W)

**Table 136. FUNCTIONS_ENABLE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INTERRUPTS_ENABLE | TIMESTAMP_EN | 0(1) | 0(1) | DIS_RST_LIR_ALL_INT | 0(1) | INACT_EN_1 | INACT_EN_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 137. FUNCTIONS_ENABLE register description**

| | |
|---|---|
| INTERRUPTS_ENABLE | Enables basic interrupts (6D/4D, free-fall, wake-up, tap, activity/inactivity). Default value: 0<br>(0: interrupt disabled; 1: interrupt enabled) |
| TIMESTAMP_EN | Enables timestamp counter. The counter is readable in TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h). Default value: 0<br>(0: disabled; 1: enabled) |
| DIS_RST_LIR_ALL_INT | When this bit is set to 1, reading the ALL_INT_SRC (1Dh) register does not reset the latched interrupt signals. This can be useful in order to not reset some status flags before reading the corresponding status register. Default value: 0<br>(0: disabled; 1: enabled) |
| INACT_EN_[1:0] | Enables activity/inactivity (sleep) function. Default value: 00<br>(00: stationary/motion-only interrupts generated, accelerometer and gyroscope configuration do not change;<br>01: sets accelerometer to low-power mode 1 with accelerometer ODR selected through the XL_INACT_ODR_[1:0] bits of the INACTIVITY_DUR (54h) register, gyroscope configuration does not change;<br>10: sets accelerometer to low-power mode 1 with accelerometer ODR selected through the XL_INACT_ODR_[1:0] bits of the INACTIVITY_DUR (54h) register, gyroscope in sleep mode;<br>11: sets accelerometer to low-power mode 1 with accelerometer ODR selected through the XL_INACT_ODR_[1:0] bits of the INACTIVITY_DUR (54h) register, gyroscope in power-down mode) |

## 9.50 DEN (51h)

DEN configuration register (R/W)

**Table 138. DEN register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | LVL1_EN | LVL2_EN | DEN_XL_EN | DEN_X | DEN_Y | DEN_Z | DEN_XL_G |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 139. DEN register description**

| | |
|---|---|
| LVL1_EN | Enables DEN data level-sensitive trigger. Refer to Table 140. |
| LVL2_EN | Enables DEN level-sensitive latched. Refer to Table 140. |
| DEN_XL_EN | Extends DEN functionality to accelerometer sensor. Default value: 0<br>(0: disabled; 1: enabled) |
| DEN_X | DEN value stored in LSB of X-axis. Default value: 1<br>(0: DEN not stored in X-axis LSB; 1: DEN stored in X-axis LSB) |
| DEN_Y | DEN value stored in LSB of Y-axis. Default value: 1<br>(0: DEN not stored in Y-axis LSB; 1: DEN stored in Y-axis LSB) |
| DEN_Z | DEN value stored in LSB of Z-axis. Default value: 1<br>(0: DEN not stored in Z-axis LSB; 1: DEN stored in Z-axis LSB) |
| DEN_XL_G | DEN stamping sensor selection. Default value: 0<br>(0: DEN pin info stamped in the gyroscope axis selected by bits DEN_X, DEN_Y, DEN_Z;<br>1: DEN pin info stamped in the accelerometer axis selected by bits DEN_X, DEN_Y, DEN_Z) |

**Table 140. Trigger mode selection**

| LVL1_EN, LVL2_EN | Trigger mode |
|---|---|
| 10 | Level-sensitive trigger mode is selected |
| 11 | Level-sensitive latched mode is selected |

## 9.51 INACTIVITY_DUR (54h)

Activity/inactivity configuration register (R/W)

**Table 141. INACTIVITY_DUR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SLEEP_STATUS_ON_INT | WU_INACT_THS_W_2 | WU_INACT_THS_W_1 | WU_INACT_THS_W_0 | XL_INACT_ODR_1 | XL_INACT_ODR_0 | INACT_DUR_1 | INACT_DUR_0 |

**Table 142. INACTIVITY_DUR register description**

| | |
|---|---|
| SLEEP_STATUS_ON_INT | Activity/inactivity interrupt mode configuration.<br>If the INT1_SLEEP_CHANGE or INT2_SLEEP_CHANGE bit is enabled, drives the sleep status or sleep change on the INT pin. Default value: 0<br>(0: sleep change notification on INT pin;<br>1: sleep status reported on INT pin) |
| WU_INACT_THS_W_[2:0] | Weight of 1 LSB of wake-up (WU_THS) and activity/inactivity (INACT_THS) threshold.<br>(000: 7.8125 mg/LSB (default);<br>001: 15.625 mg/LSB;<br>010: 31.25 mg/LSB;<br>011: 62.5 mg/LSB;<br>100: 125 mg/LSB;<br>101 - 110 - 111: 250 mg/LSB) |
| XL_INACT_ODR_[1:0] | Selects the ODR_XL target during inactivity.<br>(00: 1.875 Hz;<br>01: 15 Hz (default);<br>10: 30 Hz;<br>11: 60 Hz) |
| INACT_DUR_[1:0] | Duration in the transition from stationary to motion (from inactivity to activity).<br>(00: transition to motion (activity) immediately at first overthreshold event (default);<br>01: transition to motion (activity) after two consecutive overthreshold events;<br>10: transition to motion (activity) after three consecutive overthreshold events;<br>11: transition to motion (activity) after four consecutive overthreshold events) |

## 9.52 INACTIVITY_THS (55h)

Activity/inactivity threshold setting register (R/W)

**Table 143. INACTIVITY_THS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | INACT_THS_5 | INACT_THS_4 | INACT_THS_3 | INACT_THS_2 | INACT_THS_1 | INACT_THS_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 144. INACTIVITY_THS register description**

| | |
|---|---|
| INACT_THS_[5:0] | Activity/inactivity threshold. The resolution of the threshold depends on the value of WU_INACT_THS_W_[2:0] in the INACTIVITY_DUR (54h) register. Default value: 000000 |

## 9.53 TAP_CFG0 (56h)

Tap configuration register 0 (R/W)

**Table 145. TAP_CFG0 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | LOW_PASS_ ON_6D | HW_FUNC_MASK _XL_SETTL | SLOPE_ FDS | TAP_X_EN | TAP_Y_EN | TAP_Z_EN | LIR |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 146. TAP_CFG0 register description**

| | |
|---|---|
| LOW_PASS_ON_6D | LPF2 filter on 6D function selection. Refer to Figure 30. Default value: 0<br>(0: ODR/2 low-pass filtered data sent to 6D interrupt function;<br>1: LPF2 output data sent to 6D interrupt function) |
| HW_FUNC_MASK_XL_SETTL | Enables masking the execution trigger of the basic interrupt functions (6D/4D, free-fall, wake-up, tap, activity/inactivity) when accelerometer data are settling. Default value: 0<br>(0: disabled; 1: enabled) |
| SLOPE_FDS | HPF or slope filter selection on wake-up and activity/inactivity functions. Refer to Figure 30. Default value: 0<br>(0: slope filter applied; 1: HPF applied) |
| TAP_X_EN | Enables X direction in tap recognition. Default value: 0<br>(0: X direction disabled; 1: X direction enabled) |
| TAP_Y_EN | Enables Y direction in tap recognition. Default value: 0<br>(0: Y direction disabled; 1: Y direction enabled) |
| TAP_Z_EN | Enables Z direction in tap recognition. Default value: 0<br>(0: Z direction disabled; 1: Z direction enabled) |
| LIR | Latched interrupt. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched) |

## 9.54 TAP_CFG1 (57h)

Tap configuration register 1 (R/W)

**Table 147. TAP_CFG1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TAP_ PRIORITY_2 | TAP_ PRIORITY_1 | TAP_ PRIORITY_0 | TAP_ THS_X_4 | TAP_ THS_X_3 | TAP_ THS_X_2 | TAP_ THS_X_1 | TAP_ THS_X_0 |

**Table 148. TAP_CFG1 register description**

| | |
|---|---|
| TAP_PRIORITY_[2:0] | Selection of axis priority for tap detection (see Table 149) |
| TAP_THS_X_[4:0] | X-axis tap recognition threshold. Default value: 0<br>1 LSB = FS_XL / ($2^5$) |

**Table 149. TAP priority decoding**

| TAP_PRIORITY_[2:0] | Max. priority | Mid. priority | Min. priority |
|---|---|---|---|
| 000 | X | Y | Z |
| 001 | Y | X | Z |
| 010 | X | Z | Y |
| 011 | Z | Y | X |
| 100 | X | Y | Z |
| 101 | Y | Z | X |
| 110 | Z | X | Y |
| 111 | Z | Y | X |

## 9.55 TAP_CFG2 (58h)

Tap configuration register 2 (R/W)

**Table 150. TAP_CFG2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | TAP_ THS_Y_4 | TAP_ THS_Y_3 | TAP_ THS_Y_2 | TAP_ THS_Y_1 | TAP_ THS_Y_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 151. TAP_CFG2 register description**

| | |
|---|---|
| TAP_THS_Y_[4:0] | Y-axis tap recognition threshold. Default value: 0<br>1 LSB = FS_XL / ($2^5$) |

## 9.56 TAP_THS_6D (59h)

Portrait/landscape position and tap function threshold register (R/W)

**Table 152. TAP_THS_6D register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D4D_EN | SIXD_THS_1 | SIXD_THS_0 | TAP_ THS_Z_4 | TAP_ THS_Z_3 | TAP_ THS_Z_2 | TAP_ THS_Z_1 | TAP_ THS_Z_0 |

**Table 153. TAP_THS_6D register description**

| | |
|---|---|
| D4D_EN | Enables 4D orientation detection. Z-axis position detection is disabled. Default value: 0<br>(0: disabled; 1: enabled) |
| SIXD_THS_[1:0] | Threshold for 4D/6D function. Default value: 00<br>For details, refer to Table 154. |
| TAP_THS_Z_[4:0] | Z-axis recognition threshold. Default value: 0<br>1 LSB = FS_XL / ($2^5$) |

**Table 154. Threshold for D4D/D6D function**

| SIXD_THS_[1:0] | Threshold value |
|---|---|
| 00 | 80 degrees |
| 01 | 70 degrees |
| 10 | 60 degrees |
| 11 | 50 degrees |

## 9.57 TAP_DUR (5Ah)

Tap recognition function setting register (R/W)

**Table 155. TAP_DUR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DUR_3 | DUR_2 | DUR_1 | DUR_0 | QUIET_1 | QUIET_0 | SHOCK_1 | SHOCK_0 |

**Table 156. TAP_DUR register description**

| | |
|---|---|
| DUR_[3:0] | Duration of maximum time gap for double-tap recognition. Default: 0000<br>When double-tap recognition is enabled, this register expresses the maximum time between two consecutive detected taps to determine a double-tap event. The default value of these bits is 0000b which corresponds to 16/ODR_XL time. If the DUR_[3:0] bits are set to a different value, 1LSB corresponds to 32/ODR_XL time. |
| QUIET_[1:0] | Expected quiet time after a tap detection. Default value: 00<br>Quiet time is the time after the first detected tap in which there must not be any overthreshold event. The default value of these bits is 00b which corresponds to 2/ODR_XL time. If the QUIET_[1:0] bits are set to a different value, 1LSB corresponds to 4/ODR_XL time. |
| SHOCK_[1:0] | Maximum duration of overthreshold event. Default value: 00<br>Maximum duration is the maximum time of an overthreshold signal detection to be recognized as a tap event. The default value of these bits is 00b which corresponds to 4/ODR_XL time. If the SHOCK_[1:0] bits are set to a different value, 1LSB corresponds to 8/ODR_XL time. |

## 9.58 WAKE_UP_THS (5Bh)

Single/double-tap selection and wake-up configuration (R/W)

**Table 157. WAKE_UP_THS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SINGLE_ DOUBLE_TAP | USR_OFF _ON_WU | WK_THS_5 | WK_THS_4 | WK_THS_3 | WK_THS_2 | WK_THS_1 | WK_THS_0 |

**Table 158. WAKE_UP_THS register description**

| | |
|---|---|
| SINGLE_DOUBLE_TAP | Enables single/double-tap event. Default value: 0<br>(0: only single-tap event enabled;<br>1: both single and double-tap events enabled) |
| USR_OFF_ON_WU | Drives the low-pass filtered data with user offset correction (instead of high-pass filtered data) to the wake-up and the activity/inactivity functions. Refer to Figure 30. Default value: 0 |
| WK_THS_[5:0] | Wake-up threshold. The resolution of the threshold depends on the value of WU_INACT_THS_W_[2:0] in the INACTIVITY_DUR (54h) register. Default value: 000000 |

## 9.59 WAKE_UP_DUR (5Ch)

Free-fall, wake-up, and sleep mode functions duration setting register (R/W)

**Table 159. WAKE_UP_DUR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FF_DUR_5 | WAKE_DUR_1 | WAKE_DUR_0 | 0(1) | SLEEP_DUR_3 | SLEEP_DUR_2 | SLEEP_DUR_1 | SLEEP_DUR_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 160. WAKE_UP_DUR register description**

| | |
|---|---|
| FF_DUR_5 | Free-fall duration event. Default: 0<br>For the complete configuration of the free-fall duration, refer to FF_DUR_[4:0] in the FREE_FALL (5Dh) configuration.<br>1 LSB = 1/ODR_XL time |
| WAKE_DUR_[1:0] | Wake-up duration event. Default: 00<br>1 LSB = 1/ODR_XL time |
| SLEEP_DUR_[3:0] | Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR)<br>1 LSB = 512/ODR_XL time |

## 9.60 FREE_FALL (5Dh)

Free-fall function duration setting register (R/W)

**Table 161. FREE_FALL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FF_DUR_4 | FF_DUR_3 | FF_DUR_2 | FF_DUR_1 | FF_DUR_0 | FF_THS_2 | FF_THS_1 | FF_THS_0 |

**Table 162. FREE_FALL register description**

| | |
|---|---|
| FF_DUR_[4:0] | Free-fall duration event. Default: 0<br>For the complete configuration of the free-fall duration, refer to FF_DUR_5 in the WAKE_UP_DUR (5Ch) configuration. |
| FF_THS_[2:0] | Free-fall threshold setting. Default: 000<br>For details refer to Table 163. |

**Table 163. Threshold for free-fall function**

| FF_THS_[2:0] | Threshold value |
|---|---|
| 000 | 156 mg |
| 001 | 219 mg |
| 010 | 250 mg |
| 011 | 312 mg |
| 100 | 344 mg |
| 101 | 406 mg |
| 110 | 469 mg |
| 111 | 500 mg |

## 9.61 MD1_CFG (5Eh)

Functions routing to INT1 pin register (R/W). Each bit in this register enables a signal to be carried over the INT1 pin. The output of the pin is the OR combination of the signals selected here and in the INT1_CTRL (0Dh) register.

**Table 164. MD1_CFG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT1_SLEEP_CHANGE | INT1_SINGLE_TAP | INT1_WU | INT1_FF | INT1_DOUBLE_TAP | INT1_6D | INT1_EMB_FUNC | INT1_SHUB |

**Table 165. MD1_CFG register description**

| | |
|---|---|
| INT1_SLEEP_CHANGE(1) | Routing activity/inactivity recognition event to INT1. Default: 0<br>(0: routing activity/inactivity event to INT1 disabled;<br>1: routing activity/inactivity event to INT1 enabled) |
| INT1_SINGLE_TAP | Routing single-tap recognition event to INT1. Default: 0<br>(0: routing single-tap event to INT1 disabled;<br>1: routing single-tap event to INT1 enabled) |
| INT1_WU | Routing wake-up event to INT1. Default value: 0<br>(0: routing wake-up event to INT1 disabled;<br>1: routing wake-up event to INT1 enabled) |
| INT1_FF | Routing free-fall event to INT1. Default value: 0<br>(0: routing free-fall event to INT1 disabled;<br>1: routing free-fall event to INT1 enabled) |
| INT1_DOUBLE_TAP | Routing tap event to INT1. Default value: 0<br>(0: routing double-tap event to INT1 disabled;<br>1: routing double-tap event to INT1 enabled) |
| INT1_6D | Routing 6D event to INT1. Default value: 0<br>(0: routing 6D event to INT1 disabled;<br>1: routing 6D event to INT1 enabled) |
| INT1_EMB_FUNC | Routing embedded functions event to INT1. Default value: 0<br>(0: routing embedded functions event to INT1 disabled;<br>1: routing embedded functions event to INT1 enabled) |
| INT1_SHUB | Routing sensor hub communication concluded event to INT1. Default value: 0<br>(0: routing sensor hub communication concluded event to INT1 disabled;<br>1: routing sensor hub communication concluded event to INT1 enabled) |

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the INACTIVITY_DUR (54h) register.*

## 9.62 MD2_CFG (5Fh)

Functions routing to INT2 pin register (R/W). Each bit in this register enables a signal to be carried over the INT2 pin. The output of the pin is the OR combination of the signals selected here and in the INT2_CTRL (0Eh) register.

**Table 166. MD2_CFG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_SLEEP_CHANGE | INT2_SINGLE_TAP | INT2_WU | INT2_FF | INT2_DOUBLE_TAP | INT2_6D | INT2_EMB_FUNC | INT2_TIMESTAMP |

**Table 167. MD2_CFG register description**

| | |
|---|---|
| INT2_SLEEP_CHANGE[1] | Routing activity/inactivity recognition event to INT2. Default: 0<br>(0: routing activity/inactivity event to INT2 disabled;<br>1: routing activity/inactivity event to INT2 enabled) |
| INT2_SINGLE_TAP | Single-tap recognition routing to INT2. Default: 0<br>(0: routing single-tap event to INT2 disabled;<br>1: routing single-tap event to INT2 enabled) |
| INT2_WU | Routing wake-up event to INT2. Default value: 0<br>(0: routing wake-up event to INT2 disabled;<br>1: routing wake-up event to INT2 enabled) |
| INT2_FF | Routing free-fall event to INT2. Default value: 0<br>(0: routing free-fall event to INT2 disabled;<br>1: routing free-fall event to INT2 enabled) |
| INT2_DOUBLE_TAP | Routing tap event to INT2. Default value: 0<br>(0: routing double-tap event to INT2 disabled;<br>1: routing double-tap event to INT2 enabled) |
| INT2_6D | Routing 6D event to INT2. Default value: 0<br>(0: routing 6D event to INT2 disabled;<br>1: routing 6D event to INT2 enabled) |
| INT2_EMB_FUNC | Routing embedded functions event to INT2. Default value: 0<br>(0: routing embedded functions event to INT2 disabled;<br>1: routing embedded functions event to INT2 enabled) |
| INT2_TIMESTAMP | Enables routing the alert for timestamp overflow within 5.6 ms to the INT2 pin. |

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the INACTIVITY_DUR (54h) register.*

## 9.63 EMB_FUNC_CFG (63h)

Embedded functions configuration register (R/W)

**Table 168. EMB_FUNC_CFG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | EMB_FUNC_IRQ_MASK_G_SETTL | EMB_FUNC_IRQ_MASK_XL_SETTL | EMB_FUNC_DISABLE | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 169. EMB_FUNC_CFG register description**

| | |
|---|---|
| EMB_FUNC_IRQ_MASK_G_SETTL | Enables / masks execution trigger of the embedded functions when gyroscope data are settling. Default value: 0<br>(0: disabled;<br>1: masks execution trigger of the embedded functions until gyroscope filter settling ends) |
| EMB_FUNC_IRQ_MASK_XL_SETTL | Enables / masks execution trigger of the embedded functions when accelerometer data are settling. Default value: 0<br>(0: disabled;<br>1: masks execution trigger of the embedded functions until accelerometer filter settling ends) |
| EMB_FUNC_DISABLE | Disables execution of the embedded functions. Default value: 0<br>(0: disabled;<br>1: embedded functions execution trigger is not generated anymore and all initialization procedures are forced when this bit is set back to 0). |

## 9.64 UI_HANDSHAKE_CTRL (64h)

Control register (UI side) for UI / SPI2 shared registers (R/W)

**Table 170. UI_HANDSHAKE_CTRL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | UI_SHARED_ACK | UI_SHARED_REQ |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 171. UI_HANDSHAKE_CTRL register description**

| | |
|---|---|
| UI_SHARED_ACK | Primary interface side. This bit acknowledges the handshake. If the secondary interface is not accessing the shared registers, this bit is set to 1 by the device and the R/W operation on the UI_SPI2_SHARED_0 (65h) through UI_SPI2_SHARED_5 (6Ah) registers is allowed on the primary interface. |
| UI_SHARED_REQ | This bit is used by the primary interface master to request access to the UI_SPI2_SHARED_0 (65h) through UI_SPI2_SHARED_5 (6Ah) registers. When the R/W operation is finished, the master must reset this bit. |

## 9.65 UI_SPI2_SHARED_0 (65h)

UI / SPI2 shared register 0 (R/W)

**Table 172. UI_SPI2_SHARED_0 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 173. UI_SPI2_SHARED_0 register description**

| | |
|---|---|
| D[7:0] | Volatile byte is used as a contact point between the primary and secondary interface host. These shared registers are accessible only by one interface at a time and access is managed through the UI_SHARED_ACK and UI_SHARED_REQ bits of register UI_HANDSHAKE_CTRL (64h) and the SPI2_SHARED_ACK and SPI2_SHARED_REQ bits of register SPI2_HANDSHAKE_CTRL (6Eh). |

## 9.66 UI_SPI2_SHARED_1 (66h)

UI / SPI2 shared register 1 (R/W)

**Table 174. UI_SPI2_SHARED_1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 175. UI_SPI2_SHARED_1 register description**

| | |
|---|---|
| D[7:0] | Volatile byte is used as a contact point between the primary and secondary interface host. These shared registers are accessible only by one interface at a time and access is managed through the UI_SHARED_ACK and UI_SHARED_REQ bits of register UI_HANDSHAKE_CTRL (64h) and the SPI2_SHARED_ACK and SPI2_SHARED_REQ bits of register SPI2_HANDSHAKE_CTRL (6Eh). |

## 9.67 UI_SPI2_SHARED_2 (67h)

UI / SPI2 shared register 2 (R/W)

**Table 176. UI_SPI2_SHARED_2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 177. UI_SPI2_SHARED_2 register description**

| | |
|---|---|
| D[7:0] | Volatile byte is used as a contact point between the primary and secondary interface host. These shared registers are accessible only by one interface at a time and access is managed through the UI_SHARED_ACK and UI_SHARED_REQ bits of register UI_HANDSHAKE_CTRL (64h) and the SPI2_SHARED_ACK and SPI2_SHARED_REQ bits of register SPI2_HANDSHAKE_CTRL (6Eh). |

## 9.68 UI_SPI2_SHARED_3 (68h)

UI / SPI2 shared register 3 (R/W)

**Table 178. UI_SPI2_SHARED_3 register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

**Table 179. UI_SPI2_SHARED_3 register description**

| | |
|---|---|
| D[7:0] | Volatile byte is used as a contact point between the primary and secondary interface host. These shared registers are accessible only by one interface at a time and access is managed through the UI_SHARED_ACK and UI_SHARED_REQ bits of register UI_HANDSHAKE_CTRL (64h) and the SPI2_SHARED_ACK and SPI2_SHARED_REQ bits of register SPI2_HANDSHAKE_CTRL (6Eh). |

## 9.69 UI_SPI2_SHARED_4 (69h)

UI / SPI2 shared register 4 (R/W)

**Table 180. UI_SPI2_SHARED_4 register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

**Table 181. UI_SPI2_SHARED_4 register description**

| | |
|---|---|
| D[7:0] | Volatile byte is used as a contact point between the primary and secondary interface host. These shared registers are accessible only by one interface at a time and access is managed through the UI_SHARED_ACK and UI_SHARED_REQ bits of register UI_HANDSHAKE_CTRL (64h) and the SPI2_SHARED_ACK and SPI2_SHARED_REQ bits of register SPI2_HANDSHAKE_CTRL (6Eh). |

## 9.70 UI_SPI2_SHARED_5 (6Ah)

UI / SPI2 shared register 5 (R/W)

**Table 182. UI_SPI2_SHARED_5 register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

**Table 183. UI_SPI2_SHARED_5 register description**

| | |
|---|---|
| D[7:0] | Volatile byte is used as a contact point between the primary and secondary interface host. These shared registers are accessible only by one interface at a time and access is managed through the UI_SHARED_ACK and UI_SHARED_REQ bits of register UI_HANDSHAKE_CTRL (64h) and the SPI2_SHARED_ACK and SPI2_SHARED_REQ bits of register SPI2_HANDSHAKE_CTRL (6Eh). |

## 9.71 CTRL_EIS (6Bh)

Gyroscope EIS channel control register (R/W)

**Table 184. CTRL_EIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ODR_G_EIS_1 | ODR_G_EIS_0 | 0(1) | LPF_G_EIS_BW | G_EIS_ON_G_OIS_OUT_REG | FS_G_EIS_2 | FS_G_EIS_1 | FS_G_EIS_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 185. CTRL_EIS register description**

| | |
|---|---|
| ODR_G_EIS_[1:0] | Enables and selects the ODR of the gyroscope EIS channel.<br>(00: EIS channel is off (default);<br>01: 1.92 kHz;<br>10: 960 Hz;<br>11: reserved) |
| LPF_G_EIS_BW | Gyroscope digital LPF_EIS filter bandwidth selection. Refer to Table 186. |
| G_EIS_ON_G_OIS_OUT_REG | Enables routing gyroscope EIS output to OIS from UI output addresses (2Eh – 33h). When this bit is set to 1, the gyroscope OIS data cannot be read from primary interface. Default value: 0<br>(0: disabled; 1: enabled) |
| FS_G_EIS_[2:0] | Gyroscope full-scale selection for EIS channel. If the FS_G_[3:0] bits in CTRL6 (15h) are equal to 1100 (±4000 dps), FS_G_EIS_[2:0] must be set to “100” in order to have ±4000 dps full scale on both UI and EIS channels. If the FS_G_3 bit in register CTRL6 (15h) is equal to 0, the EIS channel full scale can be selected as follows:<br>(000: ±125 dps (default);<br>001: ±250 dps;<br>010: ±500 dps;<br>011: ±1000 dps;<br>100: ±2000 dps;<br>101: reserved;<br>110: reserved;<br>111: reserved) |

**Table 186. Gyroscope EIS chain digital LPF_EIS filter bandwidth selection**

| ODR_G_EIS_[1:0] | Gyroscope EIS ODR [Hz] | LPF_G_EIS_BW | Cutoff [Hz] | Phase @ 20 Hz [°] |
|---|---|---|---|---|
| 01 | 1.92 kHz | 0 | 153 Hz | -13.5° |
| | | 1 | 203 Hz | -10.8° |
| 10 | 960 | 0 | 148 Hz | -15.4° |
| | | 1 | 193 Hz | -12.7° |

## 9.72 UI_INT_OIS (6Fh)

OIS interrupt configuration register

The primary interface can write to this register when the OIS_CTRL_FROM_UI bit in the FUNC_CFG_ACCESS (01h) register is equal to 1 (primary IF full control mode); this register is read-only when the OIS_CTRL_FROM_UI bit is equal to 0 (SPI2 full control mode) and shows the content of the SPI2_INT_OIS (6Fh) register.

**Table 187. UI_INT_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_ DRDY_OIS | DRDY_ MASK_OIS | 0(1) | ST_OIS_ CLAMPDIS | 0(1) | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 188. UI_INT_OIS register description**

| | |
|---|---|
| INT2_DRDY_OIS | Enables OIS chain DRDY on INT2 pin from the UI interface. This setting has priority over all other INT2 settings. |
| DRDY_MASK_OIS | Enables / masks OIS data available. Default value: 0<br>(0: disabled;<br>1: masks OIS DRDY on pin (both accelerometer and gyroscope) until filter settling ends (accelerometer and gyroscope independently masked)) |
| ST_OIS_CLAMPDIS | Disables OIS chain clamp during self-test. Default value: 0<br>(0: All OIS chain outputs = 8000h during self-test;<br>1: OIS chain self-test outputs) |

## 9.73 UI_CTRL1_OIS (70h)

OIS configuration register

The primary interface can write this register when the OIS_CTRL_FROM_UI bit in the FUNC_CFG_ACCESS (01h) register is equal to 1 (primary IF full control mode); this register is read-only when the OIS_CTRL_FROM_UI bit is equal to 0 (SPI2 full control mode) and shows the content of the SPI2_CTRL1_OIS (70h) register.

**Table 189. UI_CTRL1_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | SIM_OIS | 0(1) | 0(1) | OIS_ XL_EN | OIS_ G_EN | SPI2_READ _EN |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 190. UI_CTRL1_OIS register description**

| | |
|---|---|
| SIM_OIS | SPI2 3- or 4-wire interface. Default value: 0<br>(0: 4-wire SPI2;<br>1: 3-wire SPI2) |
| OIS_XL_EN | Enables accelerometer OIS chain. Default value: 0<br>(0: accelerometer OIS chain disabled;<br>1: accelerometer OIS chain enabled) |
| OIS_G_EN | Enables gyroscope OIS chain. Default value: 0<br>(0: gyroscope OIS chain disabled;<br>1: gyroscope OIS chain enabled) |
| SPI2_READ_EN | In primary IF full control mode, enables auxiliary SPI for reading OIS data in registers SPI2_OUTX_L_G_OIS (22h) and SPI2_OUTX_H_G_OIS (23h) through Section 11.9 SPI2_OUTZ_L_A_OIS (2Ch) and SPI2_OUTZ_H_A_OIS (2Dh). Default value: 0<br>(0: OIS data read from auxiliary SPI disabled;<br>1: OIS data read from auxiliary SPI enabled) |

## 9.74 UI_CTRL2_OIS (71h)

OIS configuration register

The primary interface can write this register when the OIS_CTRL_FROM_UI bit in the FUNC_CFG_ACCESS (01h) register is equal to 1 (primary IF full control mode); this register is read-only when the OIS_CTRL_FROM_UI bit is equal to 0 (SPI2 full control mode) and shows the content of the SPI2_CTRL2_OIS (71h) register.

**Table 191. UI_CTRL2_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | LPF1_G_ OIS_BW_1 | LPF1_G_ OIS_BW_0 | FS_G _OIS_2 | FS_G _OIS_1 | FS_G _OIS_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 192. UI_CTRL2_OIS register description**

| | |
|---|---|
| LPF1_G_OIS_BW_[1:0] | Gyroscope OIS digital LPF1 filter bandwidth selection. Refer to Table 193. |
| FS_G_OIS_[2:0] | Gyroscope OIS full-scale selection:<br>(000: ±125 dps;<br>001: ±250 dps;<br>010: ±500 dps;<br>011: ±1000 dps;<br>100: ±2000 dps;<br>101: reserved;<br>110: reserved;<br>111: reserved) |

**Table 193. Gyroscope OIS chain digital LPF1 filter bandwidth selection**

| LPF1_G_OIS_BW_[1:0] | Cutoff [Hz] | Phase @ 20 Hz [°] |
|---|---|---|
| 00 | 293 Hz | -7.1° |
| 01 | 217 Hz | -9.1° |
| 10 | 158 Hz | -11.9° |
| 11 | 476 Hz | -5.1° |

## 9.75 UI_CTRL3_OIS (72h)

OIS configuration register

The primary interface can write this register when the OIS_CTRL_FROM_UI bit in the FUNC_CFG_ACCESS (01h) register is equal to 1 (primary IF full control mode); this register is read-only when the OIS_CTRL_FROM_UI bit is equal to 0 (SPI2 full control mode) and shows the content of the SPI2_CTRL3_OIS (72h) register.

**Table 194. UI_CTRL3_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | LPF_XL_ OIS_BW_2 | LPF_XL_ OIS_BW_1 | LPF_XL_ OIS_BW_0 | 0(1) | FS_XL _OIS_1 | FS_XL _OIS_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 195. UI_CTRL3_OIS register description**

| | |
|---|---|
| LPF_XL_OIS_BW_[2:0] | Selects accelerometer OIS channel bandwidth, see Table 196. Default value: 0 |
| FS_XL_OIS_[1:0] | Selects accelerometer OIS channel full-scale:<br>(00: ±2 *g* (default);<br>01: ±4 *g*;<br>10: ±8 *g*;<br>11: ±16 *g*) |

*Note: When the accelerometer full-scale value is selected only from the UI side it is readable also from the OIS side.*

**Table 196. Accelerometer OIS channel bandwidth and phase**

| LPF_XL_OIS_BW_[2:0] | Typ. overall bandwidth [Hz] | Typ. overall phase [°] |
|---|---|---|
| 000 | 749 Hz | -3.41 deg @ 20 Hz |
| 001 | 539 Hz | -4.04 deg@ 20 Hz |
| 010 | 342 Hz | -5.31 deg@ 20 Hz |
| 011 | 162 Hz | -9.08 deg@ 20 Hz |
| 100 | 78.5 Hz | -16.4 deg @ 20 Hz |
| 101 | 38.6 Hz | -29.6 deg@ 20 Hz |
| 110 | 19.3 Hz | -28.8 deg @ 10 Hz |
| 111 | 9.8 Hz | -29.1 deg @ 5 Hz |

## 9.76 X_OFS_USR (73h)

Accelerometer X-axis user offset correction (R/W). The offset value set in the X_OFS_USR offset register is internally subtracted from the acceleration value measured on the X-axis.

**Table 197. X_OFS_USR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X_OFS_USR_7 | X_OFS_USR_6 | X_OFS_USR_5 | X_OFS_USR_4 | X_OFS_USR_3 | X_OFS_USR_2 | X_OFS_USR_1 | X_OFS_USR_0 |

**Table 198. X_OFS_USR register description**

| | |
|---|---|
| X_OFS_USR_[7:0] | Accelerometer X-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL9 (18h). The offset can be applied to the output registers (see USR_OFF_ON_OUT bit in the CTRL9 (18h) register) or to the wake-up function input data (see USR_OFF_ON_WU bit in the WAKE_UP_THS (5Bh) register).<br>The value must be in the range [-127 127]. |

## 9.77 Y_OFS_USR (74h)

Accelerometer Y-axis user offset correction (R/W). The offset value set in the Y_OFS_USR offset register is internally subtracted from the acceleration value measured on the Y-axis.

**Table 199. Y_OFS_USR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Y_OFS_USR_7 | Y_OFS_USR_6 | Y_OFS_USR_5 | Y_OFS_USR_4 | Y_OFS_USR_3 | Y_OFS_USR_2 | Y_OFS_USR_1 | Y_OFS_USR_0 |

**Table 200. Y_OFS_USR register description**

| | |
|---|---|
| Y_OFS_USR_[7:0] | Accelerometer Y-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL9 (18h). The offset can be applied to the output registers (see USR_OFF_ON_OUT bit in the CTRL9 (18h) register) or to the wake-up function input data (see USR_OFF_ON_WU bit in the WAKE_UP_THS (5Bh) register).<br>The value must be in the range [-127 127]. |

## 9.78 Z_OFS_USR (75h)

Accelerometer Z-axis user offset correction (R/W). The offset value set in the Z_OFS_USR offset register is internally subtracted from the acceleration value measured on the Z-axis.

**Table 201. Z_OFS_USR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Z_OFS_USR_7 | Z_OFS_USR_6 | Z_OFS_USR_5 | Z_OFS_USR_4 | Z_OFS_USR_3 | Z_OFS_USR_2 | Z_OFS_USR_1 | Z_OFS_USR_0 |

**Table 202. Z_OFS_USR register description**

| | |
|---|---|
| Z_OFS_USR_[7:0] | Accelerometer Z-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL9 (18h). The offset can be applied to the output registers (see USR_OFF_ON_OUT bit in the CTRL9 (18h) register) or to the wake-up function input data (see USR_OFF_ON_WU bit in the WAKE_UP_THS (5Bh) register).<br>The value must be in the range [-127 127]. |

## 9.79 FIFO_DATA_OUT_TAG (78h)

FIFO tag register (R)

**Table 203. FIFO_DATA_OUT_TAG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TAG_ SENSOR_4 | TAG_ SENSOR_3 | TAG_ SENSOR_2 | TAG_ SENSOR_1 | TAG_ SENSOR_0 | TAG_CNT_1 | TAG_CNT_0 | - |

**Table 204. FIFO_DATA_OUT_TAG register description**

| | |
|---|---|
| TAG_SENSOR_[4:0] | FIFO tag. Identifies the sensor in:<br>FIFO_DATA_OUT_X_L (79h) and FIFO_DATA_OUT_X_H (7Ah), FIFO_DATA_OUT_Y_L (7Bh) and FIFO_DATA_OUT_Y_H (7Ch), and FIFO_DATA_OUT_Z_L (7Dh) and FIFO_DATA_OUT_Z_H (7Eh)<br>For details, refer to Table 205. |
| TAG_CNT_[1:0] | 2-bit counter which identifies sensor time slot |

**Table 205. FIFO tag**

| TAG_SENSOR_[4:0] | Sensor name |
|---|---|
| 0x00 | FIFO empty |
| 0x01 | Gyroscope NC |
| 0x02 | Accelerometer NC |
| 0x03 | Temperature |
| 0x04 | Timestamp |
| 0x05 | CFG_Change |
| 0x06 | Accelerometer NC_T_2 |
| 0x07 | Accelerometer NC_T_1 |
| 0x08 | Accelerometer 2xC |
| 0x09 | Accelerometer 3xC |
| 0x0A | Gyroscope NC_T_2 |
| 0x0B | Gyroscope NC_T_1 |
| 0x0C | Gyroscope 2xC |
| 0x0D | Gyroscope 3xC |
| 0x0E | Sensor hub slave 0 |
| 0x0F | Sensor hub slave 1 |
| 0x10 | Sensor hub slave 2 |
| 0x11 | Sensor hub slave 3 |
| 0x12 | Step counter |
| 0x19 | Sensor hub nack |
| 0x1D | Accelerometer dualC |
| 0x1E | Enhanced EIS gyroscope |

## 9.80 FIFO_DATA_OUT_X_L (79h) and FIFO_DATA_OUT_X_H (7Ah)

FIFO data output X (R)

**Table 206. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L registers**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 207. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L register description**

| | |
|---|---|
| D[15:0] | FIFO X-axis output |

## 9.81 FIFO_DATA_OUT_Y_L (7Bh) and FIFO_DATA_OUT_Y_H (7Ch)

FIFO data output Y (R)

**Table 208. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L registers**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 209. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L register description**

| | |
|---|---|
| D[15:0] | FIFO Y-axis output |

## 9.82 FIFO_DATA_OUT_Z_L (7Dh) and FIFO_DATA_OUT_Z_H (7Eh)

FIFO data output Z (R)

**Table 210. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L registers**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 211. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L register description**

| | |
|---|---|
| D[15:0] | FIFO Z-axis output |

# 10 SPI2 register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

All these registers are accessible from auxiliary SPI interface only.

**Table 212. SPI2 register address map**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| SPI2_WHO_AM_I | R | 0F | 00001111 | 01110000 | |
| SPI2_STATUS_REG_OIS | R | 1E | 00011110 | output | |
| SPI2_OUT_TEMP_L | R | 20 | 00100000 | output | |
| SPI2_OUT_TEMP_H | R | 21 | 00100001 | output | |
| SPI2_OUTX_L_G_OIS | R | 22 | 00100010 | output | |
| SPI2_OUTX_H_G_OIS | R | 23 | 00100011 | output | |
| SPI2_OUTY_L_G_OIS | R | 24 | 00100100 | output | |
| SPI2_OUTY_H_G_OIS | R | 25 | 00100101 | output | |
| SPI2_OUTZ_L_G_OIS | R | 26 | 00100110 | output | |
| SPI2_OUTZ_H_G_OIS | R | 27 | 00100111 | output | |
| SPI2_OUTX_L_A_OIS | R | 28 | 00101000 | output | |
| SPI2_OUTX_H_A_OIS | R | 29 | 00101001 | output | |
| SPI2_OUTY_L_A_OIS | R | 2A | 00101010 | output | |
| SPI2_OUTY_H_A_OIS | R | 2B | 00101011 | output | |
| SPI2_OUTZ_L_A_OIS | R | 2C | 00101100 | output | |
| SPI2_OUTZ_H_A_OIS | R | 2D | 00101101 | output | |
| SPI2_HANDSHAKE_CTRL | R/W | 6E | 01101110 | 00000000 | |
| SPI2_INT_OIS | R/W (SPI2 full-control mode)<br>R (primary IF full-control mode) | 6F | 01101111 | 00000000 | |
| SPI2_CTRL1_OIS | R/W (SPI2 full-control mode)<br>R (primary IF full-control mode) | 70 | 01110000 | 00000000 | |
| SPI2_CTRL2_OIS | R/W (SPI2 full-control mode)<br>R (primary IF full-control mode) | 71 | 01110001 | 00000000 | |
| SPI2_CTRL3_OIS | R/W (SPI2 full-control mode)<br>R (primary IF full-control mode) | 72 | 01110010 | 00000000 | |

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

# 11 SPI2 register description

## 11.1 SPI2_WHO_AM_I (0Fh)

WHO_AM_I register (R). This is a read-only register. Its value is fixed at 70h.

**Table 213. SPI2_WhoAmI register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

## 11.2 SPI2_STATUS_REG_OIS (1Eh)

The SPI2_STATUS_REG_OIS register is read by the auxiliary SPI (R).

**Table 214. SPI2_STATUS_REG_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | GYRO_ SETTLING | GDA | XLDA |

**Table 215. SPI2_STATUS_REG_OIS description**

| | |
|---|---|
| GYRO_SETTLING | High when the gyroscope output is in the settling phase |
| GDA | Gyroscope data available (reset when one of the high parts of the output data is read) |
| XLDA | Accelerometer data available (reset when one of the high parts of the output data is read) |

## 11.3 SPI2_OUT_TEMP_L (20h) and SPI2_OUT_TEMP_H (21h)

Temperature data output register (R). L and H registers together express a 16-bit word in two's complement.

**Table 216. SPI2_OUT_TEMP_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Temp7 | Temp6 | Temp5 | Temp4 | Temp3 | Temp2 | Temp1 | Temp0 |

**Table 217. SPI2_OUT_TEMP_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Temp15 | Temp14 | Temp13 | Temp12 | Temp11 | Temp10 | Temp9 | Temp8 |

**Table 218. SPI2_OUT_TEMP register description**

| | |
|---|---|
| Temp[15:0] | Temperature sensor output data<br>The value is expressed as two's complement sign extended on the MSB. |

## 11.4 SPI2_OUTX_L_G_OIS (22h) and SPI2_OUTX_H_G_OIS (23h)

Angular rate sensor pitch axis (X) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the gyroscope full-scale and ODR (7.68 kHz) settings of the OIS gyroscope.

**Table 219. SPI2_OUTX_L_G_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 220. SPI2_OUTX_H_G_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 221. SPI2_OUTX_H_G_OIS register description**

| | |
|---|---|
| D[15:0] | Gyroscope OIS chain pitch axis (X) angular rate output value |

## 11.5 SPI2_OUTY_L_G_OIS (24h) and SPI2_OUTY_H_G_OIS (25h)

Angular rate sensor roll axis (Y) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the gyroscope full-scale and ODR (7.68 kHz) settings of the OIS gyroscope.

**Table 222. SPI2_OUTY_L_G_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 223. SPI2_OUTY_H_G_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 224. SPI2_OUTY_H_G_OIS register description**

| | |
|---|---|
| D[15:0] | Gyroscope OIS chain roll axis (Y) angular rate output value |

## 11.6 SPI2_OUTZ_L_G_OIS (26h) and SPI2_OUTZ_H_G_OIS (27h)

Angular rate sensor yaw axis (Z) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the gyroscope full-scale and ODR (7.68 kHz) settings of the OIS gyroscope.

**Table 225. SPI2_OUTZ_L_G_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 226. SPI2_OUTZ_H_G_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 227. SPI2_OUTZ_H_G_OIS register description**

| | |
|---|---|
| D[15:0] | Gyroscope OIS chain yaw axis (Z) angular rate output value |

## 11.7 SPI2_OUTX_L_A_OIS (28h) and SPI2_OUTX_H_A_OIS (29h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the accelerometer full scale and ODR (7.68 kHz) settings of the OIS accelerometer.

**Table 228. SPI2_OUTX_L_A_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 229. SPI2_OUTX_H_A_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 230. SPI2_OUTX_H_A_OIS register description**

| | |
|---|---|
| D[15:0] | Accelerometer OIS chain X-axis linear acceleration output value |

## 11.8 SPI2_OUTY_L_A_OIS (2Ah) and SPI2_OUTY_H_A_OIS (2Bh)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the accelerometer full scale and ODR (7.68 kHz) settings of the OIS accelerometer.

**Table 231. SPI2_OUTY_L_A_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 232. SPI2_OUTY_H_A_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 233. SPI2_OUTY_H_A_OIS register description**

| | |
|---|---|
| D[15:0] | Accelerometer OIS chain Y-axis linear acceleration output value |

## 11.9 SPI2_OUTZ_L_A_OIS (2Ch) and SPI2_OUTZ_H_A_OIS (2Dh)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the accelerometer full scale and ODR (7.68 kHz) settings of the OIS accelerometer.

**Table 234. SPI2_OUTZ_L_A_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 235. SPI2_OUTZ_H_A_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

**Table 236. SPI2_OUTZ_H_A_OIS register description**

| | |
|---|---|
| D[15:0] | Accelerometer OIS chain Z-axis linear acceleration output value |

## 11.10 SPI2_HANDSHAKE_CTRL (6Eh)

Control register (SPI2 side) for UI / SPI2 shared registers (R/W)

**Table 237. SPI2_HANDSHAKE_CTRL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | SPI2_ SHARED_REQ | SPI2_ SHARED_ACK |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 238. SPI2_HANDSHAKE_CTRL register description**

| | |
|---|---|
| SPI2_SHARED_REQ | This bit is used by the auxiliary SPI (SPI2) interface master to request access to the UI_SPI2_SHARED_0 (65h) through UI_SPI2_SHARED_5 (6Ah) registers. When the R/W operation is finished, the master must reset this bit. |
| SPI2_SHARED_ACK | Auxiliary SPI (SPI2) interface side. This bit acknowledges the handshake. If the primary interface is not accessing the shared registers, this bit is set to 1 by the device and the R/W operation on the UI_SPI2_SHARED_0 (65h) through UI_SPI2_SHARED_5 (6Ah) registers is allowed on the auxiliary SPI interface. |

## 11.11 SPI2_INT_OIS (6Fh)

OIS interrupt configuration register and self-test setting

The auxiliary SPI interface can write this register when the OIS_CTRL_FROM_UI bit in the FUNC_CFG_ACCESS (01h) register is equal to 0 (SPI2 full control mode); this register is read-only when the OIS_CTRL_FROM_UI bit is equal to 1 (primary IF full control mode) and shows the content of the UI_INT_OIS (6Fh) register.

**Table 239. SPI2_INT_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_ DRDY_OIS | DRDY_MASK _OIS | 0(1) | ST_OIS_ CLAMPDIS | ST_G_ OIS_1 | ST_G_ OIS_0 | ST_XL_ OIS_1 | ST_XL_ OIS_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 240. SPI2_INT_OIS register description**

| | |
|---|---|
| INT2_DRDY_OIS | Enables OIS chain DRDY on INT2 pin. This setting has priority over all other INT2 settings. |
| DRDY_MASK_OIS | Enables / masks OIS data available. Default value: 0<br>(0: disabled;<br>1: masks OIS DRDY on pin (both accelerometer and gyroscope) until filter settling ends (accelerometer and gyroscope independently masked)) |
| ST_OIS_CLAMPDIS | Disables OIS chain clamp during self-test. Default value: 0<br>(0: All OIS chain outputs = 8000h during self-test;<br>1: OIS chain self-test outputs) |
| ST_G_OIS_[1:0] | Gyroscope OIS chain self-test selection when the self-test is enabled and ST_OIS_CLAMPDIS = 0.<br>(00: normal mode (default);<br>01: positive sign self-test;<br>10: normal mode;<br>11: negative sign self-test) |
| ST_XL_OIS_[1:0] | Accelerometer OIS chain self-test selection; activated only if the accelerometer OIS chain is enabled.<br>(00: normal mode (default);<br>01: positive sign self-test;<br>10: negative sign self-test;<br>11: reserved) |

## 11.12 SPI2_CTRL1_OIS (70h)

OIS configuration register

The auxiliary SPI interface can write this register when the OIS_CTRL_FROM_UI bit in the FUNC_CFG_ACCESS (01h) register is equal to 0 (SPI2 full control mode); this register is read-only when the OIS_CTRL_FROM_UI bit is equal to 1 (primary IF full control mode) and shows the content of the UI_CTRL1_OIS (70h) register.

**Table 241. SPI2_CTRL1_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | SIM_OIS | 0(1) | 0(1) | OIS_ XL_EN | OIS_ G_EN | SPI2_READ _EN |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 242. SPI2_CTRL1_OIS register description**

| | |
|---|---|
| SIM_OIS | SPI2 3- or 4-wire interface. Default value: 0<br>(0: 4-wire SPI2;<br>1: 3-wire SPI2) |
| OIS_XL_EN | Enables accelerometer OIS chain. Default value: 0<br>(0: accelerometer OIS chain disabled;<br>1: accelerometer OIS chain enabled) |
| OIS_G_EN | Enables gyroscope OIS chain. Default value: 0<br>(0: gyroscope OIS chain disabled;<br>1: gyroscope OIS chain enabled) |
| SPI2_READ_EN | In auxiliary SPI full control mode, enables auxiliary SPI for reading OIS data in registers SPI2_OUTX_L_G_OIS (22h) and SPI2_OUTX_H_G_OIS (23h) through Section 11.9 SPI2_OUTZ_L_A_OIS (2Ch) and SPI2_OUTZ_H_A_OIS (2Dh). Default value: 0<br>(0: OIS data read from auxiliary SPI disabled;<br>1: OIS data read from auxiliary SPI enabled) |

## 11.13 SPI2_CTRL2_OIS (71h)

OIS configuration register

The auxiliary SPI interface can write this register when the OIS_CTRL_FROM_UI bit in the FUNC_CFG_ACCESS (01h) register is equal to 0 (SPI2 full control mode); this register is read-only when the OIS_CTRL_FROM_UI bit is equal to 1 (primary IF full control mode) and shows the content of the UI_CTRL2_OIS (71h) register.

**Table 243. SPI2_CTRL2_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | LPF1_G_ OIS_BW_1 | LPF1_G_ OIS_BW_0 | FS_G _OIS_2 | FS_G _OIS_1 | FS_G _OIS_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 244. SPI2_CTRL2_OIS register description**

| | |
|---|---|
| LPF1_G_OIS_BW_[1:0] | Gyroscope OIS digital LPF1 filter bandwidth selection. Refer to Table 245. |
| FS_G_OIS_[2:0] | Gyroscope OIS full-scale selection:<br>(000: ±125 dps;<br>001: ±250 dps;<br>010: ±500 dps;<br>011: ±1000 dps;<br>100: ±2000 dps;<br>101: reserved;<br>110: reserved;<br>111: reserved) |

**Table 245. Gyroscope OIS chain digital LPF1 filter bandwidth selection**

| LPF1_G_OIS_BW_[1:0] | Cutoff [Hz] | Phase @ 20 Hz [°] |
|---|---|---|
| 00 | 293 Hz | -7.1° |
| 01 | 217 Hz | -9.1° |
| 10 | 158 Hz | -11.9° |
| 11 | 476 Hz | -5.1° |

## 11.14 SPI2_CTRL3_OIS (72h)

OIS configuration register

The auxiliary SPI interface can write this register when the OIS_CTRL_FROM_UI bit in the FUNC_CFG_ACCESS (01h) register is equal to 0 (SPI2 full control mode); this register is read-only when the OIS_CTRL_FROM_UI bit is equal to 1 (primary IF full control mode) and shows the content of the UI_CTRL3_OIS (72h) register.

**Table 246. SPI2_CTRL3_OIS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | LPF_XL_ OIS_BW_2 | LPF_XL_ OIS_BW_1 | LPF_XL_ OIS_BW_0 | 0(1) | FS_XL _OIS_1 | FS_XL _OIS_0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 247. SPI2_CTRL3_OIS register description**

| | |
|---|---|
| LPF_XL_OIS_BW_[2:0] | Selects accelerometer OIS channel bandwidth, see Table 248. Default value: 0 |
| FS_XL_OIS_[1:0] | Selects accelerometer OIS channel full-scale:<br>(00: ±2 *g* (default);<br>01: ±4 *g*;<br>10: ±8 *g*;<br>11: ±16 *g*) |

*Note: When the accelerometer full-scale value is selected only from the UI side it is readable also from the OIS side.*

**Table 248. Accelerometer OIS channel bandwidth and phase**

| LPF_XL_OIS_BW_[2:0] | Typ. overall bandwidth [Hz] | Typ. overall phase [°] |
|---|---|---|
| 000 | 749 Hz | -3.41 deg @ 20 Hz |
| 001 | 539 Hz | -4.04 deg@ 20 Hz |
| 010 | 342 Hz | -5.31 deg@ 20 Hz |
| 011 | 162 Hz | -9.08 deg@ 20 Hz |
| 100 | 78.5 Hz | -16.4 deg @ 20 Hz |
| 101 | 38.6 Hz | -29.6 deg@ 20 Hz |
| 110 | 19.3 Hz | -28.8 deg @ 10 Hz |
| 111 | 9.8 Hz | -29.1 deg @ 5 Hz |

# 12 Embedded functions register mapping

The table given below provides a list of the registers for the embedded functions available in the device and the corresponding addresses. Embedded functions registers are accessible when EMB_FUNC_REG_ACCESS is set to 1 in FUNC_CFG_ACCESS (01h).

**Table 249. Register address map - embedded functions**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| PAGE_SEL | R/W | 02 | 00000010 | 00000001 | |
| EMB_FUNC_EN_A | R/W | 04 | 00000100 | 00000000 | |
| EMB_FUNC_EN_B | R/W | 05 | 00000101 | 00000000 | |
| EMB_FUNC_EXEC_STATUS | R | 07 | 00000111 | output | |
| PAGE_ADDRESS | R/W | 08 | 00001000 | 00000000 | |
| PAGE_VALUE | R/W | 09 | 00001001 | 00000000 | |
| EMB_FUNC_INT1 | R/W | 0A | 00001010 | 00000000 | |
| FSM_INT1 | R/W | 0B | 00001011 | 00000000 | |
| RESERVED | - | 0C-0D | | | |
| EMB_FUNC_INT2 | R/W | 0E | 00001110 | 00000000 | |
| FSM_INT2 | R/W | 0F | 00001111 | 00000000 | |
| RESERVED | - | 10-11 | | | |
| EMB_FUNC_STATUS | R | 12 | 00010010 | output | |
| FSM_STATUS | R | 13 | 00010011 | output | |
| RESERVED | - | 14-15 | | | |
| PAGE_RW | R/W | 17 | 00010111 | 00000000 | |
| RESERVED | - | 18-43 | | | |
| EMB_FUNC_FIFO_EN_A | R/W | 44 | 01000100 | 00000000 | |
| RESERVED | - | 45 | | | |
| FSM_ENABLE | R/W | 46 | 01000110 | 00000000 | |
| RESERVED | - | 47 | | | |
| FSM_LONG_COUNTER_L | R/W | 48 | 01001000 | 00000000 | |
| FSM_LONG_COUNTER_H | R/W | 49 | 01001001 | 00000000 | |
| RESERVED | - | 4A | | | |
| INT_ACK_MASK | R/W | 4B | 01001011 | 00000000 | |
| FSM_OUTS1 | R | 4C | 01001100 | output | |
| FSM_OUTS2 | R | 4D | 01001101 | output | |
| FSM_OUTS3 | R | 4E | 01001110 | output | |
| FSM_OUTS4 | R | 4F | 01001111 | output | |
| FSM_OUTS5 | R | 50 | 01010000 | output | |
| FSM_OUTS6 | R | 51 | 01010001 | output | |
| FSM_OUTS7 | R | 52 | 01010010 | output | |
| FSM_OUTS8 | R | 53 | 01010011 | output | |
| RESERVED | - | 54- 5E | | | |

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| FSM_ODR | R/W | 5F | 01011111 | 01001011 | |
| RESERVED | - | 60 | | | |
| STEP_COUNTER_L | R | 62 | 01100010 | output | |
| STEP_COUNTER_H | R | 63 | 01100011 | output | |
| EMB_FUNC_SRC | R/W | 64 | 01100100 | output | |
| EMB_FUNC_INIT_A | R/W | 66 | 01100110 | 00000000 | |
| EMB_FUNC_INIT_B | R/W | 67 | 01100111 | 00000000 | |

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

# 13 Embedded functions register description

## 13.1 PAGE_SEL (02h)

Enable advanced features dedicated page (R/W)

**Table 250. PAGE_SEL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PAGE_SEL3 | PAGE_SEL2 | PAGE_SEL1 | PAGE_SEL0 | 0(1) | 0(1) | 0(1) | 1(2) |

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

**Table 251. PAGE_SEL register description**

| | |
|---|---|
| PAGE_SEL[3:0] | Selects the advanced features dedicated page. Default value: 0000 |

## 13.2 EMB_FUNC_EN_A (04h)

Enable embedded functions register (R/W)

**Table 252. EMB_FUNC_EN_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | SIGN_ MOTION_EN | TILT_EN | PEDO_EN | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 253. EMB_FUNC_EN_A register description**

| | |
|---|---|
| SIGN_MOTION_EN | Enables significant motion detection function. Default value: 0<br>(0: significant motion detection function disabled;<br>1: significant motion detection function enabled) |
| TILT_EN | Enables tilt calculation. Default value: 0<br>(0: tilt algorithm disabled;<br>1: tilt algorithm enabled) |
| PEDO_EN | Enables pedometer algorithm. Default value: 0<br>(0: pedometer algorithm disabled;<br>1: pedometer algorithm enabled) |

## 13.3 EMB_FUNC_EN_B (05h)

Enable embedded functions register (R/W)

**Table 254. EMB_FUNC_EN_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | FIFO_ COMPR_EN | 0(1) | 0(1) | FSM_EN |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 255. EMB_FUNC_EN_B register description**

| | |
|---|---|
| FIFO_COMPR_EN(1) | Enables FIFO compression function. Default value: 0<br>(0: FIFO compression function disabled;<br>1: FIFO compression function enabled) |
| FSM_EN | Enables finite state machine (FSM) function. Default value: 0<br>(0: FSM function disabled; 1: FSM function enabled) |

1. *This bit is activated if the FIFO_COMPR_RT_EN bit of FIFO_CTRL2 (08h) is set to 1.*

## 13.4 EMB_FUNC_EXEC_STATUS (07h)

Embedded functions execution status register (R)

**Table 256. EMB_FUNC_EXEC_STATUS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | EMB_FUNC_ EXEC_OVR | EMB_FUNC _ENDOP |

**Table 257. EMB_FUNC_EXEC_STATUS register description**

| | |
|---|---|
| EMB_FUNC_EXEC_OVR | This bit is set to 1 when the execution of the embedded functions program exceeds maximum time (new data are generated before the end of the algorithms). Default value: 0 |
| EMB_FUNC_ENDOP | When this bit is set to 1, no embedded function is running. Default value: 0 |

## 13.5 PAGE_ADDRESS (08h)

Page address register (R/W)

**Table 258. PAGE_ADDRESS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PAGE_ ADDR7 | PAGE_ ADDR6 | PAGE_ ADDR5 | PAGE_ ADDR4 | PAGE_ ADDR3 | PAGE_ ADDR2 | PAGE_ ADDR1 | PAGE_ ADDR0 |

**Table 259. PAGE_ADDRESS register description**

| | |
|---|---|
| PAGE_ADDR[7:0] | After setting the bit PAGE_WRITE / PAGE_READ in register PAGE_RW (17h), this register is used to set the address of the register to be written/read in the advanced features page selected through the bits PAGE_SEL[3:0] in register PAGE_SEL (02h). |

## 13.6 PAGE_VALUE (09h)

Page value register (R/W)

**Table 260. PAGE_VALUE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PAGE_ VALUE7 | PAGE_ VALUE6 | PAGE_ VALUE5 | PAGE_ VALUE4 | PAGE_ VALUE3 | PAGE_ VALUE2 | PAGE_ VALUE1 | PAGE_ VALUE0 |

**Table 261. PAGE_VALUE register description**

| | |
|---|---|
| PAGE_VALUE[7:0] | These bits are used to write (if the bit PAGE_WRITE = 1 in register PAGE_RW (17h)) or read (if the bit PAGE_READ = 1 in register PAGE_RW (17h)) the data at the address PAGE_ADDR[7:0] of the selected advanced features page. |

## 13.7 EMB_FUNC_INT1 (0Ah)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

**Table 262. EMB_FUNC_INT1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT1_ FSM_LC | 0(1) | INT1_ SIG_MOT | INT1_TILT | INT1_STEP _DETECTOR | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 263. EMB_FUNC_INT1 register description**

| | |
|---|---|
| INT1_FSM_LC(1) | Routing FSM long counter timeout interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_SIG_MOT(1) | Routing significant motion event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_TILT(1) | Routing tilt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_STEP_DETECTOR(1) | Routing pedometer step recognition event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |

1. *This bit is activated if the INT1_EMB_FUNC bit of MD1_CFG (5Eh) is set to 1.*

## 13.8 FSM_INT1 (0Bh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

**Table 264. FSM_INT1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT1_FSM8 | INT1_FSM7 | INT1_FSM6 | INT1_FSM5 | INT1_FSM4 | INT1_FSM3 | INT1_FSM2 | INT1_FSM1 |

**Table 265. FSM_INT1 register description**

| | |
|---|---|
| INT1_FSM8[1] | Routing FSM8 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM7[1] | Routing FSM7 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM6[1] | Routing FSM6 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM5[1] | Routing FSM5 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM4[1] | Routing FSM4 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM3[1] | Routing FSM3 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM2[1] | Routing FSM2 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |
| INT1_FSM1[1] | Routing FSM1 interrupt event to INT1. Default value: 0<br>(0: routing to INT1 disabled; 1: routing to INT1 enabled) |

1. *This bit is activated if the INT1_EMB_FUNC bit of MD1_CFG (5Eh) is set to 1.*

## 13.9 EMB_FUNC_INT2 (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

**Table 266. EMB_FUNC_INT2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_ FSM_LC | 0(1) | INT2_ SIG_MOT | INT2_TILT | INT2_STEP _DETECTOR | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 267. EMB_FUNC_INT2 register description**

| | |
|---|---|
| INT2_FSM_LC(1) | Routing FSM long counter timeout interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_SIG_MOT(1) | Routing significant motion event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_TILT(1) | Routing tilt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_STEP_DETECTOR(1) | Routing pedometer step recognition event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |

1. *This bit is activated if the INT2_EMB_FUNC bit of MD2_CFG (5Fh) is set to 1.*

## 13.10 FSM_INT2 (0Fh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

**Table 268. FSM_INT2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| INT2_FSM8 | INT2_FSM7 | INT2_FSM6 | INT2_FSM5 | INT2_FSM4 | INT2_FSM3 | INT2_FSM2 | INT2_FSM1 |

**Table 269. FSM_INT2 register description**

| | |
|---|---|
| INT2_FSM8(1) | Routing FSM8 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM7(1) | Routing FSM7 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM6(1) | Routing FSM6 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM5(1) | Routing FSM5 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM4(1) | Routing FSM4 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM3(1) | Routing FSM3 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM2(1) | Routing FSM2 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |
| INT2_FSM1(1) | Routing FSM1 interrupt event to INT2. Default value: 0<br>(0: routing to INT2 disabled; 1: routing to INT2 enabled) |

1. *This bit is activated if the INT2_EMB_FUNC bit of MD2_CFG (5Fh) is set to 1.*

## 13.11 EMB_FUNC_STATUS (12h)

Embedded function status register (R)

**Table 270. EMB_FUNC_STATUS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_FSM_LC | 0 | IS_SIGMOT | IS_TILT | IS_STEP_DET | 0 | 0 | 0 |

**Table 271. EMB_FUNC_STATUS register description**

| | |
|---|---|
| IS_FSM_LC | Interrupt status bit for FSM long counter timeout interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_SIGMOT | Interrupt status bit for significant motion detection<br>(1: interrupt detected; 0: no interrupt) |
| IS_TILT | Interrupt status bit for tilt detection<br>(1: interrupt detected; 0: no interrupt) |
| IS_STEP_DET | Interrupt status bit for step detection<br>(1: interrupt detected; 0: no interrupt) |

## 13.12 FSM_STATUS (13h)

Finite state machine status register (R)

**Table 272. FSM_STATUS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IS_FSM8 | IS_FSM7 | IS_FSM6 | IS_FSM5 | IS_FSM4 | IS_FSM3 | IS_FSM2 | IS_FSM1 |

**Table 273. FSM_STATUS register description**

| | |
|---|---|
| IS_FSM8 | Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM7 | Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM6 | Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM5 | Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM4 | Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM3 | Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM2 | Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM1 | Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt) |

## 13.13 PAGE_RW (17h)

Enable read and write mode of advanced features dedicated page (R/W)

**Table 274. PAGE_RW register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EMB_ FUNC_LIR | PAGE_ WRITE | PAGE_ READ | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 275. PAGE_RW register description**

| | |
|---|---|
| EMB_FUNC_LIR | Latched interrupt mode for embedded functions. Default value: 0<br>(0: embedded functions interrupt request not latched;<br>1: embedded functions interrupt request latched) |
| PAGE_WRITE | Enables writes to the selected advanced features dedicated page.(1) Default value: 0<br>(1: enable; 0: disable) |
| PAGE_READ | Enables reads from the selected advanced features dedicated page.(1) Default value: 0<br>(1: enable; 0: disable) |

1. *Page selected by PAGE_SEL[3:0] in PAGE_SEL (02h) register.*

## 13.14 EMB_FUNC_FIFO_EN_A (44h)

Embedded functions FIFO configuration register A (R/W)

**Table 276. EMB_FUNC_FIFO_EN_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | STEP_COUNTER_FIFO_EN | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 277. EMB_FUNC_FIFO_EN_A register description**

| | |
|---|---|
| STEP_COUNTER_FIFO_EN | Enables batching the step counter values in the FIFO buffer. Default value: 0<br>(0: disabled; 1: enabled) |

## 13.15 FSM_ENABLE (46h)

Enable FSM register (R/W)

**Table 278. FSM_ENABLE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM8_EN | FSM7_EN | FSM6_EN | FSM5_EN | FSM4_EN | FSM3_EN | FSM2_EN | FSM1_EN |

**Table 279. FSM_ENABLE register description**

| | |
|---|---|
| FSM8_EN | Enables FSM8. Default value: 0 (0: FSM8 disabled; 1: FSM8 enabled) |
| FSM7_EN | Enables FSM7. Default value: 0 (0: FSM7 disabled; 1: FSM7 enabled) |
| FSM6_EN | Enables FSM6. Default value: 0 (0: FSM6 disabled; 1: FSM6 enabled) |
| FSM5_EN | Enables FSM5. Default value: 0 (0: FSM5 disabled; 1: FSM5 enabled) |
| FSM4_EN | Enables FSM4. Default value: 0 (0: FSM4 disabled; 1: FSM4 enabled) |
| FSM3_EN | Enables FSM3. Default value: 0 (0: FSM3 disabled; 1: FSM3 enabled) |
| FSM2_EN | Enables FSM2. Default value: 0 (0: FSM2 disabled; 1: FSM2 enabled) |
| FSM1_EN | Enables FSM1. Default value: 0 (0: FSM1 disabled; 1: FSM1 enabled) |

## 13.16 FSM_LONG_COUNTER_L (48h) and FSM_LONG_COUNTER_H (49h)

FSM long counter status register (R/W)

The long counter value is an unsigned integer value (16-bit format).

**Table 280. FSM_LONG_COUNTER_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_LC_7 | FSM_LC_6 | FSM_LC_5 | FSM_LC_4 | FSM_LC_3 | FSM_LC_2 | FSM_LC_1 | FSM_LC_0 |

**Table 281. FSM_LONG_COUNTER_L register description**

| | |
|---|---|
| FSM_LC_[7:0] | Long counter current value (LSbyte). Default value: 00000000 |

**Table 282. FSM_LONG_COUNTER_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_LC_15 | FSM_LC_14 | FSM_LC_13 | FSM_LC_12 | FSM_LC_11 | FSM_LC_10 | FSM_LC_9 | FSM_LC_8 |

**Table 283. FSM_LONG_COUNTER_H register description**

| | |
|---|---|
| FSM_LC_[15:8] | Long counter current value (MSbyte). Default value: 00000000 |

## 13.17 INT_ACK_MASK (4Bh)

Reset status register (R/W)

**Table 284. INT_ACK_MASK register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IACK_ MASK7 | IACK_ MASK6 | IACK_ MASK5 | IACK_ MASK4 | IACK_ MASK3 | IACK_ MASK2 | IACK_ MASK1 | IACK_ MASK0 |

**Table 285. INT_ACK_MASK register description**

| | |
|---|---|
| IACK_MASK7 | If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h) and FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 7 of the status register is not reset. When this bit is set to 0, bit 7 of the status register is reset. Default value: 0 |
| IACK_MASK6 | If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h) and FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 6 of the status register is not reset. When this bit is set to 0, bit 6 of the status register is reset. Default value: 0 |
| IACK_MASK5 | If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h) and FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 5 of the status register is not reset. When this bit is set to 0, bit 5 of the status register is reset. Default value: 0 |
| IACK_MASK4 | If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h) and FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 4 of the status register is not reset. When this bit is set to 0, bit 4 of the status register is reset. Default value: 0 |
| IACK_MASK3 | If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h) and FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 3 of the status register is not reset. When this bit is set to 0, bit 3 of the status register is reset. Default value: 0 |
| IACK_MASK2 | If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h) and FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 2 of the status register is not reset. When this bit is set to 0, bit 2 of the status register is reset. Default value: 0 |
| IACK_MASK1 | If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h) and FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 1 of the status register is not reset. When this bit is set to 0, bit 1 of the status register is reset. Default value: 0 |
| IACK_MASK0 | If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (49h) and FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (4Ah) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 0 of the status register is not reset. When this bit is set to 0, bit 0 of the status register is reset. Default value: 0 |

## 13.18 FSM_OUTS1 (4Ch)

FSM1 output register (R)

**Table 286. FSM_OUTS1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 287. FSM_OUTS1 register description**

| | |
|---|---|
| P_X | FSM1 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM1 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM1 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM1 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM1 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM1 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM1 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM1 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 13.19 FSM_OUTS2 (4Dh)

FSM2 output register (R)

**Table 288. FSM_OUTS2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 289. FSM_OUTS2 register description**

| | |
|---|---|
| P_X | FSM2 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM2 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM2 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM2 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM2 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM2 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM2 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM2 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 13.20 FSM_OUTS3 (4Eh)

FSM3 output register (R)

**Table 290. FSM_OUTS3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 291. FSM_OUTS3 register description**

| | |
|---|---|
| P_X | FSM3 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM3 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM3 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM3 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM3 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM3 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM3 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM3 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 13.21 FSM_OUTS4 (4Fh)

FSM4 output register (R)

**Table 292. FSM_OUTS4 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 293. FSM_OUTS4 register description**

| | |
|---|---|
| P_X | FSM4 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM4 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM4 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM4 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM4 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM4 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM4 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM4 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 13.22 FSM_OUTS5 (50h)

FSM5 output register (R)

**Table 294. FSM_OUTS5 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 295. FSM_OUTS5 register description**

| | |
|---|---|
| P_X | FSM5 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM5 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM5 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM5 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM5 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM5 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM5 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM5 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 13.23 FSM_OUTS6 (51h)

FSM6 output register (R)

**Table 296. FSM_OUTS6 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 297. FSM_OUTS6 register description**

| | |
|---|---|
| P_X | FSM6 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM6 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM6 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM6 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM6 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM6 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM6 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM6 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 13.24 FSM_OUTS7 (52h)

FSM7 output register (R)

**Table 298. FSM_OUTS7 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 299. FSM_OUTS7 register description**

| | |
|---|---|
| P_X | FSM7 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM7 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM7 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM7 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM7 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM7 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM7 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM7 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 13.25 FSM_OUTS8 (53h)

FSM8 output register (R)

**Table 300. FSM_OUTS8 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |

**Table 301. FSM_OUTS8 register description**

| | |
|---|---|
| P_X | FSM8 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM8 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM8 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM8 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM8 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM8 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM8 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM8 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 13.26 FSM_ODR (5Fh)

Finite state machine output data rate configuration register (R/W)

**Table 302. FSM_ODR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 1(2) | FSM_ODR_2 | FSM_ODR_1 | FSM_ODR_0 | 0(1) | 1(2) | 1(2) |

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

**Table 303. FSM_ODR register description**

| | |
|---|---|
| FSM_ODR_[2:0] | Finite state machine ODR configuration:<br>(000: 15 Hz;<br>001: 30 Hz (default);<br>010: 60 Hz;<br>011: 120 Hz;<br>100: 240 Hz;<br>101: 480 Hz;<br>110: 960 Hz) |

## 13.27 STEP_COUNTER_L (62h) and STEP_COUNTER_H (63h)

Step counter output register (R)

**Table 304. STEP_COUNTER_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| STEP_7 | STEP_6 | STEP_5 | STEP_4 | STEP_3 | STEP_2 | STEP_1 | STEP_0 |

**Table 305. STEP_COUNTER_L register description**

| | |
|---|---|
| STEP_[7:0] | Step counter output (LSbyte) |

**Table 306. STEP_COUNTER_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| STEP_15 | STEP_14 | STEP_13 | STEP_12 | STEP_11 | STEP_10 | STEP_9 | STEP_8 |

**Table 307. STEP_COUNTER_H register description**

| | |
|---|---|
| STEP_[15:8] | Step counter output (MSbyte) |

## 13.28 EMB_FUNC_SRC (64h)

Embedded function source register (R/W)

**Table 308. EMB_FUNC_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PEDO_ RST_STEP | 0(1) | STEP_ DETECTED | STEP_COUNT _DELTA_IA | STEP_ OVERFLOW | STEPCOUNTER _BIT_SET | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 309. EMB_FUNC_SRC register description**

| | |
|---|---|
| PEDO_RST_STEP | Reset pedometer step counter. Read/write bit.<br>(0: disabled; 1: enabled) |
| STEP_DETECTED | Step detector event detection status. Read-only bit.<br>(0: step detection event not detected; 1: step detection event detected) |
| STEP_COUNT_DELTA_IA | Pedometer step recognition on delta time status. Read-only bit.<br>(0: no step recognized during delta time;<br>1: at least one step recognized during delta time) |
| STEP_OVERFLOW | Step counter overflow status. Read-only bit.<br>(0: step counter value < $2^{16}$; 1: step counter value reached $2^{16}$) |
| STEPCOUNTER_BIT_SET | This bit is equal to 1 when the step count is increased. If a timer period is programmed in PEDO_SC_DELTAT_L (D0h) and PEDO_SC_DELTAT_H (D1h) embedded advanced features (page 1) registers, this bit is kept at 0.<br>Read-only bit. |

## 13.29 EMB_FUNC_INIT_A (66h)

Embedded functions initialization register (R/W)

**Table 310. EMB_FUNC_INIT_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | SIG_MOT_INIT | TILT_INIT | STEP_DET_INIT | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 311. EMB_FUNC_INIT_A register description**

| | |
|---|---|
| SIG_MOT_INIT | Significant motion detection algorithm initialization request. Default value: 0 |
| TILT_INIT | Tilt algorithm initialization request. Default value: 0 |
| STEP_DET_INIT | Pedometer step counter/detector algorithm initialization request. Default value: 0 |

## 13.30 EMB_FUNC_INIT_B (67h)

Embedded functions initialization register (R/W)

**Table 312. EMB_FUNC_INIT_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | FIFO_COMPR_INIT | 0(1) | 0(1) | FSM_INIT |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 313. EMB_FUNC_INIT_B register description**

| | |
|---|---|
| FIFO_COMPR_INIT | FIFO compression feature initialization request. Default value: 0 |
| FSM_INIT | FSM initialization request. Default value: 0 |

# 14 Embedded advanced features pages

The table given below provides a list of the registers for the embedded advanced features page 0. These registers are accessible when PAGE_SEL[3:0] are set to 0000 in PAGE_SEL (02h).

*Note: External sensor offset compensation registers and transformation matrix correction registers affect FSM data only. When these registers are set with their default values, no compensation is applied.*

**Table 314. Register address map - embedded advanced features page 0**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| FSM_EXT_SENSITIVITY_L | R/W | BA | 10111010 | 00100100 | |
| FSM_EXT_SENSITIVITY_H | R/W | BB | 10111011 | 00010110 | |
| FSM_EXT_OFFX_L | R/W | C0 | 11000000 | 00000000 | |
| FSM_EXT_OFFX_H | R/W | C1 | 11000001 | 00000000 | |
| FSM_EXT_OFFY_L | R/W | C2 | 11000010 | 00000000 | |
| FSM_EXT_OFFY_H | R/W | C3 | 11000011 | 00000000 | |
| FSM_EXT_OFFZ_L | R/W | C4 | 11000100 | 00000000 | |
| FSM_EXT_OFFZ_H | R/W | C5 | 11000101 | 00000000 | |
| FSM_EXT_MATRIX_XX_L | R/W | C6 | 11000110 | 00000000 | |
| FSM_EXT_MATRIX_XX_H | R/W | C7 | 11000111 | 00111100 | |
| FSM_EXT_MATRIX_XY_L | R/W | C8 | 11001000 | 00000000 | |
| FSM_EXT_MATRIX_XY_H | R/W | C9 | 11001001 | 00000000 | |
| FSM_EXT_MATRIX_XZ_L | R/W | CA | 11001010 | 00000000 | |
| FSM_EXT_MATRIX_XZ_H | R/W | CB | 11001011 | 00000000 | |
| FSM_EXT_MATRIX_YY_L | R/W | CC | 11001100 | 00000000 | |
| FSM_EXT_MATRIX_YY_H | R/W | CD | 11001101 | 00111100 | |
| FSM_EXT_MATRIX_YZ_L | R/W | CE | 11001110 | 00000000 | |
| FSM_EXT_MATRIX_YZ_H | R/W | CF | 11001111 | 00000000 | |
| FSM_EXT_MATRIX_ZZ_L | R/W | D0 | 11010000 | 00000000 | |
| FSM_EXT_MATRIX_ZZ_H | R/W | D1 | 11010001 | 00111100 | |
| EXT_CFG_A | R/W | D4 | 11010100 | 00000101 | |
| EXT_CFG_B | R/W | D5 | 11010101 | 00000010 | |

The following table provides a list of the registers for the embedded advanced features page 1. These registers are accessible when PAGE_SEL[3:0] are set to 0001 in PAGE_SEL (02h).

**Table 315. Register address map - embedded advanced features page 1**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| FSM_LC_TIMEOUT_L | R/W | 7A | 01111010 | 00000000 | |
| FSM_LC_TIMEOUT_H | R/W | 7B | 01111011 | 00000000 | |
| FSM_PROGRAMS | R/W | 7C | 01111100 | 00000000 | |
| FSM_START_ADD_L | R/W | 7E | 01111110 | 00000000 | |
| FSM_START_ADD_H | R/W | 7F | 01111111 | 00000000 | |
| PEDO_CMD_REG | R/W | 83 | 10000011 | 00000000 | |
| PEDO_DEB_STEPS_CONF | R/W | 84 | 10000100 | 00001010 | |
| PEDO_SC_DELTAT_L | R/W | D0 | 11010000 | 00000000 | |
| PEDO_SC_DELTAT_H | R/W | D1 | 11010001 | 00000000 | |

The following table provides a list of the registers for the embedded advanced features page 2. These registers are accessible when PAGE_SEL[3:0] are set to 0010 in PAGE_SEL (02h).

**Table 316. Register address map - embedded advanced features page 2**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| EXT_FORMAT | R/W | 00 | 00000000 | 00000000 | |
| EXT_3BYTE_SENSITIVITY_L | R/W | 02 | 00000010 | 00000000 | |
| EXT_3BYTE_SENSITIVITY_H | R/W | 03 | 00000011 | 00001100 | |
| EXT_3BYTE_OFFSET_XL | R/W | 06 | 00000110 | 00000000 | |
| EXT_3BYTE_OFFSET_L | R/W | 07 | 00000111 | 01010100 | |
| EXT_3BYTE_OFFSET_H | R/W | 08 | 00001000 | 00111111 | |

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

**Write procedure example:** write value 06h in register at address 84h (PEDO_DEB_STEPS_CONF) in Page 1

1. Write bit EMB_FUNC_REG_ACCESS = 1 in FUNC_CFG_ACCESS (01h) // Enable access to embedded functions registers
2. Write bit PAGE_WRITE = 1 in PAGE_RW (17h) register // Select write operation mode
3. Write 0001 in PAGE_SEL[3:0] field of register PAGE_SEL (02h) // Select page 1
4. Write 84h in PAGE_ADDR register (08h) // Set address
5. Write 06h in PAGE_DATA register (09h) // Set value to be written
6. Write bit PAGE_WRITE = 0 in PAGE_RW (17h) register // Write operation disabled
7. Write bit EMB_FUNC_REG_ACCESS = 0 in FUNC_CFG_ACCESS (01h) // Disable access to embedded functions registers

**Read procedure example**: read value of register at address 84h (PEDO_DEB_STEPS_CONF) in Page 1

| | | |
|---|---|---|
| 1. | Write bit EMB_FUNC_REG_ACCESS = 1 in FUNC_CFG_ACCESS (01h) | // Enable access to embedded functions registers |
| 2. | Write bit PAGE_READ = 1 in PAGE_RW (17h) register | // Select read operation mode |
| 3. | Write 0001 in PAGE_SEL[3:0] field of register PAGE_SEL (02h) | // Select page 1 |
| 4. | Write 84h in PAGE_ADDR register (08h) | // Set address |
| 5. | Read value of PAGE_DATA register (09h) | // Get register value |
| 6. | Write bit PAGE_READ = 0 in PAGE_RW (17h) register | // Read operation disabled |
| 7. | Write bit EMB_FUNC_REG_ACCESS = 0 in FUNC_CFG_ACCESS (01h) | // Disable access to embedded functions registers |

*Note: Steps 1 and 2 of both procedures are intended to be performed at the beginning of the procedure. Steps 6 and 7 of both procedures are intended to be performed at the end of the procedure. If the procedure involves multiple operations, only steps 3, 4 and 5 must be repeated for each operation. If, in particular, the multiple operations involve consecutive registers, only step 5 can be performed.*

# 15 Embedded advanced features register description

## 15.1 Page 0 - embedded advanced features registers

### 15.1.1 FSM_EXT_SENSITIVITY_L (BAh) and FSM_EXT_SENSITIVITY_H (BBh)

External sensor sensitivity value register for the finite state machine (R/W)

This register corresponds to the conversion value of the external sensor. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Default value of FSM_EXT_S_[15:0] bits is 0x1624 (when using an external magnetometer this value corresponds to 0.0015 gauss/LSB).

**Table 317. FSM_EXT_SENSITIVITY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_S_7 | FSM_EXT_S_6 | FSM_EXT_S_5 | FSM_EXT_S_4 | FSM_EXT_S_3 | FSM_EXT_S_2 | FSM_EXT_S_1 | FSM_EXT_S_0 |

**Table 318. FSM_EXT_SENSITIVITY_L register description**

| | |
|---|---|
| FSM_EXT_S_[7:0] | External sensor sensitivity (LSbyte). Default value: 00100100 |

**Table 319. FSM_EXT_SENSITIVITY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_S_15 | FSM_EXT_S_14 | FSM_EXT_S_13 | FSM_EXT_S_12 | FSM_EXT_S_11 | FSM_EXT_S_10 | FSM_EXT_S_9 | FSM_EXT_S_8 |

**Table 320. FSM_EXT_SENSITIVITY_H register description**

| | |
|---|---|
| FSM_EXT_S_[15:8] | External sensor (MSbyte). Default value: 00010110 |

### 15.1.2 FSM_EXT_OFFX_L (C0h) and FSM_EXT_OFFX_H (C1h)

External sensor X-axis offset

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 321. FSM_EXT_OFFX_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_OFFX_7 | FSM_EXT_OFFX_6 | FSM_EXT_OFFX_5 | FSM_EXT_OFFX_4 | FSM_EXT_OFFX_3 | FSM_EXT_OFFX_2 | FSM_EXT_OFFX_1 | FSM_EXT_OFFX_0 |

**Table 322. FSM_EXT_OFFX_L register description**

| | |
|---|---|
| FSM_EXT_OFFX_[7:0] | External sensor X-axis offset (LSbyte). Default value: 00000000 |

**Table 323. FSM_EXT_OFFX_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_OFFX_15 | FSM_EXT_OFFX_14 | FSM_EXT_OFFX_13 | FSM_EXT_OFFX_12 | FSM_EXT_OFFX_11 | FSM_EXT_OFFX_10 | FSM_EXT_OFFX_9 | FSM_EXT_OFFX_8 |

**Table 324. FSM_EXT_OFFX_H register description**

| | |
|---|---|
| FSM_EXT_OFFX_[15:8] | External sensor X-axis offset (MSbyte). Default value: 00000000 |

### 15.1.3 FSM_EXT_OFFY_L (C2h) and FSM_EXT_OFFY_H (C3h)

External sensor Y-axis offset

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 325. FSM_EXT_OFFY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_OFFY_7 | FSM_EXT_OFFY_6 | FSM_EXT_OFFY_5 | FSM_EXT_OFFY_4 | FSM_EXT_OFFY_3 | FSM_EXT_OFFY_2 | FSM_EXT_OFFY_1 | FSM_EXT_OFFY_0 |

**Table 326. FSM_EXT_OFFY_L register description**

| | |
|---|---|
| FSM_EXT_OFFY_[7:0] | External sensor Y-axis offset (LSbyte). Default value: 00000000 |

**Table 327. FSM_EXT_OFFY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_OFFY_15 | FSM_EXT_OFFY_14 | FSM_EXT_OFFY_13 | FSM_EXT_OFFY_12 | FSM_EXT_OFFY_11 | FSM_EXT_OFFY_10 | FSM_EXT_OFFY_9 | FSM_EXT_OFFY_8 |

**Table 328. FSM_EXT_OFFY_H register description**

| | |
|---|---|
| FSM_EXT_OFFY_[15:8] | External sensor Y-axis offset (MSbyte). Default value: 00000000 |

### 15.1.4 FSM_EXT_OFFZ_L (C4h) and FSM_EXT_OFFZ_H (C5h)

External sensor Z-axis offset register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 329. FSM_EXT_OFFZ_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_OFFZ_7 | FSM_EXT_OFFZ_6 | FSM_EXT_OFFZ_5 | FSM_EXT_OFFZ_4 | FSM_EXT_OFFZ_3 | FSM_EXT_OFFZ_2 | FSM_EXT_OFFZ_1 | FSM_EXT_OFFZ_0 |

**Table 330. FSM_EXT_OFFZ_L register description**

| | |
|---|---|
| FSM_EXT_OFFZ_[7:0] | External sensor Z-axis offset (LSbyte). Default value: 00000000 |

**Table 331. FSM_EXT_OFFZ_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_OFFZ_15 | FSM_EXT_OFFZ_14 | FSM_EXT_OFFZ_13 | FSM_EXT_OFFZ_12 | FSM_EXT_OFFZ_11 | FSM_EXT_OFFZ_10 | FSM_EXT_OFFZ_9 | FSM_EXT_OFFZ_8 |

**Table 332. FSM_EXT_OFFZ_H register description**

| | |
|---|---|
| FSM_EXT_OFFZ_[15:8] | External sensor Z-axis offset (MSbyte). Default value: 00000000 |

### 15.1.5 FSM_EXT_MATRIX_XX_L (C6h) and FSM_EXT_MATRIX_XX_H (C7h)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 333. FSM_EXT_MATRIX_XX_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_XX_7 | FSM_EXT_MAT_XX_6 | FSM_EXT_MAT_XX_5 | FSM_EXT_MAT_XX_4 | FSM_EXT_MAT_XX_3 | FSM_EXT_MAT_XX_2 | FSM_EXT_MAT_XX_1 | FSM_EXT_XX_0 |

**Table 334. FSM_EXT_MATRIX_XX_L register description**

| | |
|---|---|
| FSM_EXT_MAT_XX_[7:0] | Transformation matrix row1 col1 coefficient (LSbyte). Default value: 00000000 |

**Table 335. FSM_EXT_MATRIX_XX_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_XX_15 | FSM_EXT_MAT_XX_14 | FSM_EXT_MAT_XX_13 | FSM_EXT_MAT_XX_12 | FSM_EXT_MAT_XX_11 | FSM_EXT_MAT_XX_10 | FSM_EXT_XX_9 | FSM_EXT_XX_8 |

**Table 336. FSM_EXT_MATRIX_XX_H register description**

| | |
|---|---|
| FSM_EXT_MAT_[15:8] | Transformation matrix row1 col1 coefficient (MSbyte). Default value: 00111100 |

### 15.1.6 FSM_EXT_MATRIX_XY_L (C8h) and FSM_EXT_MATRIX_XY_H (C9h)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 337. FSM_EXT_MATRIX_XY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_XY_7 | FSM_EXT_MAT_XY_6 | FSM_EXT_MAT_XY_5 | FSM_EXT_MAT_XY_4 | FSM_EXT_MAT_XY_3 | FSM_EXT_MAT_XY_2 | FSM_EXT_MAT_XY_1 | FSM_EXT_MAT_XY_0 |

**Table 338. FSM_EXT_MATRIX_XY_L register description**

| | |
|---|---|
| FSM_EXT_MAT_XY_[7:0] | Transformation matrix row1 col2 (and row2 col1) coefficient (LSbyte). Default value: 00000000 |

**Table 339. FSM_EXT_MATRIX_XY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_XY_15 | FSM_EXT_XY_14 | FSM_EXT_XY_13 | FSM_EXT_XY_12 | FSM_EXT_XY_11 | FSM_EXT_XY_10 | FSM_EXT_XY_9 | FSM_EXT_XY_8 |

**Table 340. FSM_EXT_MATRIX_XY_H register description**

| | |
|---|---|
| FSM_EXT_MAT_XY_[15:8] | Transformation matrix row1 col2 (and row2 col1) coefficient (MSbyte). Default value: 00000000 |

### 15.1.7 FSM_EXT_MATRIX_XZ_L (CAh) and FSM_EXT_MATRIX_XZ_H (CBh)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 341. FSM_EXT_MATRIX_XZ_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_XZ_7 | FSM_EXT_MAT_XZ_6 | FSM_EXT_MAT_XZ_5 | FSM_EXT_MAT_XZ_4 | FSM_EXT_MAT_XZ_3 | FSM_EXT_MAT_XZ_2 | FSM_EXT_MAT_XZ_1 | FSM_EXT_MAT_XZ_0 |

**Table 342. FSM_EXT_MATRIX_XZ_L register description**

| | |
|---|---|
| FSM_EXT_MAT_XZ_[7:0] | Transformation matrix row1 col3 (and row3 col1) coefficient (LSbyte). Default value: 00000000 |

**Table 343. FSM_EXT_MATRIX_XZ_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_XZ_15 | FSM_EXT_MAT_XZ_14 | FSM_EXT_MAT_XZ_13 | FSM_EXT_MAT_XZ_12 | FSM_EXT_MAT_XZ_11 | FSM_EXT_MAT_XZ_10 | FSM_EXT_MAT_XZ_9 | FSM_EXT_MAT_XZ_8 |

**Table 344. FSM_EXT_MATRIX_XZ_H register description**

| | |
|---|---|
| FSM_EXT_MAT_XZ_[15:8] | Transformation matrix row1 col3 (and row3 col1) coefficient (MSbyte). Default value: 00000000 |

### 15.1.8 FSM_EXT_MATRIX_YY_L (CCh) and FSM_EXT_MATRIX_YY_H (CDh)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 345. FSM_EXT_MATRIX_YY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_YY_7 | FSM_EXT_MAT_YY_6 | FSM_EXT_MAT_YY_5 | FSM_EXT_MAT_YY_4 | FSM_EXT_MAT_YY_3 | FSM_EXT_MAT_YY_2 | FSM_EXT_MAT_YY_1 | FSM_EXT_MAT_YY_0 |

**Table 346. FSM_EXT_MATRIX_YY_L register description**

| | |
|---|---|
| FSM_EXT_MAT_YY_[7:0] | Transformation matrix row2 col2 coefficient (LSbyte). Default value: 00000000 |

**Table 347. FSM_EXT_MATRIX_YY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_YY_15 | FSM_EXT_MAT_YY_14 | FSM_EXT_MAT_YY_13 | FSM_EXT_MAT_YY_12 | FSM_EXT_MAT_YY_11 | FSM_EXT_MAT_YY_10 | FSM_EXT_MAT_YY_9 | FSM_EXT_MAT_YY_8 |

**Table 348. FSM_EXT_MATRIX_YY_H register description**

| | |
|---|---|
| FSM_EXT_MAT_YY_[15:8] | Transformation matrix row2 col2 coefficient (MSbyte). Default value: 00111100 |

### 15.1.9 FSM_EXT_MATRIX_YZ_L (CEh) and FSM_EXT_MATRIX_YZ_H (CFh)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 349. FSM_EXT_MATRIX_YZ_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_YZ_7 | FSM_EXT_MAT_YZ_6 | FSM_EXT_MAT_YZ_5 | FSM_EXT_MAT_YZ_4 | FSM_EXT_MAT_YZ_3 | FSM_EXT_MAT_YZ_2 | FSM_EXT_MAT_YZ_1 | FSM_EXT_MAT_YZ_0 |

**Table 350. FSM_EXT_MATRIX_YZ_L register description**

| | |
|---|---|
| FSM_EXT_MAT_YZ_[7:0] | Transformation matrix row2 col3 (and row3 col2) coefficient (LSbyte).<br>Default value: 00000000 |

**Table 351. FSM_EXT_MATRIX_YZ_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_YZ_15 | FSM_EXT_MAT_YZ_14 | FSM_EXT_MAT_YZ_13 | FSM_EXT_MAT_YZ_12 | FSM_EXT_MAT_YZ_11 | FSM_EXT_MAT_YZ_10 | FSM_EXT_MAT_YZ_9 | FSM_EXT_MAT_YZ_8 |

**Table 352. FSM_EXT_MATRIX_YZ_H register description**

| | |
|---|---|
| FSM_EXT_MAT_YZ_[15:8] | Transformation matrix row2 col3 (and row3 col2) coefficient (MSbyte).<br>Default value: 00000000 |

### 15.1.10 FSM_EXT_MATRIX_ZZ_L (D0h) and FSM_EXT_MATRIX_ZZ_H (D1h)

External sensor transformation matrix register (R/W)

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF
(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 353. FSM_EXT_MATRIX_ZZ_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_ZZ_7 | FSM_EXT_MAT_ZZ_6 | FSM_EXT_MAT_ZZ_5 | FSM_EXT_MAT_ZZ_4 | FSM_EXT_MAT_ZZ_3 | FSM_EXT_MAT_ZZ_2 | FSM_EXT_MAT_ZZ_1 | FSM_EXT_MAT_ZZ_0 |

**Table 354. FSM_EXT_MATRIX_ZZ_L register description**

| | |
|---|---|
| FSM_EXT_MAT_ZZ_[7:0] | Transformation matrix row3 col3 coefficient (LSbyte). Default value: 00000000 |

**Table 355. FSM_EXT_MATRIX_ZZ_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_EXT_MAT_ZZ_15 | FSM_EXT_MAT_ZZ_14 | FSM_EXT_MAT_ZZ_13 | FSM_EXT_MAT_ZZ_12 | FSM_EXT_MAT_ZZ_11 | FSM_EXT_MAT_ZZ_10 | FSM_EXT_MAT_ZZ_9 | FSM_EXT_MAT_ZZ_8 |

**Table 356. FSM_EXT_MATRIX_ZZ_H register description**

| | |
|---|---|
| FSM_EXT_MAT_ZZ_[15:8] | Transformation matrix row3 col3 coefficient (MSbyte). Default value: 00111100 |

### 15.1.11 EXT_CFG_A (D4h)

External sensor coordinates (Z and Y axes) rotation register (r/w).

**Table 357. EXT_CFG_A register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | EXT_Y_ AXIS2 | EXT_Y_ AXIS1 | EXT_Y_ AXIS0 | 0(1) | EXT_Z_ AXIS2 | EXT_Z_ AXIS1 | EXT_Z_ AXIS0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 358. EXT_CFG_A description**

| | |
|---|---|
| EXT_Y_AXIS[2:0] | External sensor Y-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation)<br>(000: Y = Y; (default)<br>001: Y = -Y;<br>010: Y = X;<br>011: Y = -X;<br>100: Y = -Z;<br>101: Y = Z;<br>Others: Y = Y) |
| EXT_Z_AXIS[2:0] | External sensor Z-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation)<br>(000: Z = Y;<br>001: Z = -Y;<br>010: Z = X;<br>011: Z = -X;<br>100: Z = -Z;<br>101: Z = Z; (default)<br>Others: Z = Y) |

### 15.1.12 EXT_CFG_B (D5h)

External sensor coordinates (X-axis) rotation register (r/w).

**Table 359. EXT_CFG_B register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | EXT_X_ AXIS2 | EXT_X_ AXIS1 | EXT_X_ AXIS0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 360. EXT_CFG_B description**

| | |
|---|---|
| EXT_X_AXIS[2:0] | External sensor X-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation)<br>(000: X = Y;<br>001: X = -Y;<br>010: X = X; (default)<br>011: X = -X;<br>100: X = -Z;<br>101: X = Z;<br>Others: X = Y) |

## 15.2 Page 1 - embedded advanced features registers

### 15.2.1 FSM_LC_TIMEOUT_L (7Ah) and FSM_LC_TIMEOUT_H (7Bh)

FSM long counter timeout register (R/W)

The long counter timeout value is an unsigned integer value (16-bit format). When the long counter value reached this value, the FSM generates an interrupt.

**Table 361. FSM_LC_TIMEOUT_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_LC_TIMEOUT7 | FSM_LC_TIMEOUT6 | FSM_LC_TIMEOUT5 | FSM_LC_TIMEOUT4 | FSM_LC_TIMEOUT3 | FSM_LC_TIMEOUT2 | FSM_LC_TIMEOUT1 | FSM_LC_TIMEOUT0 |

**Table 362. FSM_LC_TIMEOUT_L register description**

| | |
|---|---|
| FSM_LC_TIMEOUT[7:0] | FSM long counter timeout value (LSbyte). Default value: 00000000 |

**Table 363. FSM_LC_TIMEOUT_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_LC_TIMEOUT15 | FSM_LC_TIMEOUT14 | FSM_LC_TIMEOUT13 | FSM_LC_TIMEOUT12 | FSM_LC_TIMEOUT11 | FSM_LC_TIMEOUT10 | FSM_LC_TIMEOUT9 | FSM_LC_TIMEOUT8 |

**Table 364. FSM_LC_TIMEOUT_H register description**

| | |
|---|---|
| FSM_LC_TIMEOUT[15:8] | FSM long counter timeout value (MSbyte). Default value: 00000000 |

### 15.2.2 FSM_PROGRAMS (7Ch)

FSM number of programs register (R/W)

**Table 365. FSM_PROGRAMS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_N_PROG7 | FSM_N_PROG6 | FSM_N_PROG5 | FSM_N_PROG4 | FSM_N_PROG3 | FSM_N_PROG2 | FSM_N_PROG1 | FSM_N_PROG0 |

**Table 366. FSM_PROGRAMS register description**

| | |
|---|---|
| FSM_N_PROG[7:0] | Number of FSM programs; must be less than or equal to 8.<br>Default value: 00000000 |

### 15.2.3 FSM_START_ADD_L (7Eh) and FSM_START_ADD_H (7Fh)

FSM start address register (R/W). First available address is 0x35C.

**Table 367. FSM_START_ADD_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_START7 | FSM_START6 | FSM_START5 | FSM_START4 | FSM_START3 | FSM_START2 | FSM_START1 | FSM_START0 |

**Table 368. FSM_START_ADD_L register description**

| | |
|---|---|
| FSM_START[7:0] | FSM start address value (LSbyte). Default value: 00000000 |

**Table 369. FSM_START_ADD_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FSM_START15 | FSM_START14 | FSM_START13 | FSM_START12 | FSM_START11 | FSM_START10 | FSM_START9 | FSM_START8 |

**Table 370. FSM_START_ADD_H register description**

| | |
|---|---|
| FSM_START[15:8] | FSM start address value (MSbyte). Default value: 00000000 |

### 15.2.4 PEDO_CMD_REG (83h)

Pedometer configuration register (R/W)

**Table 371. PEDO_CMD_REG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | CARRY_COUNT_EN | 0(1) | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 372. PEDO_CMD_REG register description**

| | |
|---|---|
| CARRY_COUNT_EN | Set when user wants to generate interrupt only on count overflow event. |

### 15.2.5 PEDO_DEB_STEPS_CONF (84h)

Pedometer debounce configuration register (R/W)

**Table 373. PEDO_DEB_STEPS_CONF register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DEB_ STEP7 | DEB_ STEP6 | DEB_ STEP5 | DEB_ STEP4 | DEB_ STEP3 | DEB_ STEP2 | DEB_ STEP1 | DEB_ STEP0 |

**Table 374. PEDO_DEB_STEPS_CONF register description**

| | |
|---|---|
| DEB_STEP[7:0] | Debounce threshold. Minimum number of steps to increment the step counter (debounce).<br>Default value: 00001010 |

### 15.2.6 PEDO_SC_DELTAT_L (D0h) and PEDO_SC_DELTAT_H (D1h)

Time period register for step detection on delta time (R/W)

**Table 375. PEDO_SC_DELTAT_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PD_SC_7 | PD_SC_6 | PD_SC_5 | PD_SC_4 | PD_SC_3 | PD_SC_2 | PD_SC_1 | PD_SC_0 |

**Table 376. PEDO_SC_DELTAT_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PD_SC_15 | PD_SC_14 | PD_SC_13 | PD_SC_12 | PD_SC_11 | PD_SC_10 | PD_SC_9 | PD_SC_8 |

**Table 377. PEDO_SC_DELTAT_H/L register description**

| | |
|---|---|
| PD_SC_[15:0] | Time period value (1LSB = 6.4 ms) |

## 15.3 Page 2 - embedded advanced features registers

### 15.3.1 EXT_FORMAT (00h)

External sensor data format (2-byte or 3-byte) for the finite state machine (R/W)

**Table 378. EXT_FORMAT register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | 0(1) | EXT_FORMAT_SEL | 0(1) | 0(1) |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 379. EXT_FORMAT register description**

| | |
|---|---|
| EXT_FORMAT_SEL | Selects the format of the external sensor data for FSM processing. Default value: 0<br>(0: 2-byte format; 1: 3-byte format) |

### 15.3.2 EXT_3BYTE_SENSITIVITY_L (02h) and EXT_3BYTE_SENSITIVITY_H (03h)

External sensor (3-byte output data) sensitivity value register for the finite state machine (R/W)

This register corresponds to the conversion value of the external sensor having 3-byte output data. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

The default value of EXT_3BYTE_S_[15:0] is 0x0C00 (when using an external pressure sensor this value corresponds to 2.441e-04 hPa/LSB).

**Table 380. EXT_3BYTE_SENSITIVITY_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EXT_3BYTE_S_7 | EXT_3BYTE_S_6 | EXT_3BYTE_S_5 | EXT_3BYTE_S_4 | EXT_3BYTE_S_3 | EXT_3BYTE_S_2 | EXT_3BYTE_S_1 | EXT_3BYTE_S_0 |

**Table 381. EXT_3BYTE_SENSITIVITY_L register description**

| | |
|---|---|
| EXT_3BYTE_S_[7:0] | External sensor (3-byte output data) sensitivity (LSbyte). Default value: 00000000 |

**Table 382. EXT_3BYTE_SENSITIVITY_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EXT_3BYTE_S_15 | EXT_3BYTE_S_14 | EXT_3BYTE_S_13 | EXT_3BYTE_S_12 | EXT_3BYTE_S_11 | EXT_3BYTE_S_10 | EXT_3BYTE_S_9 | EXT_3BYTE_S_8 |

**Table 383. EXT_3BYTE_SENSITIVITY_H register description**

| | |
|---|---|
| EXT_3BYTE_S_[15:8] | External sensor (3-byte output data) sensitivity (MSbyte). Default value: 00001100 |

### 15.3.3 EXT_3BYTE_OFFSET_XL (06h), EXT_3BYTE_OFFSET_L (07h) and EXT_3BYTE_OFFSET_H (08h)

External sensor (3-byte output data) offset value register for the finite state machine (R/W)

This register corresponds to the offset value applied to external sensor output data (3-byte) before being processed in the FSM. The value is expressed as a 24-bit word in two's complement.

The default value of EXT_3BYTE_OFF_[23:0] is 0x3F5400, which corresponds to 4150272 LSB. This offset is subtracted from the external output data (in LSB) before the sensitivity (configured in the EXT_3BYTE_SENSITIVITY_L (02h) and EXT_3BYTE_SENSITIVITY_H (03h) registers) is internally applied.

**Table 384. EXT_3BYTE_OFFSET_XL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EXT_3BYTE_OFF_7 | EXT_3BYTE_OFF_6 | EXT_3BYTE_OFF_5 | EXT_3BYTE_OFF_4 | EXT_3BYTE_OFF_3 | EXT_3BYTE_OFF_2 | EXT_3BYTE_OFF_1 | EXT_3BYTE_OFF_0 |

**Table 385. EXT_3BYTE_OFFSET_XL register description**

| | |
|---|---|
| EXT_3BYTE_OFF_[7:0] | External sensor (3-byte output data) offset (low byte). Default value: 00000000 |

**Table 386. EXT_3BYTE_OFFSET_L register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EXT_3BYTE_OFF_15 | EXT_3BYTE_OFF_14 | EXT_3BYTE_OFF_13 | EXT_3BYTE_OFF_12 | EXT_3BYTE_OFF_11 | EXT_3BYTE_OFF_10 | EXT_3BYTE_OFF_9 | EXT_3BYTE_OFF_8 |

**Table 387. EXT_3BYTE_OFFSET_L register description**

| | |
|---|---|
| EXT_3BYTE_OFF_[15:8] | External sensor (3-byte output data) offset (mid byte). Default value: 01010100 |

**Table 388. EXT_3BYTE_OFFSET_H register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EXT_3BYTE_OFF_23 | EXT_3BYTE_OFF_22 | EXT_3BYTE_OFF_21 | EXT_3BYTE_OFF_20 | EXT_3BYTE_OFF_19 | EXT_3BYTE_OFF_18 | EXT_3BYTE_OFF_17 | EXT_3BYTE_OFF_16 |

**Table 389. EXT_3BYTE_OFFSET_H register description**

| | |
|---|---|
| EXT_3BYTE_OFF_[23:16] | External sensor (3-byte output data) offset (high byte). Default value: 00111111 |

# 16 Sensor hub register mapping

The table given below provides a list of the registers for the sensor hub functions available in the device and the corresponding addresses. The sensor hub registers are accessible when bit SHUB_REG_ACCESS is set to 1 in FUNC_CFG_ACCESS (01h).

**Table 390. Register address map - sensor hub registers**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| SENSOR_HUB_1 | R | 02 | 00000010 | output | |
| SENSOR_HUB_2 | R | 03 | 00000011 | output | |
| SENSOR_HUB_3 | R | 04 | 00000100 | output | |
| SENSOR_HUB_4 | R | 05 | 00000101 | output | |
| SENSOR_HUB_5 | R | 06 | 00000110 | output | |
| SENSOR_HUB_6 | R | 07 | 00000111 | output | |
| SENSOR_HUB_7 | R | 08 | 00001000 | output | |
| SENSOR_HUB_8 | R | 09 | 00001001 | output | |
| SENSOR_HUB_9 | R | 0A | 00001010 | output | |
| SENSOR_HUB_10 | R | 0B | 00001011 | output | |
| SENSOR_HUB_11 | R | 0C | 00001100 | output | |
| SENSOR_HUB_12 | R | 0D | 00001101 | output | |
| SENSOR_HUB_13 | R | 0E | 00001110 | output | |
| SENSOR_HUB_14 | R | 0F | 00001111 | output | |
| SENSOR_HUB_15 | R | 10 | 00010000 | output | |
| SENSOR_HUB_16 | R | 11 | 00010001 | output | |
| SENSOR_HUB_17 | R | 12 | 00010010 | output | |
| SENSOR_HUB_18 | R | 13 | 00010011 | output | |
| MASTER_CONFIG | R/W | 14 | 00010100 | 00000000 | |
| SLV0_ADD | R/W | 15 | 00010101 | 00000000 | |
| SLV0_SUBADD | R/W | 16 | 00010110 | 00000000 | |
| SLV0_CONFIG | R/W | 17 | 00010111 | 10000000 | |
| SLV1_ADD | R/W | 18 | 00011000 | 00000000 | |
| SLV1_SUBADD | R/W | 19 | 00011001 | 00000000 | |
| SLV1_CONFIG | R/W | 1A | 00011010 | 00010000 | |
| SLV2_ADD | R/W | 1B | 00011011 | 00000000 | |
| SLV2_SUBADD | R/W | 1C | 00011100 | 00000000 | |
| SLV2_CONFIG | R/W | 1D | 00011101 | 00000000 | |
| SLV3_ADD | R/W | 1E | 00011110 | 00000000 | |
| SLV3_SUBADD | R/W | 1F | 00011111 | 00000000 | |
| SLV3_CONFIG | R/W | 20 | 00100000 | 00000000 | |
| DATAWRITE_SLV0 | R/W | 21 | 00100001 | 00000000 | |
| STATUS_MASTER | R | 22 | 00100010 | output | |

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

# 17 Sensor hub register description

## 17.1 SENSOR_HUB_1 (02h)

Sensor hub output register (R)

First byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 391. SENSOR_HUB_1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub1_7 | Sensor Hub1_6 | Sensor Hub1_5 | Sensor Hub1_4 | Sensor Hub1_3 | Sensor Hub1_2 | Sensor Hub1_1 | Sensor Hub1_0 |

**Table 392. SENSOR_HUB_1 register description**

| | |
|---|---|
| SensorHub1_[7:0] | First byte associated to external sensors |

## 17.2 SENSOR_HUB_2 (03h)

Sensor hub output register (R)

Second byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 393. SENSOR_HUB_2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub2_7 | Sensor Hub2_6 | Sensor Hub2_5 | Sensor Hub2_4 | Sensor Hub2_3 | Sensor Hub2_2 | Sensor Hub2_1 | Sensor Hub2_0 |

**Table 394. SENSOR_HUB_2 register description**

| | |
|---|---|
| SensorHub2_[7:0] | Second byte associated to external sensors |

## 17.3 SENSOR_HUB_3 (04h)

Sensor hub output register (R)

Third byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 395. SENSOR_HUB_3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub3_7 | Sensor Hub3_6 | Sensor Hub3_5 | Sensor Hub3_4 | Sensor Hub3_3 | Sensor Hub3_2 | Sensor Hub3_1 | Sensor Hub3_0 |

**Table 396. SENSOR_HUB_3 register description**

| | |
|---|---|
| SensorHub3_[7:0] | Third byte associated to external sensors |

## 17.4 SENSOR_HUB_4 (05h)

Sensor hub output register (R)

Fourth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 397. SENSOR_HUB_4 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub4_7 | Sensor Hub4_6 | Sensor Hub4_5 | Sensor Hub4_4 | Sensor Hub4_3 | Sensor Hub4_2 | Sensor Hub4_1 | Sensor Hub4_0 |

**Table 398. SENSOR_HUB_4 register description**

| | |
|---|---|
| SensorHub4_[7:0] | Fourth byte associated to external sensors |

## 17.5 SENSOR_HUB_5 (06h)

Sensor hub output register (R)

Fifth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 399. SENSOR_HUB_5 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub5_7 | Sensor Hub5_6 | Sensor Hub5_5 | Sensor Hub5_4 | Sensor Hub5_3 | Sensor Hub5_2 | Sensor Hub5_1 | Sensor Hub5_0 |

**Table 400. SENSOR_HUB_5 register description**

| | |
|---|---|
| SensorHub5_[7:0] | Fifth byte associated to external sensors |

## 17.6 SENSOR_HUB_6 (07h)

Sensor hub output register (R)

Sixth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 401. SENSOR_HUB_6 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub6_7 | Sensor Hub6_6 | Sensor Hub6_5 | Sensor Hub6_4 | Sensor Hub6_3 | Sensor Hub6_2 | Sensor Hub6_1 | Sensor Hub6_0 |

**Table 402. SENSOR_HUB_6 register description**

| | |
|---|---|
| SensorHub6_[7:0] | Sixth byte associated to external sensors |

## 17.7 SENSOR_HUB_7 (08h)

Sensor hub output register (R)

Seventh byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 403. SENSOR_HUB_7 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub7_7 | Sensor Hub7_6 | Sensor Hub7_5 | Sensor Hub7_4 | Sensor Hub7_3 | Sensor Hub7_2 | Sensor Hub7_1 | Sensor Hub7_0 |

**Table 404. SENSOR_HUB_7 register description**

| | |
|---|---|
| SensorHub7_[7:0] | Seventh byte associated to external sensors |

## 17.8 SENSOR_HUB_8 (09h)

Sensor hub output register (R)

Eighth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 405. SENSOR_HUB_8 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub8_7 | Sensor Hub8_6 | Sensor Hub8_5 | Sensor Hub8_4 | Sensor Hub8_3 | Sensor Hub8_2 | Sensor Hub8_1 | Sensor Hub8_0 |

**Table 406. SENSOR_HUB_8 register description**

| | |
|---|---|
| SensorHub8_[7:0] | Eighth byte associated to external sensors |

## 17.9 SENSOR_HUB_9 (0Ah)

Sensor hub output register (R)

Ninth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 407. SENSOR_HUB_9 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub9_7 | Sensor Hub9_6 | Sensor Hub9_5 | Sensor Hub9_4 | Sensor Hub9_3 | Sensor Hub9_2 | Sensor Hub9_1 | Sensor Hub9_0 |

**Table 408. SENSOR_HUB_9 register description**

| | |
|---|---|
| SensorHub9_[7:0] | Ninth byte associated to external sensors |

## 17.10 SENSOR_HUB_10 (0Bh)

Sensor hub output register (R)

Tenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 409. SENSOR_HUB_10 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub10_7 | Sensor Hub10_6 | Sensor Hub10_5 | Sensor Hub10_4 | Sensor Hub10_3 | Sensor Hub10_2 | Sensor Hub10_1 | Sensor Hub10_0 |

**Table 410. SENSOR_HUB_10 register description**

| | |
|---|---|
| SensorHub10_[7:0] | Tenth byte associated to external sensors |

## 17.11 SENSOR_HUB_11 (0Ch)

Sensor hub output register (R)

Eleventh byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 411. SENSOR_HUB_11 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub11_7 | Sensor Hub11_6 | Sensor Hub11_5 | Sensor Hub11_4 | Sensor Hub11_3 | Sensor Hub11_2 | Sensor Hub11_1 | Sensor Hub11_0 |

**Table 412. SENSOR_HUB_11 register description**

| | |
|---|---|
| SensorHub11_[7:0] | Eleventh byte associated to external sensors |

## 17.12 SENSOR_HUB_12 (0Dh)

Sensor hub output register (R)

Twelfth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 413. SENSOR_HUB_12 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub12_7 | Sensor Hub12_6 | Sensor Hub12_5 | Sensor Hub12_4 | Sensor Hub12_3 | Sensor Hub12_2 | Sensor Hub12_1 | Sensor Hub12_0 |

**Table 414. SENSOR_HUB_12 register description**

| | |
|---|---|
| SensorHub12_[7:0] | Twelfth byte associated to external sensors |

## 17.13 SENSOR_HUB_13 (0Eh)

Sensor hub output register (R)

Thirteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 415. SENSOR_HUB_13 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub13_7 | Sensor Hub13_6 | Sensor Hub13_5 | Sensor Hub13_4 | Sensor Hub13_3 | Sensor Hub13_2 | Sensor Hub13_1 | Sensor Hub13_0 |

**Table 416. SENSOR_HUB_13 register description**

| | |
|---|---|
| SensorHub13_[7:0] | Thirteenth byte associated to external sensors |

## 17.14 SENSOR_HUB_14 (0Fh)

Sensor hub output register (R)

Fourteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 417. SENSOR_HUB_14 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub14_7 | Sensor Hub14_6 | Sensor Hub14_5 | Sensor Hub14_4 | Sensor Hub14_3 | Sensor Hub14_2 | Sensor Hub14_1 | Sensor Hub14_0 |

**Table 418. SENSOR_HUB_14 register description**

| | |
|---|---|
| SensorHub14_[7:0] | Fourteenth byte associated to external sensors |

## 17.15 SENSOR_HUB_15 (10h)

Sensor hub output register (R)

Fifteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 419. SENSOR_HUB_15 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub15_7 | Sensor Hub15_6 | Sensor Hub15_5 | Sensor Hub15_4 | Sensor Hub15_3 | Sensor Hub15_2 | Sensor Hub15_1 | Sensor Hub15_0 |

**Table 420. SENSOR_HUB_15 register description**

| | |
|---|---|
| SensorHub15_[7:0] | Fifteenth byte associated to external sensors |

## 17.16 SENSOR_HUB_16 (11h)

Sensor hub output register (R)

Sixteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 421. SENSOR_HUB_16 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub16_7 | Sensor Hub16_6 | Sensor Hub16_5 | Sensor Hub16_4 | Sensor Hub16_3 | Sensor Hub16_2 | Sensor Hub16_1 | Sensor Hub16_0 |

**Table 422. SENSOR_HUB_16 register description**

| | |
|---|---|
| SensorHub16_[7:0] | Sixteenth byte associated to external sensors |

## 17.17 SENSOR_HUB_17 (12h)

Sensor hub output register (R)

Seventeenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 423. SENSOR_HUB_17 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub17_7 | Sensor Hub17_6 | Sensor Hub17_5 | Sensor Hub17_4 | Sensor Hub17_3 | Sensor Hub17_2 | Sensor Hub17_1 | Sensor Hub17_0 |

**Table 424. SENSOR_HUB_17 register description**

| | |
|---|---|
| SensorHub17_[7:0] | Seventeenth byte associated to external sensors |

## 17.18 SENSOR_HUB_18 (13h)

Sensor hub output register (R)

Eighteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 425. SENSOR_HUB_17 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Sensor Hub18_7 | Sensor Hub18_6 | Sensor Hub18_5 | Sensor Hub18_4 | Sensor Hub18_3 | Sensor Hub18_2 | Sensor Hub18_1 | Sensor Hub18_0 |

**Table 426. SENSOR_HUB_17 register description**

| | |
|---|---|
| SensorHub18_[7:0] | Eighteenth byte associated to external sensors |

## 17.19 MASTER_CONFIG (14h)

Master configuration register (R/W)

**Table 427. MASTER_CONFIG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| RST_MASTER_REGS | WRITE_ONCE | START_CONFIG | PASS_THROUGH_MODE | 0(1) | MASTER_ON | AUX_SENS_ON1 | AUX_SENS_ON0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 428. MASTER_CONFIG register description**

| | |
|---|---|
| RST_MASTER_REGS | Resets master logic and output registers. Must be set to 1 and then set to 0. Default value: 0 |
| WRITE_ONCE | Slave 0 write operation is performed only at the first sensor hub cycle.<br>Default value: 0<br>(0: write operation for each sensor hub cycle;<br>1: write operation only for the first sensor hub cycle) |
| START_CONFIG | Sensor hub trigger signal selection. Default value: 0<br>(0: sensor hub trigger signal is the accelerometer/gyro data-ready;<br>1: sensor hub trigger signal external from INT2 pin) |
| PASS_THROUGH_MODE | I²C interface pass-through. Default value: 0<br>(0: pass-through disabled;<br>1: pass-through enabled, primary I²C line is short-circuited with the sensor hub line) |
| MASTER_ON | Enables sensor hub I²C master. Default: 0<br>(0: master I²C of sensor hub disabled; 1: master I²C of sensor hub enabled) |
| AUX_SENS_ON[1:0] | Number of external sensors to be read by the sensor hub.<br>(00: one sensor (default);<br>01: two sensors;<br>10: three sensors;<br>11: four sensors) |

## 17.20 SLV0_ADD (15h)

I²C slave address of the first external sensor (sensor 0) register (R/W)

**Table 429. SLV0_ADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| slave0_add6 | slave0_add5 | slave0_add4 | slave0_add3 | slave0_add2 | slave0_add1 | slave0_add0 | rw_0 |

**Table 430. SLV_ADD register description**

| | |
|---|---|
| slave0_add[6:0] | I²C slave address of sensor 0 that can be read by the sensor hub.<br>Default value: 0000000 |
| rw_0 | Read/write operation on sensor 0. Default value: 0<br>(0: write operation; 1: read operation) |

## 17.21 SLV0_SUBADD (16h)

Address of register on the first external sensor (sensor 0) register (R/W)

**Table 431. SLV0_SUBADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| slave0_reg7 | slave0_reg6 | slave0_reg5 | slave0_reg4 | slave0_reg3 | slave0_reg2 | slave0_reg1 | slave0_reg0 |

**Table 432. SLV0_SUBADD register description**

| | |
|---|---|
| slave0_reg[7:0] | Address of register on sensor 0 that has to be read/written according to the rw_0 bit value in SLV0_ADD (15h). Default value: 00000000 |

## 17.22 SLV0_CONFIG (17h)

First external sensor (sensor 0) configuration and sensor hub settings register (R/W)

**Table 433. SLV0_CONFIG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SHUB_ ODR_2 | SHUB_ ODR_1 | SHUB_ ODR_0 | 0(1) | BATCH_EXT_ SENS_0_EN | Slave0_ numop2 | Slave0_ numop1 | Slave0_ numop0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 434. SLV0_CONFIG register description**

| | |
|---|---|
| SHUB_ODR_[2:0] | Rate at which the master communicates.<br>(000: 1.875 Hz;<br>001: 15 Hz;<br>010: 30 Hz;<br>011: 60 Hz;<br>100: 120 Hz (default);<br>101: 240 Hz;<br>110: 480 Hz;<br>111: reserved |
| BATCH_EXT_SENS_0_EN | Enables FIFO data batching of first slave. Default value: 0 |
| Slave0_numop[2:0] | Number of read operations on sensor 0. Default value: 000 |

## 17.23 SLV1_ADD (18h)

I²C slave address of the second external sensor (sensor 1) register (R/W)

**Table 435. SLV1_ADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave1_add6 | Slave1_add5 | Slave1_add4 | Slave1_add3 | Slave1_add2 | Slave1_add1 | Slave1_add0 | r_1 |

**Table 436. SLV1_ADD register description**

| | |
|---|---|
| Slave1_add[6:0] | I²C slave address of sensor 1 that can be read by the sensor hub.<br>Default value: 0000000 |
| r_1 | Enables read operation on sensor 1. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

## 17.24 SLV1_SUBADD (19h)

Address of register on the second external sensor (sensor 1) register (R/W)

**Table 437. SLV1_SUBADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave1_reg7 | Slave1_reg6 | Slave1_reg5 | Slave1_reg4 | Slave1_reg3 | Slave1_reg2 | Slave1_reg1 | Slave1_reg0 |

**Table 438. SLV1_SUBADD register description**

| | |
|---|---|
| Slave1_reg[7:0] | Address of register on sensor 1 that has to be read/written according to the r_1 bit value in SLV1_ADD (18h). |

## 17.25 SLV1_CONFIG (1Ah)

Second external sensor (sensor 2) configuration register (R/W)

**Table 439. SLV1_CONFIG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 1(2) | BATCH_EXT_SENS_1_EN | Slave1_numop2 | Slave1_numop1 | Slave1_numop0 |

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

**Table 440. SLV1_CONFIG register description**

| | |
|---|---|
| BATCH_EXT_SENS_1_EN | Enables FIFO data batching of second slave. Default value: 0 |
| Slave1_numop[2:0] | Number of read operations on sensor 2. Default value: 000 |

## 17.26 SLV2_ADD (1Bh)

I²C slave address of the third external sensor (sensor 2) register (R/W)

**Table 441. SLV2_ADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave2_add6 | Slave2_add5 | Slave2_add4 | Slave2_add3 | Slave2_add2 | Slave2_add1 | Slave2_add0 | r_2 |

**Table 442. SLV2_ADD register description**

| | |
|---|---|
| Slave2_add[6:0] | I²C slave address of sensor 2 that can be read by the sensor hub. |
| r_2 | Enables read operation on sensor 2. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

## 17.27 SLV2_SUBADD (1Ch)

Address of register on the third external sensor (sensor 2) register (R/W)

**Table 443. SLV2_SUBADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave2_reg7 | Slave2_reg6 | Slave2_reg5 | Slave2_reg4 | Slave2_reg3 | Slave2_reg2 | Slave2_reg1 | Slave2_reg0 |

**Table 444. SLV2_SUBADD register description**

| | |
|---|---|
| Slave2_reg[7:0] | Address of register on sensor 2 that has to be read/written according to the r_2 bit value in SLV2_ADD (1Bh). |

## 17.28 SLV2_CONFIG (1Dh)

Third external sensor (sensor 2) configuration register (R/W)

**Table 445. SLV2_CONFIG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | BATCH_EXT_SENS_2_EN | Slave2_numop2 | Slave2_numop1 | Slave2_numop0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 446. SLV2_CONFIG register description**

| | |
|---|---|
| BATCH_EXT_SENS_2_EN | Enables FIFO data batching of third slave. Default value: 0 |
| Slave2_numop[2:0] | Number of read operations on sensor 2. Default value: 000 |

## 17.29 SLV3_ADD (1Eh)

I²C slave address of the fourth external sensor (sensor 3) register (R/W)

**Table 447. SLV3_ADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave3_add6 | Slave3_add5 | Slave3_add4 | Slave3_add3 | Slave3_add2 | Slave3_add1 | Slave3_add0 | r_3 |

**Table 448. SLV3_ADD register description**

| | |
|---|---|
| Slave3_add[6:0] | I²C slave address of sensor 3 that can be read by the sensor hub. |
| r_3 | Enables read operation on sensor 3. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

## 17.30 SLV3_SUBADD (1Fh)

Address of register on the fourth external sensor (sensor 3) register (R/W)

**Table 449. SLV3_SUBADD register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave3_reg7 | Slave3_reg6 | Slave3_reg5 | Slave3_reg4 | Slave3_reg3 | Slave3_reg2 | Slave3_reg1 | Slave3_reg0 |

**Table 450. SLV3_SUBADD register description**

| | |
|---|---|
| Slave3_reg[7:0] | Address of register on sensor 3 that has to be read according to the r_3 bit value in SLV3_ADD (1Eh). |

## 17.31 SLV3_CONFIG (20h)

Fourth external sensor (sensor 3) configuration register (R/W)

**Table 451. SLV3_CONFIG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | 0(1) | 0(1) | BATCH_EXT_SENS_3_EN | Slave3_numop2 | Slave3_numop1 | Slave3_numop0 |

1. *This bit must be set to 0 for the correct operation of the device.*

**Table 452. SLV3_CONFIG register description**

| | |
|---|---|
| BATCH_EXT_SENS_3_EN | Enables FIFO data batching of fourth slave. Default value: 0 |
| Slave3_numop[2:0] | Number of read operations on sensor 3. Default value: 000 |

## 17.32 DATAWRITE_SLV0 (21h)

Data to be written into the slave device register (R/W)

**Table 453. DATAWRITE_SLV0 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Slave0_ dataw7 | Slave0_ dataw6 | Slave0_ dataw5 | Slave0_ dataw4 | Slave0_ dataw3 | Slave0_ dataw2 | Slave0_ dataw1 | Slave0_ dataw0 |

**Table 454. DATAWRITE_SLV0 register description**

| | |
|---|---|
| Slave0_dataw[7:0] | Data to be written into the slave 0 device according to the rw_0 bit in register SLV0_ADD (15h).<br>Default value: 00000000 |

## 17.33 STATUS_MASTER (22h)

Sensor hub source register (R)

**Table 455. STATUS_MASTER register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| WR_ONCE _DONE | SLAVE3_ NACK | SLAVE2_ NACK | SLAVE1_ NACK | SLAVE0_ NACK | 0 | 0 | SENS_HUB _ENDOP |

**Table 456. STATUS_MASTER register description**

| | |
|---|---|
| WR_ONCE_DONE | When the bit WRITE_ONCE in MASTER_CONFIG (14h) is configured as 1, this bit is set to 1 when the write operation on slave 0 has been performed and completed. Default value: 0 |
| SLAVE3_NACK | This bit is set to 1 if Not acknowledge occurs on slave 3 communication. Default value: 0 |
| SLAVE2_NACK | This bit is set to 1 if Not acknowledge occurs on slave 2 communication. Default value: 0 |
| SLAVE1_NACK | This bit is set to 1 if Not acknowledge occurs on slave 1 communication. Default value: 0 |
| SLAVE0_NACK | This bit is set to 1 if Not acknowledge occurs on slave 0 communication. Default value: 0 |
| SENS_HUB_ENDOP | Sensor hub communication status. Default value: 0<br>(0: sensor hub communication not concluded;<br>1: sensor hub communication concluded) |

# 18 Soldering information

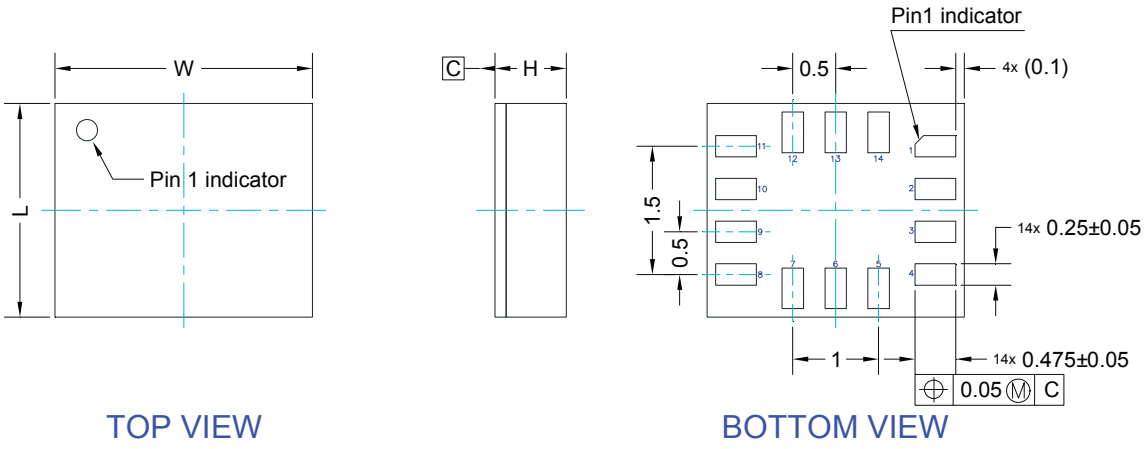
The LGA package is compliant with the ECOPACK and RoHS standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.
For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

# 19 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 19.1 LGA-14L package information

**Figure 31. LGA-14L 2.5 x 3.0 x 0.86 mm package outline and mechanical data**




Dimensions are in millimeter unless otherwise specified
General tolerance is +/-0.1mm unless otherwise specified

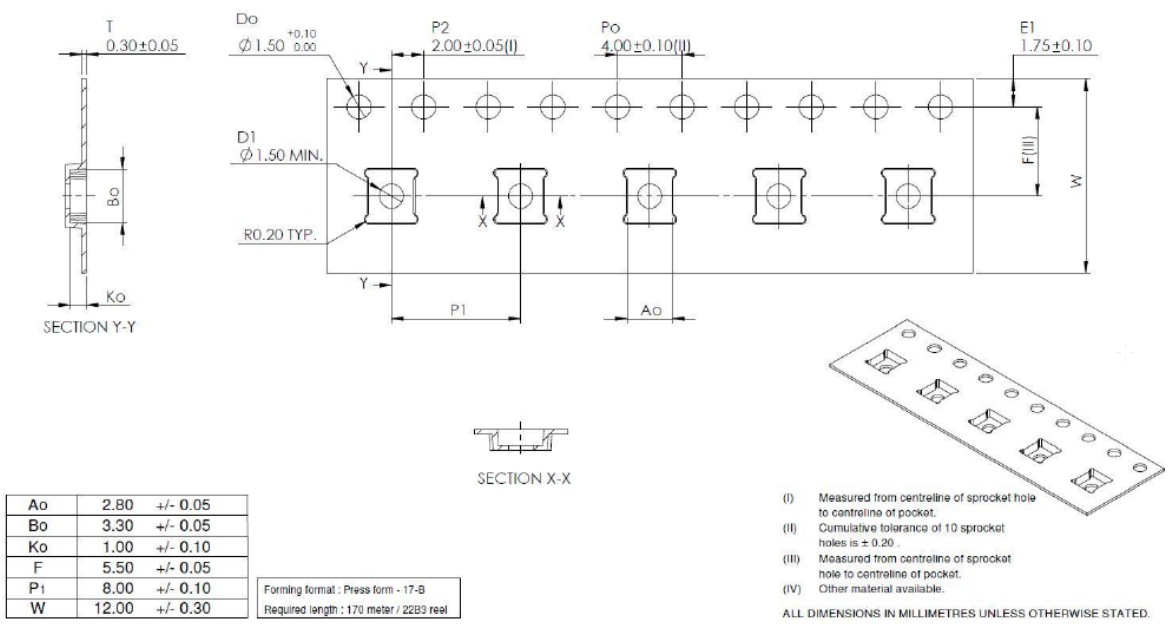
OUTER DIMENSIONS

| ITEM | DIMENSION [mm] | TOLERANCE [mm] |
|---|---|---|
| Length [L] | 2.50 | ±0.1 |
| Width [W] | 3.00 | ±0.1 |
| Height [H] | 0.86 | MAX |

DM00249496_5

## 19.2 LGA-14 packing information

Figure 32. **Carrier tape information for LGA-14 package**




| | | |
|---|---|---|
| Ao | 2.80 | +/- 0.05 |
| Bo | 3.30 | +/- 0.05 |
| Ko | 1.00 | +/- 0.10 |
| F | 5.50 | +/- 0.05 |
| P1 | 8.00 | +/- 0.10 |
| W | 12.00 | +/- 0.30 |

Forming format : Press form - 17-B
Required length : 170 meter / 22B3 reel

Figure 33. **LGA-14 package orientation in carrier tape**

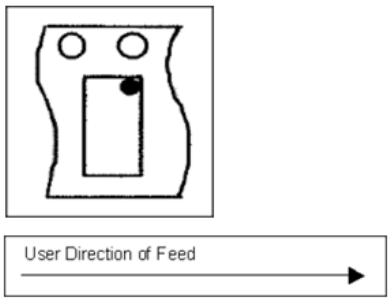


Figure 34. **Reel information for carrier tape of LGA-14 package**

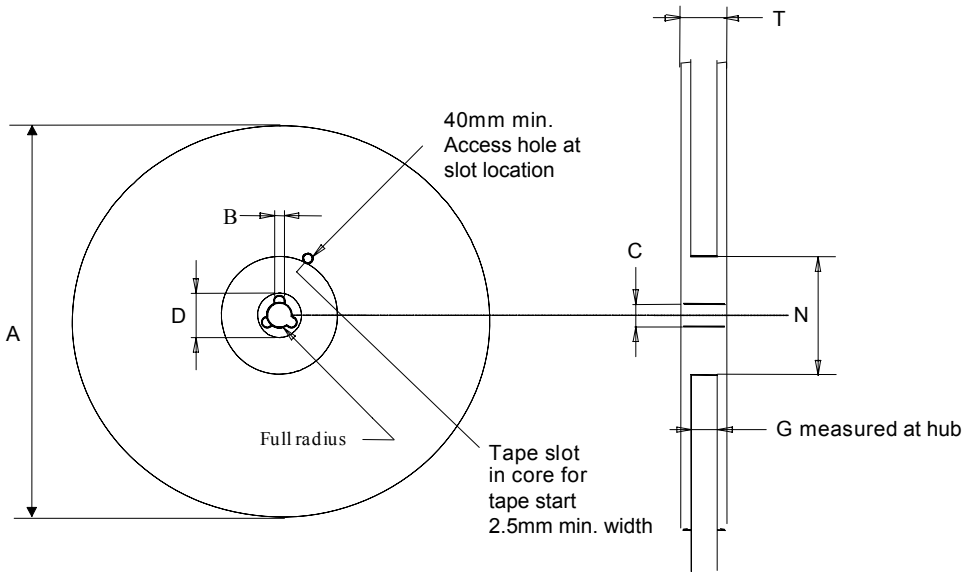



Table 457. **Reel dimensions for carrier tape of LGA-14 package**

| Reel dimensions (mm) | |
|---|---|
| A (max) | 330 |
| B (min) | 1.5 |
| C | 13 ±0.25 |
| D (min) | 20.2 |
| N (min) | 60 |
| G | 12.4 +2/-0 |
| T (max) | 18.4 |

# Revision history

Table 458. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 15-Jul-2022 | 2 | First public release |

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