## GENERAL DESCRIPTION

The MC3635 is an ultra-low power, low-noise, integrated digital output 3-axis accelerometer with a feature set optimized for wearables and consumer product motion sensing. Applications include wearable consumer products, IoT devices, user interface control, gaming motion input, electronic compass tilt compensation for cell phones, game controllers, remote controls and portable media products.

Low noise and low power are inherent in the monolithic fabrication approach, where the MEMS accelerometer is integrated in a single-chip with the electronics integrated circuit.

In the MC3635 the internal sample rate can be set from 14 to 1300 samples / second. Specific tap or sample acquisition conditions can trigger an interrupt to a remote MCU. Alternatively, the device supports the reading of sample and event status via polling.

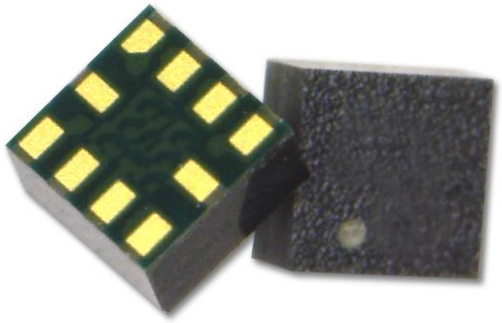
## FEATURES

### Range, Sampling & Power

- ±2, 4, 8, 12 or 16g ranges
- 8, 10 or 12-bit resolution with FIFO
  - 14-bit single samples
- Sample rate 14 - 1300 samples/sec
  - Sample trigger via internal oscillator, clock pin or software command
- Sniff and Wake modes
  - 0.3 µA Sniff current @ 1Hz
  - Separate or combined sniff/wake
- Ultra-Low Power with 32 sample FIFO
  - 0.9 µA typical current @ 25Hz
  - 1.6 µA typical current @ 50Hz
  - 2.8 µA typical current @ 100Hz
  - 36 µA typical current @ 1300Hz

### Simple System Integration

- I2C interface, up to 1 MHz
- SPI Interface, up to 8 MHz
- 1.6 × 1.6 × 0.94 mm 10-pin package
- Single-chip 3D silicon MEMS
- Low noise to 2.3mgRMS
- ROHS Compliant



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# 1 ORDER INFORMATION

**Table 1. Order Information**

| Part Number | Resolution | Order Number | Package | Shipping |
|---|---|---|---|---|
| MC3635 | 8 to 14-bit | MC3635 | LGA-10 | Tape & Reel, 5Ku |

**Table 2. Top Marking Specification**




| Row | Marking |
|---|---|
| CCC | Factory lot code |
| XX | Device identifier |
| ● | Pin1 identifier |

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# 2 FUNCTIONAL BLOCK DIAGRAM

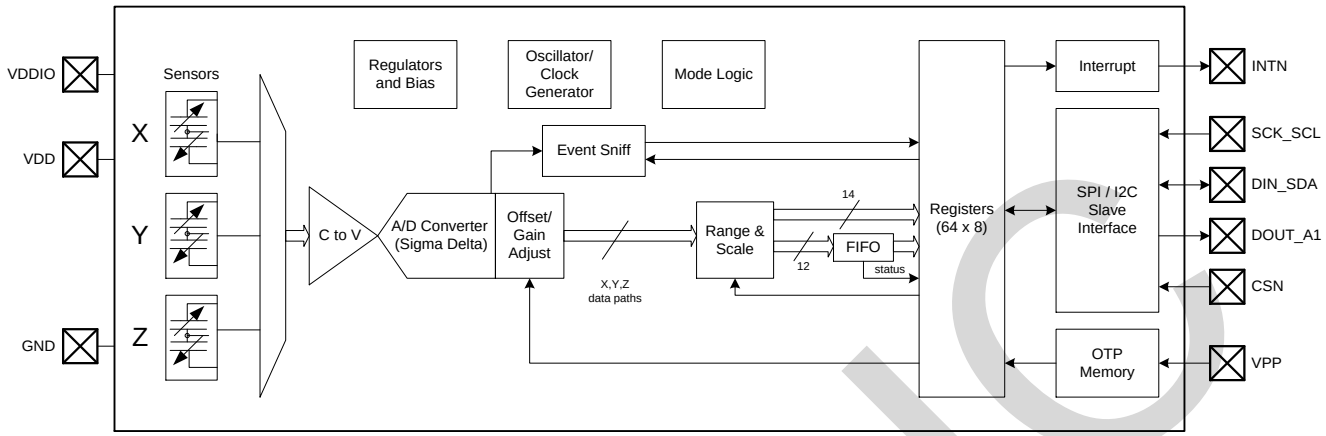
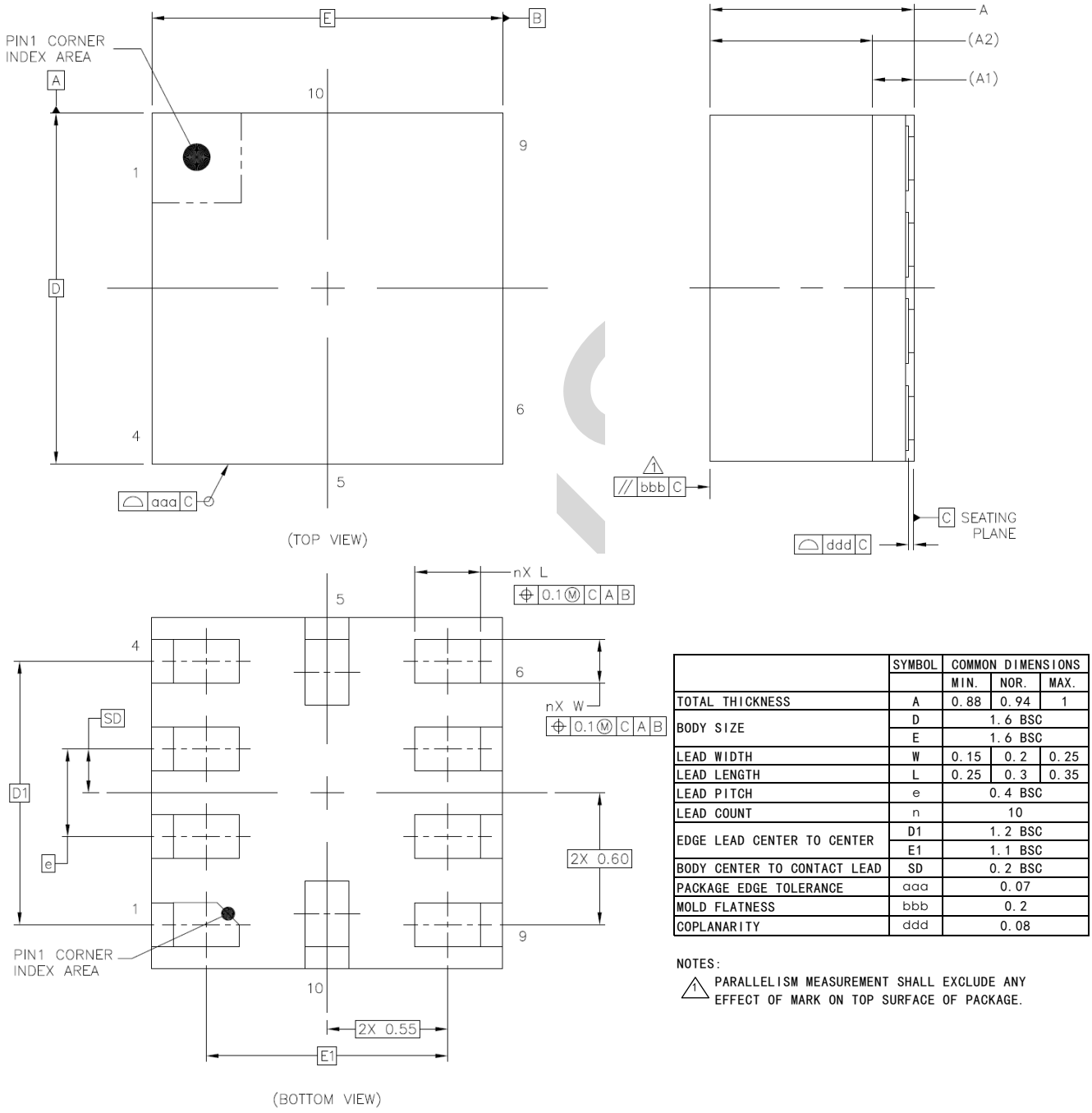



**Figure 1. Block Diagram**

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# 3 PACKAGING AND PIN DESCRIPTION

## 3.1 PACKAGE OUTLINE




| | SYMBOL | COMMON DIMENSIONS | | |
|---|---|---|---|---|
| | | MIN. | NOR. | MAX. |
| TOTAL THICKNESS | A | 0.88 | 0.94 | 1 |
| BODY SIZE | D | 1.6 BSC | | |
| | E | 1.6 BSC | | |
| LEAD WIDTH | W | 0.15 | 0.2 | 0.25 |
| LEAD LENGTH | L | 0.25 | 0.3 | 0.35 |
| LEAD PITCH | e | 0.4 BSC | | |
| LEAD COUNT | n | 10 | | |
| EDGE LEAD CENTER TO CENTER | D1 | 1.2 BSC | | |
| | E1 | 1.1 BSC | | |
| BODY CENTER TO CONTACT LEAD | SD | 0.2 BSC | | |
| PACKAGE EDGE TOLERANCE | aaa | 0.07 | | |
| MOLD FLATNESS | bbb | 0.2 | | |
| COPLANARITY | ddd | 0.08 | | |

NOTES:
1. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

**Figure 2. Package Outline and Mechanical Dimensions**

## 3.2 PACKAGE ORIENTATION

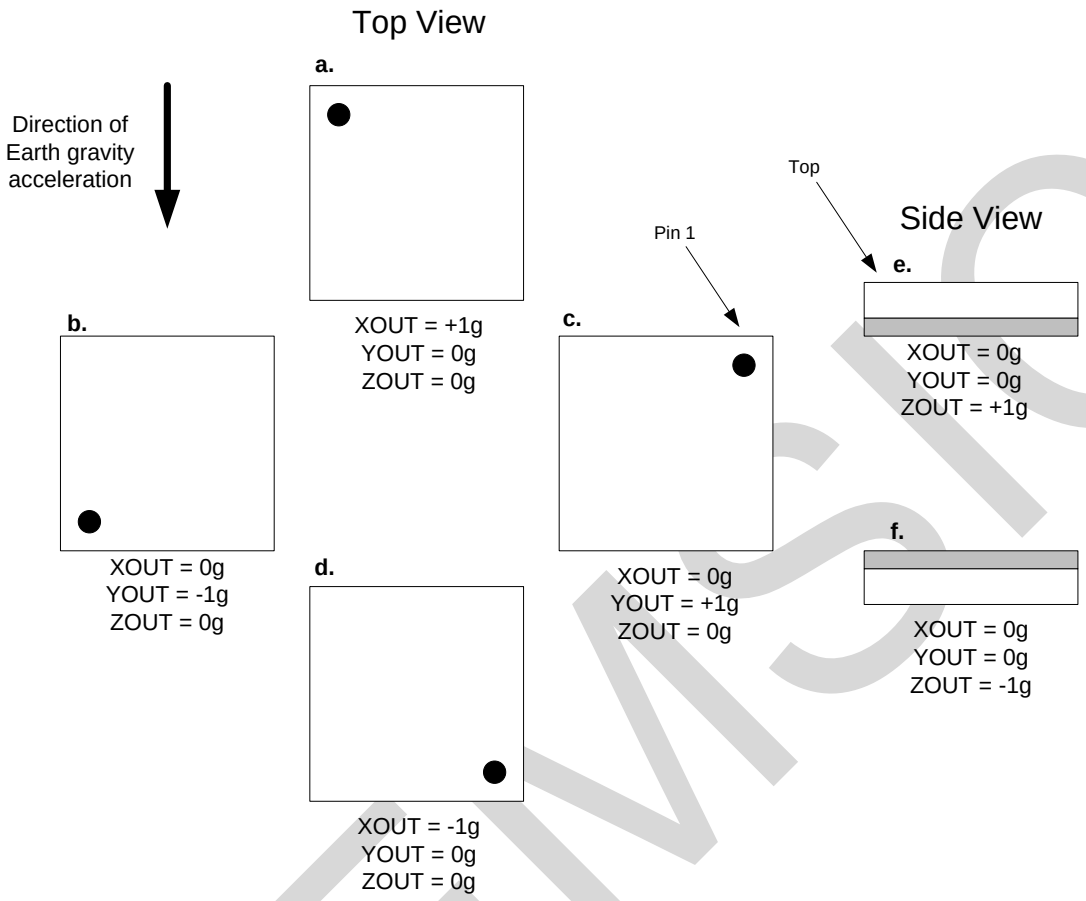



**Figure 3. Package Orientation**

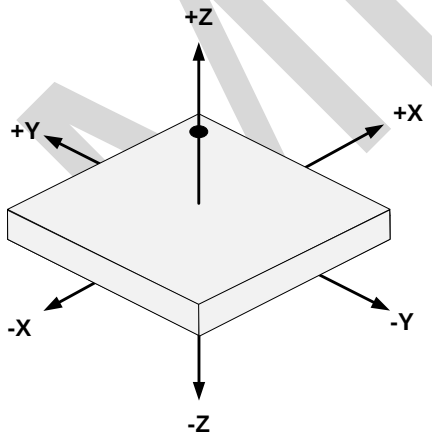



**Figure 4. Package Axis Reference**

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## 3.3 PIN DESCRIPTION

| Pin | Name | Function |
|---|---|---|
| 1 | DOUT_A1 | SPI data output<br>I2C address bit 1 |
| 2 | DIN_SDA [1] | SPI data In<br>I2C serial data input/output |
| 3 | NC | No connect |
| 4 | VPP | Connect to GND |
| 5 | INTN [2] | Interrupt active LOW [3] |
| 6 | VDDIO | Power supply for interface |
| 7 | VDD | Power supply for internal |
| 8 | GND | Ground |
| 9 | CSN | SPI Chip Select |
| 10 | SCK_SCL [1] | SPI Clock<br>I2C serial clock input |

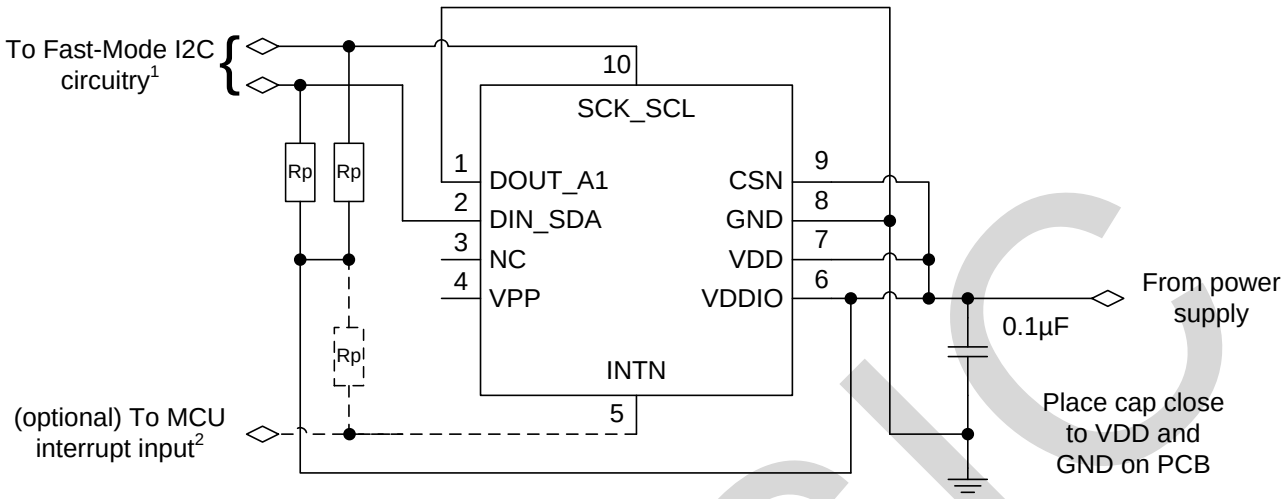
**Table 3. Pin Description**

Notes:

1) When using the I2C interface, this pin requires a pull-up resistor, typically 4.7kΩ to pin VDDIO. Refer to I2C Specification for Fast-Mode devices. Higher resistance values can be used (typically done to reduce current leakage) but such applications are outside the scope of this datasheet.
2) This pin can be configured by software to operate either as an open-drain output or push-pull output. If set to open-drain, then it requires a pull-up resistor, typically 4.7kΩ to pin VDDIO.
3) INTN pin polarity is programmable.

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## 3.4 TYPICAL APPLICATION CIRCUITS

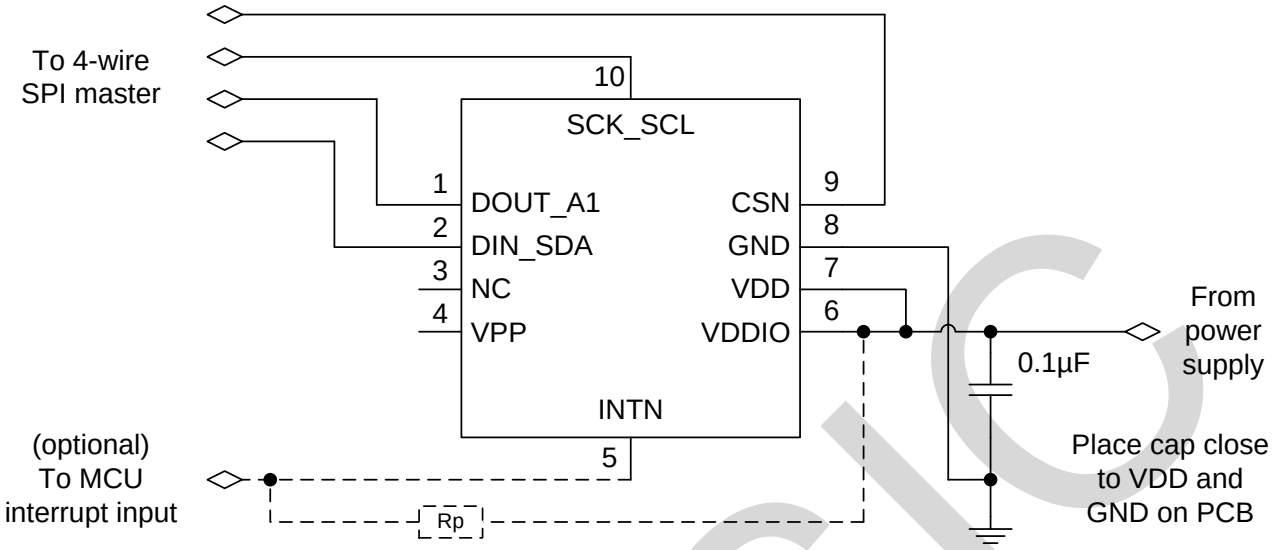



NOTE[1]: Rp are typically 4.7kΩ pullup resistors to VDDIO, per I2C specification. When VDDIO is powered down, DIN_SDA and SCK_SCL will be driven low by internal ESD diodes.
NOTE[2]: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

**Figure 5. Typical I2C Application Circuit**

In typical applications, the interface power supply may contain significant noise from external sources and other circuits which should be kept away from the device. Therefore, for some applications a lower-noise power supply might be desirable to power the device.

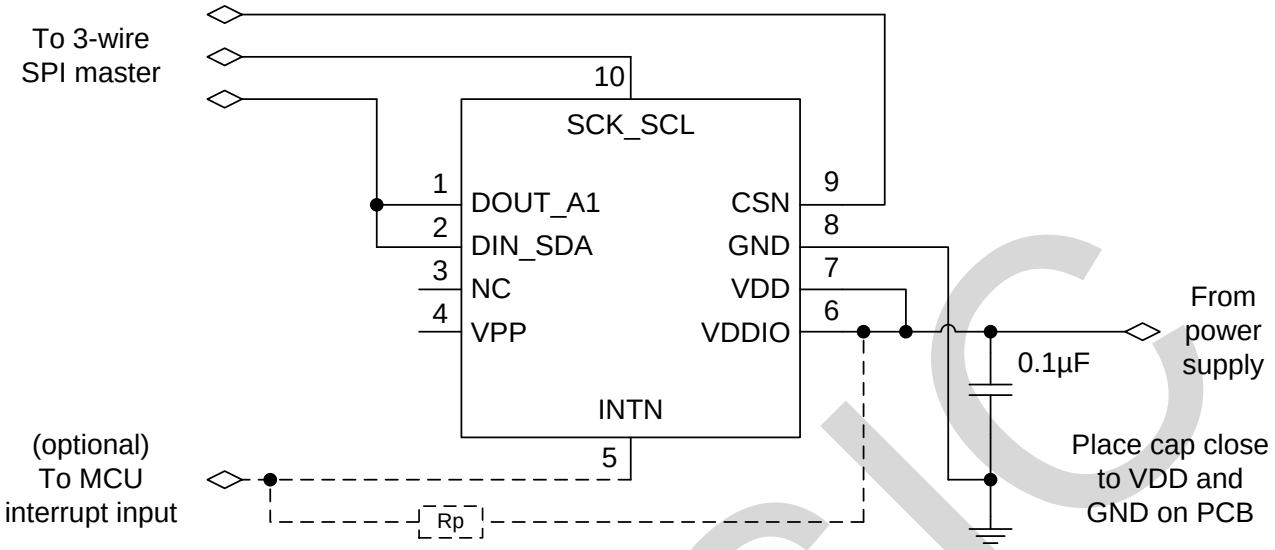
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NOTE Rp: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

**Figure 6. Typical 4-wire SPI Application Circuit**

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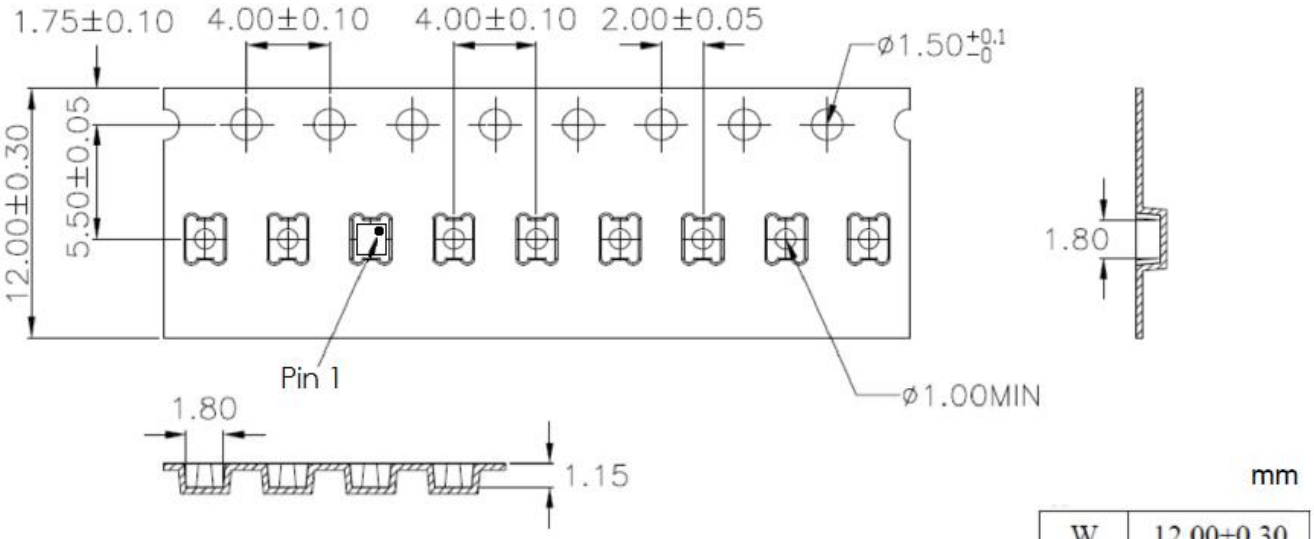

NOTE Rp: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

**Figure 7. Typical 3-wire SPI Application Circuit**

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## 3.5 TAPE AND REEL

Devices are shipped in reels, in standard cardboard box packaging. See Figure 8. MC3635 Tape Dimensions and Figure 9. MC3635 Reel Dimensions.

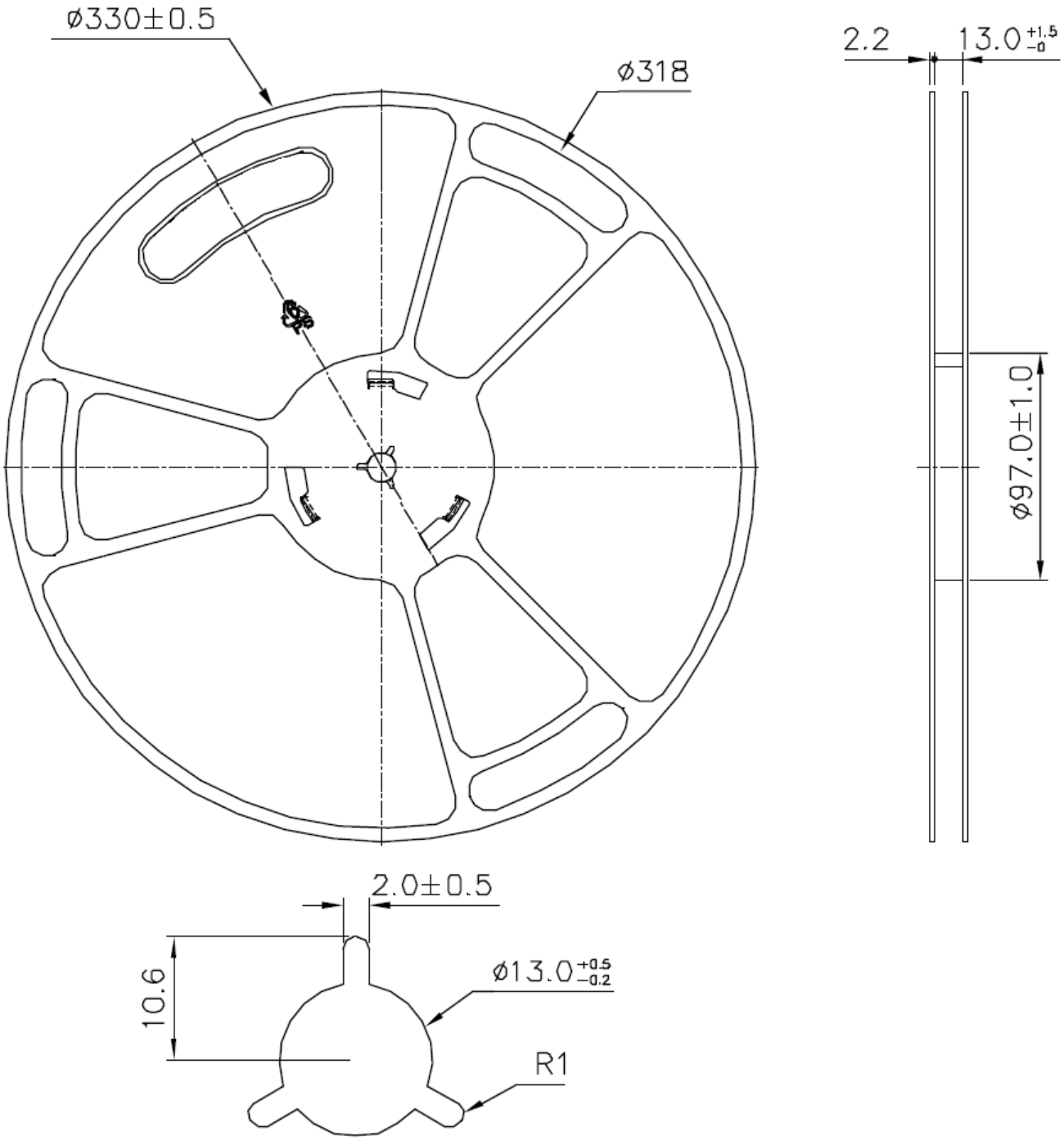



mm

| | |
|---|---|
| W | 12.00±0.30 |
| A0 | 1.80±0.05 |
| B0 | 1.80±0.05 |
| K0 | 1.15±0.10 |

**Figure 8. MC3635 Tape Dimensions**

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- Dimensions in mm.

**Figure 9. MC3635 Reel Dimensions**

## 3.6 SOLDERING PROFILE

The LGA package follows the reflow soldering classification profiles described in *Joint Industry Standard, Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices*, document number J-STD-020E. Reflow soldering has a peak temperature ($T_p$) of $260^0$C

## 3.7 SHIPPING AND HANDLING GUIDELINES

Shipping and handling follow the standards described in *Joint Industry Standard, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*, document number J-STD-033C.

The following are additional handling guidelines (refer to the MEMSIC document, PCB Design, Device Handling and Assembly Guidelines, for more information):

- While the mechanical sensor is designed to handle high-g shock events, direct mechanical shock to the package should be avoided.
- SMT assembly houses should use automated assembly equipment with either plastic nozzles or nozzles with compliant tips (for example, soft rubber or silicone).
- Avoid g-forces beyond the specified limits during transportation.
- Handling and mounting of sensors should be done in a defined and qualified installation.

## 3.8 MOISTURE SENSITIVITY LEVEL CONTROL

The Moisture Sensitivity Level, MSL, for MC3635 (10-pin LGA package) is MSL3.

Refer to IPC/JEDEC J-STD-020D.1 “Joint Industry Standard: Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices” and IPC/JEDEC J STD033A “Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.”

The following are storage recommendations (refer to the MEMSIC document, PCB Design, Device Handling and Assembly Guidelines, for more information):

- Store the tape and reel in the *unopened* dry pack, until required on the assembly floor.
- If the dry pack has been opened or the reel has been removed from the dry pack, reseal the reel inside of the dry pack with a black protective belt. Avoid crushing the tape and reel.
- Store the cardboard box in a vertical position.

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# 4 SPECIFICATIONS

## 4.1 ABSOLUTE MAXIMUM RATINGS

Parameters exceeding the Absolute Maximum Ratings may permanently damage the device.

| Rating | Symbol | Minimum / Maximum Value | Unit |
|---|---|---|---|
| Supply Voltages | Pins VDD, VDDIO | -0.3 / +3.6 | V |
| Acceleration, any axis, 100 µs | $g_{MAX}$ | 10000 | g |
| Ambient operating temperature | $T_{OP}$ | -40 / +85 | $^0$C |
| Storage temperature | $T_{STG}$ | -40 / +125 | $^0$C |
| ESD human body model | HBM | ± 2000 | V |
| Input voltage to non-power pin | Pins CSN, DIN_SDA, DOUT_A1, INTN, and SCK_SCL | -0.3 / (VDDIO + 0.3) or 3.6 whichever is lower | V |

**Table 4. Absolute Maximum Ratings**

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## 4.2 SENSOR CHARACTERISTICS

VDD = VDDIO = 1.8V, $T_{op}$ = 25 $^0$C unless otherwise noted

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Acceleration range | | | ±2<br>±4<br>±8<br>±12<br>±16 | | g |
| Sensitivity | | 8 | | 4096 | LSB/g |
| Sensitivity Temperature Coefficient [1] | | | 0.015 | | %/$^0$C |
| Zero-g Offset | Post-board mount, ODR <= 400Hz | | ± 40 | | mg |
| Zero-g Offset Temperature Coefficient [1] | | | ± 1 | | mg/$^0$C |
| Noise [1] @ 100Hz | **WAKE MODES:**<br>Ultra-Low Power, Avg X&Y&Z:<br>Low Power, Avg X&Y&Z:<br>Precision, Avg X&Y&Z:<br>**SNIFF MODES:**<br>Ultra-Low Power, Avg X&Y&Z:<br>Low Power, Avg X&Y&Z:<br>Precision, Avg X&Y&Z: | | <br>6.5<br>4.4<br>1.7<br><br>40<br>25<br>5 | | mg RMS |
| Nonlinearity [1] | | | 1 | | % FS |
| Cross-axis Sensitivity [1] | Between any two axes | | 2 | | % |

**Table 5. Sensor Characteristics**

[1] Values are based on device characterization, not tested in production.

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## 4.3 ELECTRICAL AND TIMING CHARACTERISTICS

### 4.3.1 ELECTRICAL POWER AND INTERNAL CHARACTERISTICS

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Internal voltage [2] | Pin VDD<br>Rise-time < 40mSec | VDD | 1.7 | 1.8 | 3.6 | V |
| I/O voltage | Pin VDDIO<br>Rise-time < 40mSec | VDDIO | 1.7 | 1.8 | 3.6 | V |

Test condition: VDD = VDDIO = 1.8V, $T_{op}$ = 25 $^{0}$C unless otherwise noted

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Sleep current | | $I_{ddslp}$ | | 0.1 | | µA |
| Sniff current | 1Hz | $I_{ddsnf}$ | | 0.3 | | µA |
| | 6Hz | | | 0.4 | | µA |
| Selected wake supply current (see also 7.11) | Precision, 14Hz | $I_{dd14p}$ | | 5 | | µA |
| | Ultra-Low Power, 25Hz | $I_{dd25ulp}$ | | 0.9 | | |
| | Ultra-Low Power, 50Hz | $I_{dd50ulp}$ | | 1.6 | | |
| | Low Power, 54Hz | $I_{dd54lp}$ | | 2.7 | | |
| | Precision, 55Hz | $I_{dd55p}$ | | 18 | | |
| | Ultra-Low Power, 100Hz | $I_{dd100ulp}$ | | 2.8 | | |
| | Precision, 100Hz | $I_{dd100p}$ | | 36 | | |
| | Low Power, 210Hz | $I_{dd210lp}$ | | 11 | | |
| | Ultra-Low Power, 1300Hz | $I_{dd1300ulp}$ | | 36 | | |
| Pad Leakage | Per I/O pad | $I_{pad}$ | | 0.01 | | µA |

**Table 6. Electrical Characteristics – Voltage and Current**

[2] Min and Max limits are hard limits without additional tolerance.

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### 4.3.2 ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| LOW level input voltage | VIL | -0.5 | 0.3*VDDIO | V |
| HIGH level input voltage | VIH | 0.7*VDDIO | - | V |
| Hysteresis of Schmitt trigger inputs | Vhys | 0.05*VDDIO | - | V |
| Output voltage, pin INTN, Iol ≤ 2 mA | Vol | 0 | 0.4 | V |
| | Voh | 0 | 0.9*VDDIO | V |
| Output voltage, pin DIN_SDA (open drain), Iol ≤ 1 mA | Vols | - | 0.1*VDDIO | V |
| Input current, pins DIN_SDA and SCK_SCL (input voltage between 0.1*VDDIO and 0.9*VDDIO max) | Ii | -10 | 10 | µA |
| Capacitance, pins DIN_SDA and SCK_SCL [3] | Ci | - | 10 | pF |

**Table 7. Electrical Characteristics – Interface**

NOTES:

- If multiple slaves are connected to the I2C signals in addition to this device, only 1 pull-up resistor on each of SDA and SCL should exist. Also, care must be taken to not violate the I2C specification for capacitive loading.
- When pin VDDIO is not powered and set to 0V, INTN, DIN_SDA and SCK_SCL will be held to VDDIO plus the forward voltage of the internal static protection diodes, typically about 0.6V.
- When pin VDDIO is disconnected from power or ground (e.g. Hi-Z), the device may become inadvertently powered up through the ESD diodes present on other powered signals.

[3] Values are based on device characterization, not tested in production.

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### 4.3.3 I2C TIMING CHARACTERISTICS

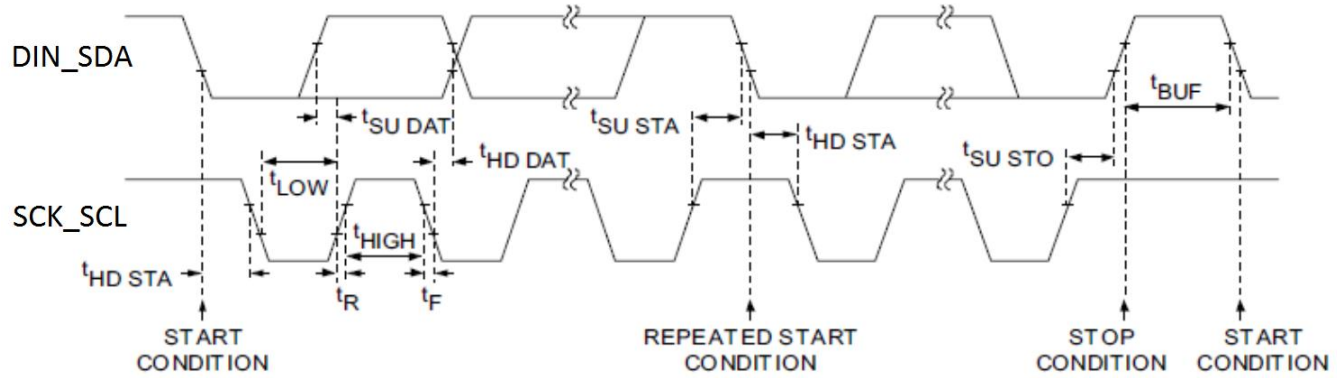



**Figure 10. I2C Interface Timing**

| Parameter | Description | Standard Mode | | Fast Mode | | Fast Mode Plus | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | | |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| $t_{HD;\ STA}$ | Hold time (repeated) START condition | 4.0 | - | 0.6 | - | 0.26 | - | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | - | 1.3 | - | 0.5 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4.0 | - | 0.6 | - | 0.26 | - | µs |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | 4.7 | - | 0.6 | - | 0.26 | - | µs |
| $t_{HD;DAT}$ | Data hold time | 5.0 | - | - | - | - | - | µs |
| $t_{SU;DAT}$ | Data set-up time | 250 | - | 100 | - | 50 | - | ns |
| $t_{SU;STO}$ | Set-up time for STOP condition | 4.0 | - | 0.6 | - | 0.26 | - | µs |
| $t_{BUF}$ | Bus free time between a STOP and START | 4.7 | - | 1.3 | - | 0.5 | - | µs |

**Table 8. I2C Timing Characteristics**

NOTE: Values are based on I2C Specification requirements, not tested in production.

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### 4.3.4 SPI TIMING CHARACTERISTICS

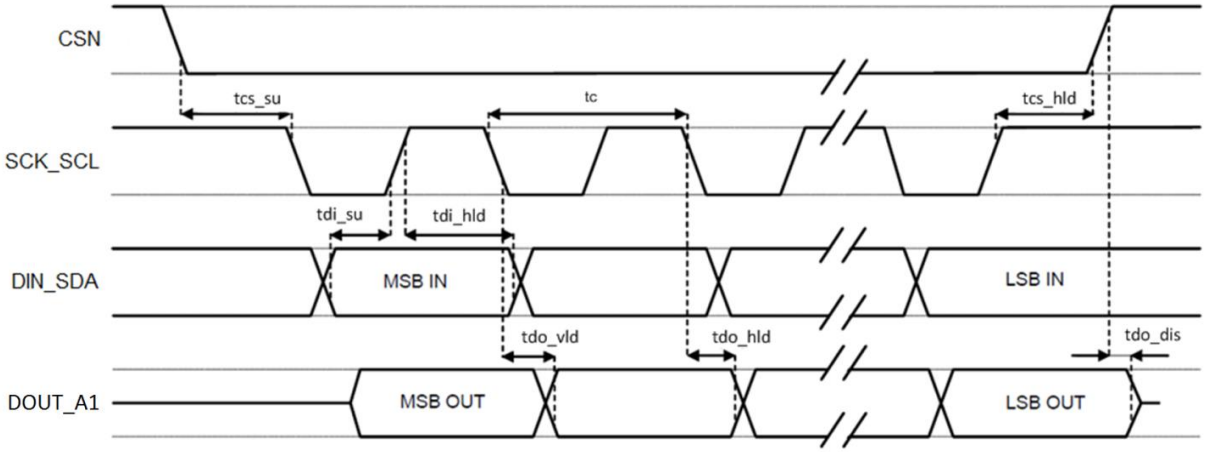



**Figure 11. SPI Interface Timing Waveform**

| Symbol | Parameter | Value | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| tc | SPI SCK_SCL Clock Cycle | 500 | | | ns |
| fc | SPI SCK_SCL Clock Frequency | | 8[4] | | MHz |
| tcs_su | SPI CSN Setup Time | 6 | | | ns |
| tcs_hld | SPI CSN Hold Time | 8 | | | ns |
| tdi_su | SPI DIN_SDA Input Setup Time | 5 | | | ns |
| tdi_hld | SPI DIN_SDA Input Hold Time | 15 | | | ns |
| tdo_vld | SPI DOUT_A1 Valid Output Time | | | 50 | ns |
| tdo_hld | SPI DOUT_A1 Output Hold Time | 9 | | | ns |
| tdo_dis | SPI DOUT_A1 Output Disable Time | | | 50 | ns |

**Table 9. SPI Interface Timing Parameters**

[4] Values are based on device characterization.

# 5 GENERAL OPERATION

The device supports the reading of samples and device status upon interrupt or via polling. It contains a 12-bit 32 sample FIFO with programmable watermark. The device is internally clocked but also includes a manual trigger mode. It can be put into several low power modes, depending upon the desired sensing application. The device can run in full-featured mode from its fast internal clock or from a slower heartbeat clock, with limited functionality and at lower power. The device can connect as a slave to either a SPI or I2C master.

## 5.1 SENSOR SAMPLING

X, Y and Z accelerometer data is stored in registers XOUT, YOUT, and ZOUT registers. The data is represented as 2's complement format.

The desired resolution and full scale acceleration range are set in the RANGE_C register.

## 5.2 OFFSET AND GAIN CALIBRATION

The default digital offset and gain calibration data can be read from the device, if necessary, in order to reduce the effects of post-assembly influences and stresses which may cause the sensor readings to be offset from their factory values.

## 5.3 RESET

The device can be completely reset via an I2C or SPI instruction. Writing register 0x24 with 0x40 (bit 6) causes a power-on reset operation to execute. No attempt should be made to access registers within 1mSec after issuing this operation. The device must be placed in STANDBY mode before executing the reset. The pin DOUT_A1 is sampled for the purposes of setting the I2C device address after this reset operation.

NOTE: Immediately after a RESET or power-up event, several registers must be written with initialization values as shown below. The recommended sequence for I2C interface is:

| Step | Address | Value which must be written | Comment |
|---|---|---|---|
| **1** | 0x10 | 0x01 | Go to standby |
| **2** | 0x24 | 0x40 | Reset (or Power-On) |
| **3** | NA | Wait at least 1mSec | Wait for reset to complete |
| **4** | 0x0D | 0x40 | I2C mode enabled |
| **5** | 0x0F | 0x42 | Initialization |
| **6** | 0x20 | 0x01 | Initialization |
| **7** | 0x21 | 0x80 | Initialization |
| **8** | 0x28 | 0x00 | Initialization |
| **9** | 0x1A | 0x00 | Initialization |
| **10** | Configure remaining registers and use sensor as normal | | |

**Table 10. Recommended Initialization Sequence for I2C Interface**

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And the recommended sequence for SPI interface is:

| Step | Address | Value which must be written | Comment |
|---|---|---|---|
| **1** | 0x10 | 0x01 | Go to standby |
| **2** | 0x24 | 0x40 | Reset (or Power-On) |
| **3** | NA | Wait at least 1mSec | Wait for reset to complete |
| **4** | 0x18 | Read | Non-zero value |
| **5** | 0x0D | 0x80 | SPI mode enabled |
| **6** | 0x0D | Read | Repeat steps 5 & 6 till 0x80 is read |
| **7** | 0x0F | 0x42 | Initialization |
| **8** | 0x10 | 0x01 | Go to Standby from Sleep |
| **9** | NA | Wait at least 10mSec | Wait for state machine |
| **10** | 0x20 | 0x01 | Initialization |
| **11** | 0x21 | 0x80 | Initialization |
| **12** | 0x28 | 0x00 | Initialization |
| **13** | 0x1A | 0x00 | Initialization |
| **14** | Configure remaining registers and use sensor as normal | | |

**Table 11. Recommended Initialization Sequence for SPI Interface**

## 5.4 RELOAD

The device registers can be reloaded from OTP via an I2C or SPI instruction. Writing register 0x24 with 0x80 (bit 7) causes a reload operation to execute. The contents of OTP are reloaded into the register set. However any non-loaded register locations will not be affected. No attempt should be made to access registers within 1mSec after issuing this operation. The device must be placed in STANDBY mode before executing the reset.

The pin DOUT_A1 is sampled for the purposes of setting the I2C device address after this reload operation.

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## 5.5 OPERATIONAL MODES

The device has various modes of operation as described below:

| Mode | Description and Comments |
|---|---|
| **SLEEP** | SLEEP is the lowest power mode. The internal regulators are enabled, and much of the chip is disabled. The SLEEP mode is the default POR mode. This command is available at any time, although up to three periods of the internal heartbeat clock may be required to complete the transition. |
| **STANDBY** | STANDBY is a low power mode. All internal regulators are enabled, and internal main and heartbeat clocks are enabled. The default STANDBY frequency for the heartbeat clock is ~500 Hz. TRIG mode operation can be executed only from this mode.<br><br>**Software must change the mode to SLEEP or STANDBY in register 0x10 before writing to any other register.** |
| **SNIFF** | SNIFF is a lower power, limited activity detection mode; Sniff circuitry is enabled and sniff-only sampling is enabled. There are no FIFO operations, and hardware will automatically transition to CWAKE mode upon activity detection. |
| **CWAKE** | CWAKE or continuous wake is the typical XYZ sampling mode. Sample data is written to the output registers, or the FIFO when enabled. Hardware will automatically transition to CWAKE mode upon SNIFF activity detection. |
| **SWAKE** | SNIFF and CWAKE circuitry are both active simultaneously. Sniff circuitry is enabled and XYZ samples are written to the output registers, or the FIFO when enabled. |
| **TRIG** | The device produces a fixed number of samples, between 1 and 254, or continuously. This mode ignores the setting in the ODR, but uses the STB_RATE[2:0] clock setting as the sampling rate. The trigger can be set to come from the external pin INTN or a write to register bit 0x10[7]. |

**Table 12. Operational Modes**

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## 5.6 MODE STATE MACHINE FLOW

Figure 12. Mode Operational Flow shows the operational mode flow for the device. The device defaults to SLEEP mode following power-on. Mode transitions occur at an approximate rate of ~500Hz. Depending on the operation, the MODE State Machine may trigger events that auto-clear or set the MCTRL[2:0] bits in register 0x10 after a particular command is chosen.

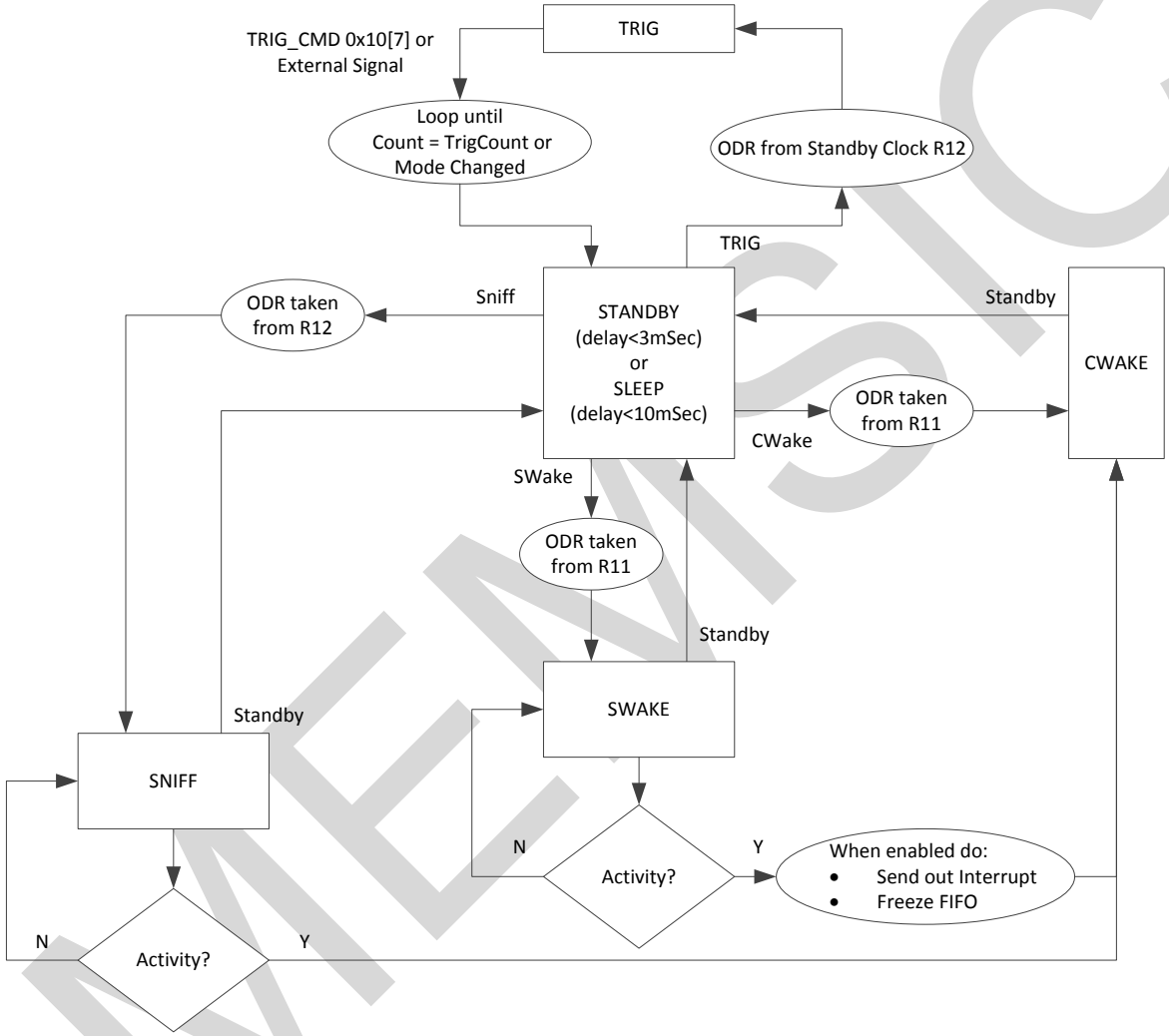



**Figure 12. Mode Operational Flow**

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# 6 INTERFACES

## 6.1 SPI VS I2C OPERATION MODES

The device contains both I2C and SPI slave interfaces which share common pins. However, only one interface can be active for correct device operation. Once the device completes POR or a hard reset, both interfaces are active.

**After power-up and any reset of the device, the first transaction to the device must be writing to the selected enable bit, either "I2C_EN" or "SPI_EN" in register 0x0D. The situation where bits are set at the same time must be avoided or unstable device operation could occur.**

To keep the "disabled" interface from interfering in future transactions, the corresponding "enable" bit must be set in the register set. For example, if the 4-wire SPI interface is to be active, write a value of 0x80 to register 0x0D.

## 6.2 I2C PHYSICAL INTERFACE

The I2C slave interface operates at a maximum speed of 1 MHz in I2C "Fast Mode Plus". The SDA (data) is an open-drain, bi-directional pin and the SCL (clock) is an input pin.

**The device always operates as an I2C slave.**

An I2C master initiates all communication and data transfers and generates the SCK_SCL clock that synchronizes the data transfer. The I2C device address depends upon the settings of various registers and pins as shown in the table below.

An I2C master initiates all communication and data transfers and generates the SCK_SCL clock that synchronizes the data transfer. The I2C device address depends upon the state of pin DOUT_A1 during power-up as shown in the table below.

| 7-bit Device ID | 8-bit Address (Write) | 8-bit Address (Read) | DOUT_A1 level upon power-up |
|---|---|---|---|
| 0x4C (0b1001100) | 0x98 | 0x99 | GND |
| 0x6C (0b1101100) | 0xD8 | 0xD9 | VDD |

**Table 13. I2C Address Selection**

The I2C interface remains active as long as power is applied to the VDDIO pin. In STANDBY mode the device responds to I2C read and write cycles, but interrupts cannot be cleared. All registers can be written in the SLEEP or STANDBY modes, but in CWAKE only the (0x10) Mode Control Register can be modified.

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Internally, the registers which are used to store samples are clocked by the sample clock and gated by I2C activity. Therefore, in order to allow the device to collect and present samples in the sample registers at least one I2C STOP condition must be present between samples.

Refer to the I2C specification for a detailed discussion of the protocol. Per I2C requirements, when the I2C interface is enabled, DIN_SDA is an open drain, bi-directional pin. Pins SCK_SCL and DIN_SDA each require an external pull-up resistor, typically 4.7kΩ.

## 6.3 I2C MESSAGE FORMAT

**NOTE: At least one I2C STOP condition must be present between samples in order for the device to update the sample data registers.**

The device uses the following general format for writing to the internal registers. The I2C master generates a START condition, and then supplies the 7-bit device ID. The 8th bit is the R/W# flag (write cycle = 0). The device pulls DIN_SDA low during the 9th clock cycle indicating a positive ACK.

The second byte is the 8-bit register address of the device to access, and the last byte is the data to write.

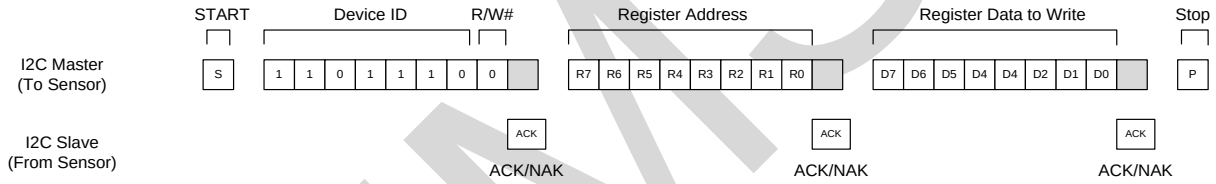



**Figure 13. I2C Message Format, Write Cycle, Single Register Write**

In a read cycle, the I2C master writes the device ID (R/W#=0) and register address to be read. The master issues a RESTART condition and then writes the device ID with the R/W# flag set to '1'. The device shifts out the contents of the register address.

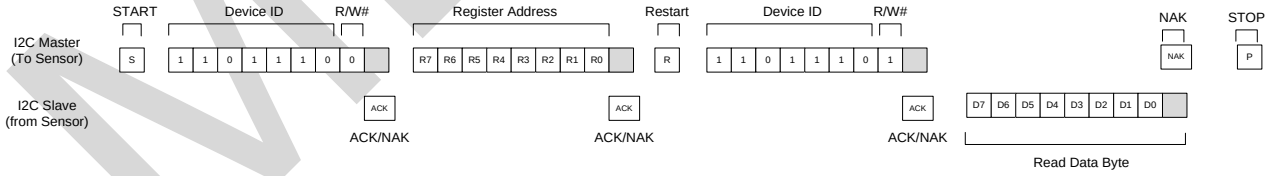



**Figure 14. I2C Message Format, Read Cycle, Single Register Read**

The I2C master may write or read consecutive register addresses by writing or reading additional bytes after the first access. The device will internally increment the register address.

**NOTE: See (0x0E) Feature Register 2 for address wrap details.**

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## 6.4 SPI PHYSICAL INTERFACE

The device always operates as an SPI slave. An SPI master must initiate all communication and data transfers and generate the SCK_SCL clock that synchronizes the data transfer. The CSN pin must be pulled up to VDDIO when the SPI interface is not in use. The SPI interface can operate in 3-wire or 4-wire mode.

## 6.5 SPI 3-WIRE MODE

SPI 3-wire mode is disabled by default. To enable 3-wire mode, the first write to the device should immediately enable this feature in register (0x0D) Feature Register 1. In 3-wire mode the pins DOUT_A1 and DIN_SDA must be connected on the PCB. Anytime there is a reset to the device, a POR event, or a power cycle the SPI 3-wire configuration will reset to 4-wire mode.

## 6.6 SPI PROTOCOL

The general protocol for the SPI interface is shown in the figures below. The falling edge of CSN initiates the start of the SPI bus cycle. The first byte of the transaction is the command/address byte. Because the register address space is 64 locations, a total of 6 address bits are required for each SPI bus cycle. During clock ‘1’, the R/W# bit is set to ‘0’ for a write cycle or ‘1’ for a read cycle.

The interface supports 2 types of addressing: 1-byte (typically used) and 2-byte (to support legacy hardware). In the case of 2-byte addressing, the bits occurring during clocks 2 and 9-16 must be driven to ‘0’ for the address to be correctly decoded. Each read or write transaction always requires a minimum of 16 or 24 cycles of the SCK_SCL pin.

When the SPI master is writing data, data may change when the clock is low, and must be stable on the clock rising edge. Similarly, output data written to the SPI master is shifted out on the falling edge of clock and can be latched by the master on the rising edge of the clock. Serial data in or out of the device is always MSB first.

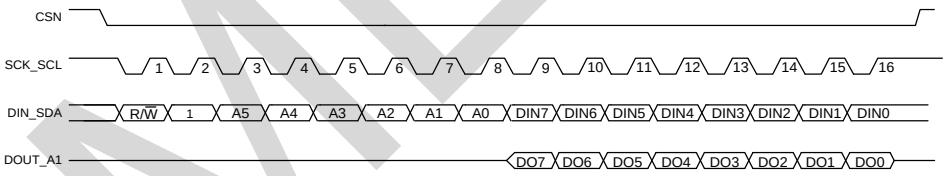



**Figure 15. General SPI Protocol, 1-Byte Address**

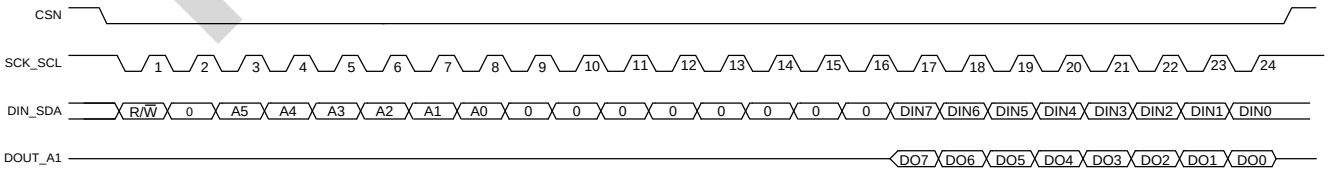



**Figure 16. General SPI Protocol, 2-Byte Address (legacy)**

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**NOTE: Either 1-byte or 2-byte addressing may be used for any SPI transaction, although for simplicity, the remaining timing diagrams show only 1-byte addressing.**

## 6.7 SPI REGISTER WRITE CYCLE - SINGLE

A single register write consists of a 16-clock transaction. As described above, the first bit is set to ‘0’ indicating a register write followed by the register address.

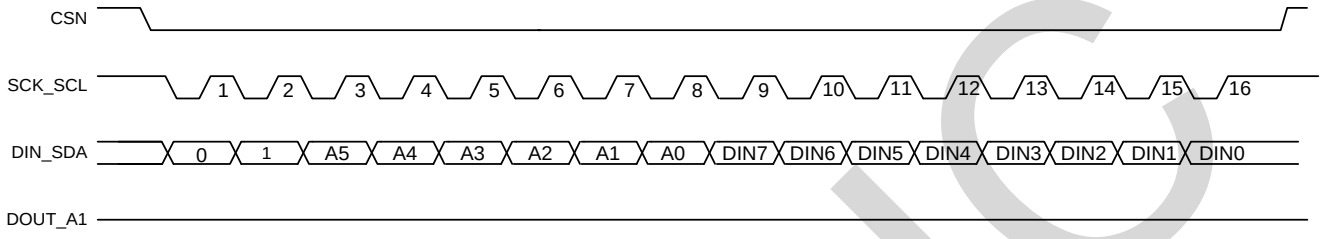



**Figure 17. SPI Register Write Cycle - Single**

## 6.8 SPI REGISTER WRITE CYCLE - BURST

A burst (multi-byte) register write cycle uses the address specified at the beginning of the transaction as the starting register address. Internally the address will auto-increment to the next consecutive address for each additional byte (8-clocks) of data written beyond clock 8.

**NOTE: See (0x0E) Feature Register 2 for address wrap details.**

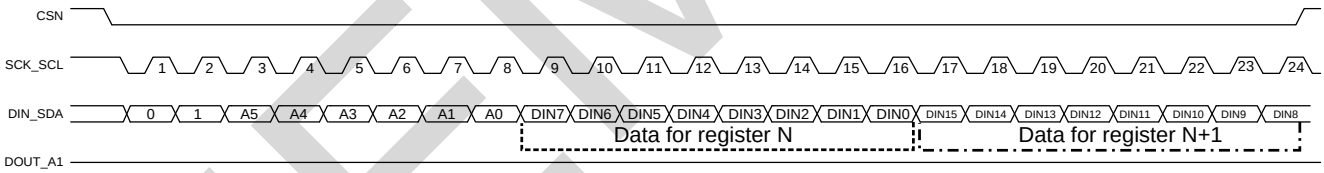



**Figure 18.SPI Register Write Cycle - Burst (2-register burst example)**

## 6.9 SPI REGISTER READ CYCLE - SINGLE

A single register read consists of a 16-clock transaction. As described above, the first bit is set to ‘1’ indicating a register read followed by the register address.

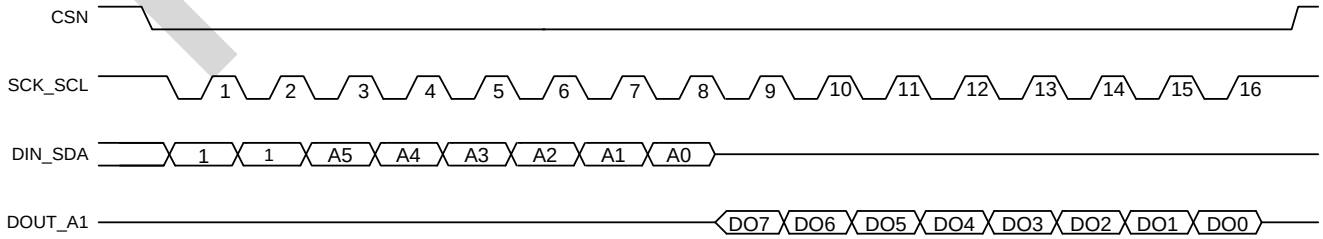



**Figure 19. SPI Register Read Cycle - Single**

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## 6.10 SPI REGISTER READ CYCLE - BURST

A burst (multi-byte) register read cycle uses the address specified at the beginning of the transaction as the starting register address. Internally the address will auto-increment to the next consecutive address for each additional byte (8-clocks) of data read beyond clock 8.

**NOTE: See (0x0E) Feature Register 2 for address wrap details.**

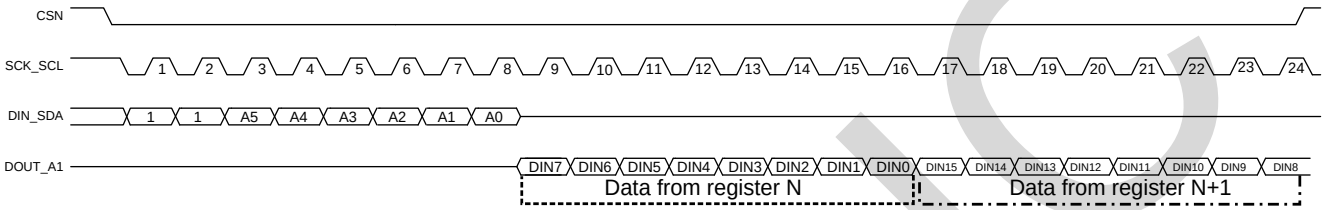



**Figure 20. SPI Register Read Cycle - Burst (2 register burst example)**

## 6.11 SPI STATUS OPTION

The device supports an optional SPI status feature, only in SPI 4-wire mode. This feature is enabled in register (0x0E) Feature Register 2. During the first 6-bits of any SPI transaction (immediately after the falling edge of CSN), the DOUT_A1 pin will output six status bits related to the device. Following the 6th clock cycle, the device will float the DOUT_A1 pin before a possible read cycle begins. The status bits sent are shown below:

| Bit 7 (First Out) | Bit6 | Bit5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (Last Out) |
|---|---|---|---|---|---|---|---|
| INT_PEND | FIFO_THRESH | FIFO_FULL | FIFO_EMPTY | NEW_DATA | WAKE | 0 | 0 |

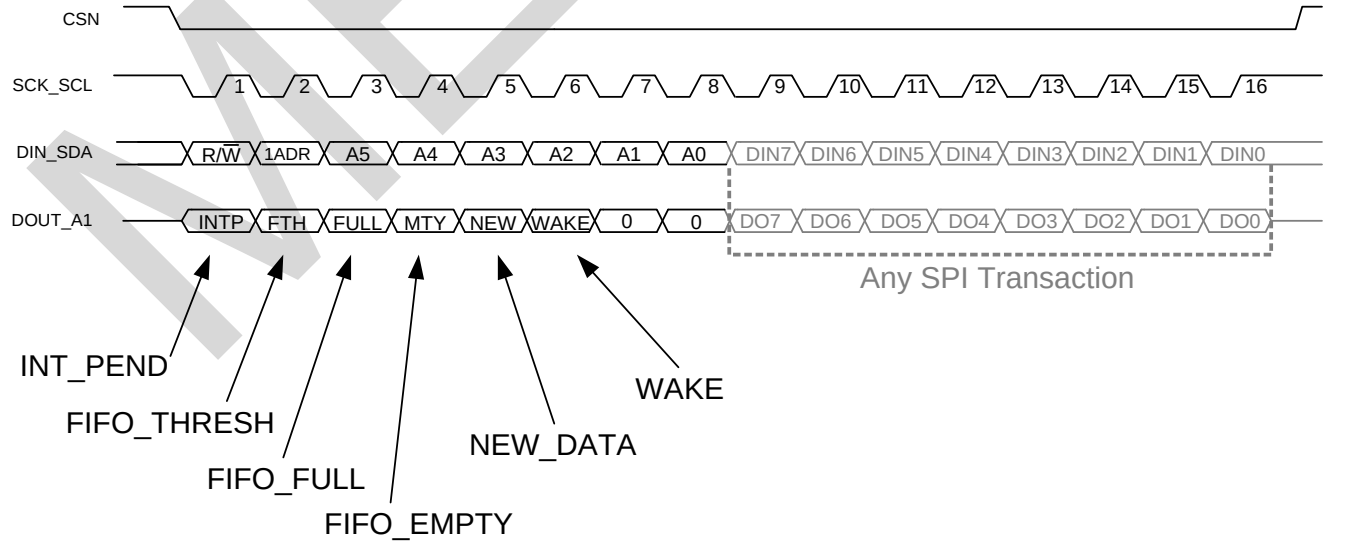



**Figure 21. SPI Status bits**

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## 6.12 SPI HIGH-SPEED MODE

To achieve SPI speed greater than 2MHz, use the following sequence:

- Start SPI at low speed (less than 2MHz)
- Enable SPI mode –
    - “SPI_EN” in section 7.7 (0x0D) Feature Register 1
- Enable high speed SPI mode –
    - “SPI_HS_EN” in section 7.20 (0x1C) Power Mode Control Register
- Increase SPI speed up to 8MHz

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# 7 REGISTER INTERFACE

The device has a simple register interface which allows an SPI or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, bit 0 is the least significant bit (LSB) of a byte register.

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## 7.1 REGISTER SUMMARY

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | EXT_STAT_1 | Extended Status 1 | RESV | RESV | RESV | RESV | I2C_AD0 | RESV | RESV | RESV | 0x00 | R |
| 0x01 | EXT_STAT_2 | Extended Status 2 | SNIFF_ DETECT | SNIFF_EN | OTP_ BUSY | RESV | RESV | RESV | PD_CLK_ STAT | OVR_ DATA | 0x04 | R |
| 0x02 | XOUT_LSB | XOUT_LSB | XOUT[7] | XOUT[6] | XOUT[5] | XOUT[4] | XOUT[3] | XOUT[2] | XOUT[1] | XOUT[0] | 0x00 | R |
| 0x03 | XOUT_MSB | XOUT_MSB | XOUT[15] | XOUT[14] | XOUT[13] | XOUT[12] | XOUT[11] | XOUT[10] | XOUT[9] | XOUT[8] | 0x00 | R |
| 0x04 | YOUT_LSB | YOUT_LSB | YOUT[7] | YOUT[6] | YOUT[5] | YOUT[4] | YOUT[3] | YOUT[2] | YOUT[1] | YOUT[0] | 0x00 | R |
| 0x05 | YOUT_MSB | YOUT_MSB | YOUT[15] | YOUT[14] | YOUT[13] | YOUT[12] | YOUT[11] | YOUT[10] | YOUT[9] | YOUT[8] | 0x00 | R |
| 0x06 | ZOUT_LSB | ZOUT_LSB | ZOUT[7] | ZOUT[6] | ZOUT[5] | ZOUT[4] | ZOUT[3] | ZOUT[2] | ZOUT[1] | ZOUT[0] | 0x00 | R |
| 0x07 | ZOUT_MSB | ZOUT_MSB | ZOUT[15] | ZOUT[14] | ZOUT[13] | ZOUT[12] | ZOUT[11] | ZOUT[10] | ZOUT[9] | ZOUT[8] | 0x00 | R |
| 0x08 | STATUS_1 | Status 1 | INT_PEND | FIFO_ THRESH | FIFO_FULL | FIFO_ EMPTY | NEW_ DATA | MODE[2] | MODE[1] | MODE[0] | 0x00 | R |
| 0x09 | STATUS_2 | Status 2 | INT_ SWAKE | INT_FIFO_ THRESH | INT_FIFO_ FULL | INT_FIFO_ EMPTY | INT_ACQ | INT_WAKE | RESV | RESV | 0x00 | R |
| 0x0A – 0x0C | | RESERVED | | | | | | | | | | |
| 0x0D | FREG_1 | Feature 1 | SPI_EN | I2C_EN | SPI3_EN | INTSC_EN | FREEZE | 0 | 0 | 0 | 0x00 | W |
| 0x0E | FREG_2 | Feature 2 | EXT_ TRIG_EN | EXT_ TRIG_POL | FIFO_ STREAM | I2CINT_ WRCLRE | FIFO_ STAT_EN | SPI_ STAT_EN | FIFO_ BURST | WRAPA | 0x00 | W |
| 0x0F | INIT_1 | Initialization 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | (See note) | WO |
| 0x10 | MODE_C | Mode Control | TRIG_ CMD | Z_AXIS_ PD | Y_AXIS_ PD | X_AXIS_ PD | RESV | MCTRL[2] | MCTRL[1] | MCTRL[0] | 0x00 | W |
| 0x11 | RATE_1 | Rate 1 | 0 | 0 | 0 | 0 | RR[3] | RR[2] | RR[1] | RR[0] | 0x00 | W |
| 0x12 | SNIFF_C | Sniff Control | STB_RATE [2] | STB_RATE [1] | STB_RATE [0] | 0 | SNIFF_SR [3] | SNIFF_SR [2] | SNIFF_SR [1] | SNIFF_SR [0] | 0x00 | W |
| 0x13 | SNIFFTH_C | Sniff Threshold Control | SNIFF_ MODE | SNIFF_ AND_OR | SNIFF_ TH[5] | SNIFF_ TH[4] | SNIFF_ TH[3] | SNIFF_ TH[2] | SNIFF_ TH[1] | SNIFF_ TH[0] | 0x00 | W |
| 0x14 | SNIFFCF_C | Sniff Configuration | SNIFF_ RESET | SNIFF_ MUX[2] | SNIFF_ MUX[1] | SNIFF_ MUX[0] | SNIFF_ CNTEN | SNIFF_ THADR[2] | SNIFF_ THADR[1] | SNIFF_ THADR[0] | 0x00 | W |
| 0x15 | RANGE_C | Range Resolution Control | RESV | RANGE [2] | RANGE [1] | RANGE [0] | RESV | RES[2] | RES[1] | RES[0] | 0x00 | W |
| 0x16 | FIFO_C | FIFO Control | FIFO_ RESET | FIFO_EN | FIFO_ MODE | FIFO_TH[4] | FIFO_TH[3] | FIFO_TH[2] | FIFO_TH[1] | FIFO_TH[0] | 0x00 | W |
| 0x17 | INTR_C | Interrupt Control | INT_ SWAKE | INT_FIFO_ THRESH | INT_FIFO_ FULL | INT_FIFO_ EMPTY | INT_ACQ | INT_ WAKE | IAH | IPP | 0x00 | R |
| 0x18 – 0x19 | | RESERVED | | | | | | | | | | |
| 0x1A | INIT_3 | Initialization 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | RW |
| 0x1B | SCRATCH | Scratchpad | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | RW |

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| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x1C | PMCR | Power Mode Control | SPI_HS_EN | SPM[2] | SPM[1] | SPM[0] | RESV | CSPM[2] | CSPM[1] | CSPM[0] | 0x00 | W |
| 0x1D – 0x1F | | RESERVED | | | | | | | | | | |
| 0x20 | DMX | Drive Motion X | 0 | 0 | 0 | 0 | DNX | DPX | 0 | 1 | 0x00 | W |
| 0x21 | DMY | Drive Motion Y | 1 | 0 | 0 | 0 | DNY | DPY | 0 | 0 | (See table) | W |
| 0x22 | DMZ | Drive Motion Z | 0 | 0 | 0 | 0 | DNZ | DPZ | 0 | 0 | 0x00 | W |
| 0x23 | | RESERVED | | | | | | | | | | |
| 0x24 | RESET | Reset | RELOAD | RESET | RESV | RESV | RESV | RESV | RESV | RESV | 0x00 | W |
| 0x25 – 0x27 | | RESERVED | | | | | | | | | | |
| 0x28 | INIT_2 | Initialization Register 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | W |
| 0x29 | TRIGC | Trigger Count | TRIGC[7] | TRIGC[6] | TRIGC[5] | TRIGC[4] | TRIGC[3] | TRIGC[2] | TRIGC[1] | TRIGC[0] | 0x00 | W |
| 0x2A | XOFFL | X-Offset LSB | XOFF[7] | XOFF[6] | XOFF[5] | XOFF[4] | XOFF[3] | XOFF[2] | XOFF[1] | XOFF[0] | Per chip | W |
| 0x2B | XOFFH | X-Offset MSB | XGAIN[8] | XOFF[14] | XOFF[13] | XOFF[12] | XOFF[11] | XOFF[10] | XOFF[9] | XOFF[8] | Per chip | W |
| 0x2C | YOFFL | Y-Offset LSB | YOFF[7] | YOFF[6] | YOFF[5] | YOFF[4] | YOFF[3] | YOFF[2] | YOFF[1] | YOFF[0] | Per chip | W |
| 0x2D | YOFFH | Y-Offset MSB | YGAIN[8] | YOFF[14] | YOFF[13] | YOFF[12] | YOFF[11] | YOFF[10] | YOFF[9] | YOFF[8] | Per chip | W |
| 0x2E | ZOFFL | Z-Offset LSB | ZOFF[7] | ZOFF[6] | ZOFF[5] | ZOFF[4] | ZOFF[3] | ZOFF[2] | ZOFF[1] | ZOFF[0] | Per chip | W |
| 0x2F | ZOFFH | Z-Offset MSB | ZGAIN[8] | ZOFF[14] | ZOFF[13] | ZOFF[12] | ZOFF[11] | ZOFF[10] | ZOFF[9] | ZOFF[8] | Per chip | W |
| 0x30 | XGAIN | X Gain | XGAIN[7] | XGAIN[6] | XGAIN[5] | XGAIN[4] | XGAIN[3] | XGAIN[2] | XGAIN[1] | XGAIN[0] | Per chip | W |
| 0x31 | YGAIN | Y Gain | YGAIN[7] | YGAIN[6] | YGAIN[5] | YGAIN[4] | YGAIN[3] | YGAIN[2] | YGAIN[1] | YGAIN[0] | Per chip | W |
| 0x32 | ZGAIN | Z Gain | ZGAIN[7] | ZGAIN[6] | ZGAIN[5] | ZGAIN[4] | ZGAIN[3] | ZGAIN[2] | ZGAIN[1] | ZGAIN[0] | Per chip | W |
| 0x33 – 0x3F | | RESERVED | | | | | | | | | | |

**Table 14. Register Summary**

[4] 'R' registers are read-only. 'W' registers are read-write. 'WO' registers are write only.

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## 7.2 (0X00) EXTENDED STATUS REGISTER 1

This register contains status for the I2C address of the device.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x00 | EXT_STAT_1 | RESV | RESV | RESV | RESV | I2C_AD0 | RESV | RESV | RESV | 00000000 | R |

| Bit | Name | Description |
|---|---|---|
| **[2:0]** | RESV | Reserved |
| **3** | I2C_AD0_BIT | Value of I2C slave address obtained from reading the DOUT_A1 pin at POR. If this bit is '1', the 7-bit base address of the I2C slave changes from 0x4C to 0x6C. |
| **[7:4]** | RESV | Reserved |

**Table 15. Extended Status Register 1 Settings**

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## 7.3 (0X01) EXTENDED STATUS REGISTER 2

The device status register reports various conditions of the device data, clock and sniff circuitry.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x01 | EXT_STAT_2 | SNIFF_ DETECT | SNIFF_EN | OTP_BUSY | RESV | RESV | RESV | PD_CLK_ STAT | OVR_ DATA | 0x04 | RO |

| Bit | Name | Description |
|---|---|---|
| **0** | OVR_DATA | 0: Previous acceleration sample has not been overwritten before read by host<br>1: Previous acceleration sample was not read by host and has been overwritten. |
| **1** | PD_CLK_STAT | Returns the power-down status of the clocks.<br>0: Clocks are enabled.<br>1: Clocks are disabled. |
| **[4:2]** | RESV | Reserved |
| **5** | OTP_BUSY | OTP VDD status bit:<br>0: OTP_VDD supply is not enabled, OTP is powered down.<br>1: OTP_VDD supply is enabled, OTP is powered. |
| **6** | SNIFF_EN | SNIFF mode enable flag:<br>0: SNIFF mode is not active.<br>1: SNIFF mode is active. |
| **7** | SNIFF_DETECT | SNIFF wakeup or detect flag:<br>0: No sniff event detected.<br>1: Sniff event detected, move to CWAKE mode. |

**Table 16. Extended Status Register 2 Settings**

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## 7.4 (0X02 – 0X07) XOUT, YOUT & ZOUT DATA OUTPUT REGISTERS

The measurements from sensors for the 3-axes are available in these 3 registers. The most-significant bit of the value is the sign bit, and is sign extended to the higher bits.

**Software must set only one of the bits SPI_EN or I2C_EN in register 0x0D to '1', depending upon if the I2C or SPI interface will be used for external communications. No data will appear in XOUT, YOUT and ZOUT registers if both the I2C_EN bit and SPI_EN bit are set to 0 (default).**

When the FIFO is enabled, the output of the FIFO is mapped to registers 0x02 to 0x07, and the data has a maximum resolution of 12-bits.

**During FIFO reads, software must start a read at address 0x02 and complete a read to address 0x07 for the FIFO pointers to increment correctly.**

Once an I2C start bit has been recognized by the device, registers will not be updated until an I2C stop bit has occurred. Therefore, if software desires to read the low and high byte registers 'atomically', knowing that the values have not been changed, it should do so by issuing a start bit, reading one register, then reading the other register then issuing a stop bit. Note that all 6 registers may be read in one burst with the same effect.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x02 | XOUT_LSB | XOUT LSB Register | XOUT [7] | XOUT [6] | XOUT [5] | XOUT [4] | XOUT [3] | XOUT [2] | XOUT [1] | XOUT [0] | 0x00 | R |
| 0x03 | XOUT_MSB | XOUT MSB Register | XOUT [15] | XOUT [14] | XOUT [13] | XOUT [12] | XOUT [11] | XOUT [10] | XOUT [9] | XOUT [8] | 0x00 | R |
| 0x04 | YOUT_LSB | YOUT LSB Register | YOUT [7] | YOUT [6] | YOUT [5] | YOUT [4] | YOUT [3] | YOUT [2] | YOUT [1] | YOUT [0] | 0x00 | R |
| 0x05 | YOUT_MSB | YOUT MSB Register | YOUT [15] | YOUT [14] | YOUT [13] | YOUT [12] | YOUT [11] | YOUT [10] | YOUT [9] | YOUT [8] | 0x00 | R |
| 0x06 | ZOUT_LSB | ZOUT LSB Register | ZOUT [7] | ZOUT [6] | ZOUT [5] | ZOUT [4] | ZOUT [3] | ZOUT [2] | ZOUT [1] | ZOUT [0] | 0x00 | R |
| 0x07 | ZOUT_MSB | ZOUT MSB Register | ZOUT [15] | ZOUT [14] | ZOUT [13] | ZOUT [12] | ZOUT [11] | ZOUT [10] | ZOUT [9] | ZOUT [8] | 0x00 | R |

**Table 17. XOUT, YOUT, ZOUT Data Output Registers**

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## 7.5 (0X08) STATUS REGISTER 1

This register reports the operational mode of the device. Note that the lower 3-bits, the MODE[2:0] field, do not immediately change once a command is written to the MODE register, but may take up to 3 transitions of the heartbeat clock.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x08 | STATUS_1 | INT_PEND | FIFO_ THRESH | FIFO_FULL | FIFO_ EMPTY | NEW_ DATA | MODE[2] | MODE[1] | MODE[0] | 00000000 | RO |

| Bit | Name | Description | | |
|---|---|---|---|---|
| **[2:0]** | MODE[2:0] | **Bit Field** | **Mode** | **Comments** |
| | | 000 | SLEEP | Lowest power mode, regulators on, no clock activity, partial chip power-down |
| | | 001 | STANDBY | Low power mode, no sampling, clocks active. |
| | | 010 | SNIFF | Sniff activity detection mode, sniff enabled, sniff sampling, no FIFO operations, automatically transition to CWAKE mode upon activity detection |
| | | 011 | RESV | Reserved |
| | | 100 | RESV | Reserved |
| | | 101 | CWAKE | Continuous wake. Active XYZ sampling. Sniff circuitry not active. |
| | | 110 | SWAKE | Use Sniff logic, main XYZ pipeline and optional FIFO at the same time; highest power consumption |

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| | | | | |
|---|---|---|---|---|
| | | 111 | TRIG | Trigger mode, 1 to 254 samples or continuous, return to sleep upon completion |
| **3** | NEW_DATA | 0: No new sample data has arrived since last read.<br>1: New sample data has arrived and has been written to FIFO/registers. This bit is always enabled and valid, regardless of the settings of any interrupt enable bits. | | |
| **4** | FIFO_EMPTY | 0: FIFO has one or more samples in storage (level)<br>1: FIFO is empty (level) (default). This bit is set to 1 immediately after device power-up or device reset. | | |
| **5** | FIFO_FULL | 0: FIFO has space or 1 or more samples (up to 32) (level).<br>1: FIFO is full, all 32 samples are used (level). | | |
| **6** | FIFO_THRESH | 0: Amount of data in FIFO is less than the threshold (level)<br>1: Amount of data in FIFO is equal to or greater than the threshold (level) | | |
| **7** | INT_PEND | 0: No interrupt flags are pending in register 0x09 (level)<br>1: One or more interrupt flags are pending in register 0x09 (logical OR) (level). | | |

**Table 18. Status Register 1 Settings**

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## 7.6 (0X09) STATUS REGISTER 2

This register reports the state of the interrupts (‘0’ means not pending; ‘1’ means pending). A bit in this register will only be set if the corresponding interrupt enable is set to ‘1’ in (0x17) Interrupt Control Register. Interrupts can be cleared in the following ways using (0x0E) Feature Register 2 bit 4:

| Interface | Method |
|---|---|
| I2C clearing method (default) | Read Register 0x09 |
| I2C clearing method (optional) | Write Register 0x09 |
| SPI clearing method | Write Register 0x09 |

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x09 | STATUS_2 | INT_ SWAKE | INT_FIFO_ THRESH | INT_FIFO_ FULL | INT_FIFO_ EMPTY | INT_ACQ | INT_WAKE | RESV | RESV | 00000000 | RO |

| Bit | Name | Description |
|---|---|---|
| **[1:0]** | Reserved | Reserved. |
| **2** | INT_WAKE | This interrupt will transition when the accelerometer automatically moves from SNIFF to CWAKE. Once cleared, another SNIFF to CWAKE event must take place to retrigger it. |
| **3** | INT_ACQ | This interrupt will transition when a new sample is acquired. This flag stays high upon the first sample acquired and will not rearm unless cleared. Only active in CWAKE and TRIG modes. |
| **4** | INT_FIFO_EMPTY | This interrupt will transition when the FIFO is empty. This flag stays high upon the first empty condition and will not rearm unless cleared. The FIFO empty condition must be negated (e.g. the FIFO must become ‘not’ empty), and then empty again for the INT_FIFO_EMPTY flag to retrigger. |

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| | | |
|---|---|---|
| **5** | INT_FIFO_FULL | This interrupt will transition when the FIFO is full (32 XYZ samples). This flag stays high upon the first full condition and will not rearm unless cleared. The FIFO full condition must be negated (e.g. the FIFO must become 'not' full), and then full again for the INT_FIFO_FULL flag to retrigger. |
| **6** | INT_FIFO_THRESH | This interrupt will transition when the FIFO sample count is equal to or greater than the threshold count 0x16[4:0]. This flag stays high upon the first threshold condition and will not rearm unless cleared. |
| **7** | INT_SWAKE | This interrupt will transition when the SNIFF block has detected an event only when the device is in SWAKE mode. Once an SWAKE interrupt is generated, the SNIFF block stops processing new events until the interrupt is cleared and the SNIFF block is reset. Optionally, the SNIFF block can be reset at the same time INT_SWAKE is cleared – see (0x0D) Feature Register 1 bit 4. |

**Table 19. Status Register 2 Settings**

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## 7.7 (0X0D) FEATURE REGISTER 1

This register is used to select the interface mode as well as the operation style of the FIFO and interrupt in SWAKE mode.

**NOTE: Software must set only one of the bits SPI_EN or I2C_EN in register 0x0D to '1', depending upon if the I2C or SPI interface will be used for external communications. No data will appear in XOUT, YOUT and ZOUT registers if both the I2C_EN bit and SPI_EN bit are set to 0 (default).**

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x0D | FREG_1 | SPI_EN | I2C_EN | SPI3_EN | INTSC_EN | FREEZE | 0 | 0 | 0 | 00000000 | RO |

| Bit | Name | Description |
|---|---|---|
| **[2:0]** | <Must write '000'> | Software must always write '000' to these 3 bits |
| **3** | FREEZE | This bit is designed to be used with "FIFO stream mode" (register 0x0E bit 5) where the FIFO is configured to continuously capture new samples and flush the oldest after reaching a FIFO full state.<br>0: FIFO operates in standard mode, does not stop capturing data in SWAKE interrupt (default).<br>1: FIFO stops capturing on SWAKE interrupt, software can examine the conditions which generated the SWAKE event. |
| **4** | INTSC_EN | Once an SWAKE interrupt is generated, the SNIFF block stops processing new events until cleared. Enabling this bit allows the SNIFF block to be reset at the same time the INT_SWAKE interrupt is cleared.<br>0: Do not re-arm SNIFF block following a SWAKE event (requires the SNIFF block to be reset by exiting SWAKE mode). (default)<br>1: Clearing the SWAKE interrupt clears and rearms the SNIFF block for subsequent detections (device may stay in SWAKE mode and continuing processing subsequent SWAKE events once interrupt is cleared). |

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| | | |
|---|---|---|
| **5** | SPI3_EN | 0: SPI interface is 4-wire<br>1: SPI interface is 3-wire (DOUT_A1 is the bidirectional pin) |
| **6** | I2C_EN | 0: Device interface is still defined as it was at power-up but no data will appear in XOUT, YOUT and ZOUT registers if both this bit and SPI_EN are set to 0 (default).<br>1: Disables any SPI communications. |
| **7** | SPI_EN | 0: Device interface is still defined as it was at power-up but no data will appear in XOUT, YOUT and ZOUT registers if both this bit and I2C_EN are set to 0 (default).<br>1: Disables any I2C communications. |

**Table 20. Feature Register 1 Settings**

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## 7.8 (0X0E) FEATURE REGISTER 2

This register allows selection of various features for the FIFO, external trigger input, method of interrupt clearing and burst address wrapping.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x0E | FREG_2 | EXT_ TRIG_EN | EXT_ TRIG_POL | FIFO_ STREAM | I2CINT_ WRCLRE | FIFO_ STAT_EN | SPI_ STAT_EN | FIFO_ BURST | WRAPA | 00000000 | RO |

| Bit | Name | Description |
|---|---|---|
| **0** | WRAPA | Burst read address wrap control. This bit determines the "roll-back" or wrap address during burst reads. This bit works in I2C mode and both SPI modes.<br>0: Burst read cycle address wrap address is 0x07, counter automatically returns to 0x02. (default)<br>1: Burst read cycle address wrap address is 0x09, counter automatically returns to 0x02. This setting allows for status registers 0x08 and 0x09 to be included in the burst read. |
| **1** | FIFO_BURST | FIFO burst feature. This bit enables address increment logic which allows extended atomic burst reads of the FIFO greater than the standard 6-byte (3x16 bits) atomic burst read of XYZ data. This bit works in I2C mode and both SPI modes.<br>0: FIFO burst read cycles are 6-bytes in length, 0x02 to 0x07 per read cycle transaction (default).<br>1: FIFO burst read cycle can be any number of 6-byte reads, up to 32 x 6 bytes (i.e. the entire FIFO contents can be read). |

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| | | |
|---|---|---|
| **2** | SPI_STAT_EN | SPI 4-wire mode SPI status token.<br>During the first SPI write cycle from the host, enabling this bit will cause the interface to send out system status information on the DOUT_A1 pin without requiring a separate read cycle. See 6.11 SPI Status Option.<br>0: No SPI status flags are shifted out (default)<br>1: SPI status flags are shifted out on the first byte of all 4-wire SPI transactions (SPI 3-wire and I2C modes are not supported, so no effect will be seen in those modes). |
| **3** | FIFO_STAT_EN | FIFO status token enable. This bit enables a 4-bit FIFO status token to be appended to the top 4 bits of the Z-channel data in every FIFO read cycle. This feature works in I2C mode and both SPI modes. When enabled, the format of the FIFO status token is:<br>0: FIFO status feature is disabled, Z channel FIFO data is not overwritten with FIFO status information. (default)<br>1: FIFO status feature is enabled. When the resolution is less than 14-bits, the top 4-bits of 16-bit Z channel FIFO data are replaced with FIFO status information:<br>{[INT_PEND, FIFO_TH, FIFO_FULL, FIFO_EMPTY], Z[11:0]}<br>When the resolution is 14-bits or above, the bottom 4-bits are replaced:<br>{[ Z[15:4], INT_PEND, FIFO_TH, FIFO_FULL, FIFO_EMPTY]} |
| **4** | I2CINT_WRCLRE | Clear interrupts on register 0x09 write in I2C mode. The default method of interrupt clearing is reading register 0x09, the INT_STATUS or STATUS_2 register. When this bit is enabled, reads to register 0x09 do not clear pending interrupts. SW must write to register 0x09 (contents do not matter) to clear any pending interrupts.<br>**NOTE: In SPI mode this bit has no effect; SPI interrupt clearing requires a write to register 0x09; reads are not supported.**<br>0: In I2C mode, interrupts are cleared when reading register 0x09 (default)<br>1: if I2C_EN is '1', then interrupts are cleared when writing to register 0x09. Otherwise I2C reads to register 0x09 will still clear pending interrupts. |

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| | | |
|---|---|---|
| **5** | FIFO_STREAM | FIFO stream or “continuous” write mode. This bit enables the FIFO to be used as a moving sample buffer, discarding the oldest sample data when the FIFO is full and new sample data arrives. This is intended to work primarily with SWAKE mode, but CWAKE mode is also supported. Note that the FIFO_EN bit must be set to ‘1’ for this bit to function. FIFO stream mode works in I2C mode and both SPI modes.<br>0: FIFO steam mode is disabled, FIFO stops accepting new data when FULL (default)<br>1: FIFO stream mode is enabled, FIFO discards oldest samples once new data arrives |
| **6** | EXT_TRIG_POL | External trigger polarity.<br>0: Trigger polarity is negative edge triggered (default)<br>1: Trigger polarity is positive edge triggered |
| **7** | EXT_TRIG_EN | External trigger mode enable.<br>0: External trigger mode is not enabled (default)<br>1: External trigger mode is enabled, use INTN pin as the external trigger input.<br>This mode is not used with the TRIG_CMD bit in Register 0x10 bit 7. To use this mode, set the TRIG mode in Register 0x10 bits [2:0]. |

**Table 21. Feature Register 2 Settings**

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## 7.9 (0X0F) INITIALIZATION REGISTER 1

Software must write a fixed value to this register immediately after power-up or reset. This register will not typically read-back the value which was written (see below).

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x0F | INIT_1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | (See note) | W |

Note: During the internal chip start-up sequence, the read-back value will be 0x45. The read-back value will become 0x40 after the start-up sequence completes. After the initialization value of 0x42 is written, the read-back value will be 0x43.

| Bit | Name | Description |
|---|---|---|
| **[7:0]** | **INIT_1** | **Software must write a value of 0x42.** |

**Table 22. Initialization Register 1 Settings**

MEMSIC

## 7.10 (0X10) MODE CONTROL REGISTER

This register is the primary control register for the accelerometer. The operational mode of the device, X/Y/Z axis enables, and the TRIG one-shot mode can be written through this register. The mode transitions controlled by this register may take up to 3 transitions of the heartbeat clock. Depending on the operation, the lower 3-bits (MCTRL[2:0]) may be automatically set or cleared by hardware if auto-triggered events are executed.

In general, when software sets an operational mode using the MCTRL [2:0] bits, there might be a delay time of 2 to 10 mSec before the operational mode is reflected by the MODE[2:0] bits in Status Register 1.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x10 | MODE_C | Mode Control | TRIG_ CMD | Z_AXIS_PD | Y_AXIS_PD | X_AXIS_PD | RESV | MCTRL[2] | MCTRL[1] | MCTRL[0] | 0x00 | W |

| Bit | Name | Description | | |
|---|---|---|---|---|
| **[2:0]** | MCTRL[2:0] | **Bit Field** | **Mode** | **Comments** |
| | | 000 | SLEEP | Lowest power mode, regulators on, no clock activity, partial chip power-down. |
| | | 001 | STANDBY | Low power mode, no sampling, clocks active. |
| | | 010 | SNIFF | Sniff activity detection mode, sniff enabled, no sampling, no FIFO operations, automatically transition to CWAKE mode upon activity detection. |
| | | 011 | Reserved | Reserved |
| | | 100 | Reserved | Reserved |
| | | 101 | CWAKE | Continuous wake. Active XYZ sampling. Sniff circuitry not active. |

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| | | | | |
|---|---|---|---|---|
| | | 110 | SWAKE | Use Sniff logic, main XYZ pipeline and optional FIFO at the same time; highest power consumption |
| | | 111 | TRIG | Trigger mode, 1 to 254 samples or continuous, return to sleep upon completion. |
| **3** | RESV | Reserved | | |
| **4** | X_AXIS_PD | 0: X-axis is enabled.<br>1: X-axis is disabled. | | |
| **5** | Y_AXIS_PD | 0: Y-axis is enabled.<br>1: Y-axis is disabled. | | |
| **6** | Z_AXIS_PD | 0: Z-axis is enabled.<br>1: Z-axis is disabled. | | |
| **7** | TRIG_CMD | Setting this bit will execute a one-shot trigger mode where 1 to 254 samples are acquired (or the device will continuously sample if the value is 255). The number of samples is specified by the TRIG_COUNT in register 0x29. TRIG mode can only be started from STANDBY. Unless the value is 255, after the number of samples is completed, the device will return to STANDBY mode. | | |

**Table 23. Mode Control Register Settings**

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## 7.11 (0X11) RATE REGISTER 1

This register configures the sample rates for wake modes. The rates also depend upon the value in register 0x1C. The device has several power modes which can be adjusted to achieve a desired power consumption at a certain ODR. The tradeoff for lower power is either higher noise or lower ODR. See the table below.

**NOTE: The power mode bits referenced in 0x1C are different than for the SNIFF rates.**

**NOTE: Software must set bits[7:4] to 0.**

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x11 | RATE_1 | 0 | 0 | 0 | 0 | RR[3] | RR[2] | RR[1] | RR[0] | 00000000 | RW |

| Register 0x11 Value | Ultra-Low Power (0x1C[2:0]=>0x03) | | Low Power (0x1C[2:0]=>0x00) | | Precision (0x1C[2:0]=>0x04) | |
|---|---|---|---|---|---|---|
| | CWAKE ODR (Hz) | Current (µA) | CWAKE ODR (Hz) | Current (µA) | CWAKE ODR (Hz) | Current (µA) |
| 0x05 | n/a | | 14 | 1 | 14 | 5 |
| 0x06 | 25 | 0.9 | 28 | 1.6 | 28 | 10 |
| 0x07 | 50 | 1.6 | 54 | 2.7 | 55 | 18 |
| 0x08 | 100 | 2.8 | 105 | 5 | 80 | 25 |
| 0x09 | 190 | 5.5 | 210 | 11 | n/a | |
| 0x0A | 380 | 10 | 400 | 19 | n/a | |
| 0x0B | 750 | 18 | 600 | 26 | n/a | |
| 0x0C | 1100 | 26 | n/a | | n/a | |
| 0x0F*NOTE | 1300 | 36 | 750 | 36 | 100 | 36 |

**Table 24. Rate Register 1 Settings**

**NOTE:** Specific setup steps are required in order to set up Register 0x11 value 0x0F (“Rate 15”), as shown below. These steps are not required when using the other modes:

MEMSIC

| Step | Write Register Address | Values To Be Written | | | Comment |
|---|---|---|---|---|---|
| | | ULP | LP | Precision | |
| **1** | 0x10 | 0x01 | | | Go to standby |
| **2** | 0x15 | (0x04 or other) | | | <desired range & resolution> |
| **3** | 0x16 | (0x5D or other) | | | <desired FIFO settings> |
| **4** | 0x1C | 0x03 | 0x00 | 0x04 | Choose mode |
| **5** | 0x11 | 0x10 | | | Point to set wake/sniff settings |
| **6** | 0x29 | 0x03 | | | Rate 15 setup 1 for CWAKE |
| **7** | 0x11 | 0x20 | | | Rate 15 setup 2 for CWAKE |
| **8** | 0x29 | 0x01 | | | Rate 15 setup 3 for CWAKE |
| **9** | 0x11 | 0x40 | | | Point to value 1 |
| **10** | 0x29 | 0x52 | 0x72 | 0x32 | Write value 1 |
| **11** | 0x11 | 0x50 | | | Point to value 2 |
| **12** | 0x29 | 0x01 | 0x02 | 0x12 | Write value 2 |
| **13** | 0x11 | 0x0F | | | Apply the values |
| **14** | 0x10 | 0x05 | | | Go to CWAKE |

**Table 25. Setup Steps for CWAKE Using "Rate 15"**

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## 7.12 (0X12) SNIFF CONTROL REGISTER

This register selects the sample rate for SNIFF mode and the clock rate for STANDBY mode.

**NOTE: The power mode bits referenced in 0x1C are different than for the WAKE rates.**

**NOTE: Software must always write 0 to bit 4.**

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x12 | SNIFF_C | STB_RATE[2] | STB_RATE[1] | STB_RATE[0] | 0 | SNIFF_SR[3] | SNIFF_SR[2] | SNIFF_SR[1] | SNIFF_SR[0] | 00000000 | RW |

| Bit | Name | Description | | | |
|---|---|---|---|---|---|
| [3:0] | SNIFF_SR[3:0] | Approximate typical maximum clock rate when trigger count > 1 (Hz) | | | |
| | | Bit Field | Ultra-Low Power (0x1C[6:4]=>0x03) | Low Power (0x1C[6:4]=>0x00) | Precision (0x1C[6:4]=>0x04) |
| | | 0000 (default) | 6 | 7 | 7 |
| | | 0001 | 0.4 | 0.4 | 0.2 |
| | | 0010 | 0.8 | 0.8 | 0.4 |
| | | 0011 | 1.5 | 1.5 | 0.9 |
| | | 0100 | 6 | 7 | 7 |
| | | 0101 | 13 | 14 | 14 |
| | | 0110 | 25 | 28 | 28 |
| | | 0111 | 50 | 54 | 55 |
| | | 1000 | 100 | 105 | 80 |
| | | 1001 | 190 | 210 | n/a |
| | | 1010 | 380 | 400 | n/a |
| | | 1011 | 750 | 600 | n/a |

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| | | | | | |
|---|---|---|---|---|---|
| | | 1100 | 1100 | n/a | n/a |
| | | 1101 | n/a | n/a | n/a |
| | | 1110 | n/a | n/a | n/a |
| | | 1111*NOTE | 1300 | 750 | 100 |
| **4** | 0 | **Software must always write 0 to this bit.** | | | |
| **[7:5]** | STB_RATE[2:0] | **Approximate typical maximum clock rate when trigger count > 1 (Hz)** | | | |
| | | **Bit Field** | **Ultra-Low Power (0x1C[6:4]=>0x03)** | **Low Power (0x1C[6:4]=>0x00)** | **Precision (0x1C[6:4]=>0x04)** |
| | | 000 (default) | 1 | 0.5 | 0.1 |
| | | 001 | 3 | 1 | 0.2 |
| | | 010 | 5 | 3 | 0.4 |
| | | 011 | 10 | 6 | 0.8 |
| | | 100 | 23 | 12 | 1.5 |
| | | 101 | 45 | 24 | 3 |
| | | 110 | 90 | 48 | 5 |
| | | 111 | 180 | 100 | 10 |

**Table 26. Sniff Control Register Settings**

**NOTE:** Specific setup steps are required in order to set up Register 0x12 value 0x0F (“Rate 15”) for sniff, as shown below. These steps are not required when using the other modes:

MEMSIC

| Step | Write Register Address | Values To Be Written | | | Comment |
|---|---|---|---|---|---|
| | | ULP | LP | Precision | |
| **1** | 0x10 | 0x01 | | | Go to standby |
| **2** | 0x15 | (0x04 or other) | | | <desired range & resolution> |
| **3** | 0x16 | (0x5D or other) | | | <desired FIFO settings> |
| **4** | 0x1C | 0x30 | 0x00 | 0x40 | Choose mode |
| **5** | 0x11 | 0x10 | | | Point to set wake/sniff settings |
| **6** | 0x29 | 0x30 | | | Rate 15 setup 1 for sniff |
| **7** | 0x11 | 0x30 | | | Rate 15 setup 2 for sniff |
| **8** | 0x29 | 0x01 | | | Rate 15 setup 3 for sniff |
| **9** | 0x11 | 0x60 | | | Point to value 1 |
| **10** | 0x29 | 0x52 | 0x72 | 0x32 | Write value 1 |
| **11** | 0x11 | 0x70 | | | Point to value 2 |
| **12** | 0x29 | 0x01 | 0x02 | 0x12 | Write value 2 |
| **13** | 0x11 | 0x0F | | | Apply the values |
| **14** | 0x10 | 0x02 | | | Go to sniff |

**Table 27. Setup Steps For Sniff Using "Rate 15"**

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## 7.13 (0X13) SNIFF THRESHOLD CONTROL REGISTER

This register sets the threshold values used by the SNIFF logic for activity detection. For each axis, a delta count is generated and compared to the threshold. When the delta count is greater than the threshold, a SNIFF wakeup event occurs. There is a unique sniff threshold for each axis, and an optional “false detection count” which requires multiple sniff detection events to occur before a wakeup condition is declared. These features are set by six shadow registers accessed by register 0x13[5:0] and register 0x14 bits [2:0].

The SNIFF block supports the logical AND or OR of the X/Y/Z SNIFF wakeup flags when generating a SNIFF wakeup interrupt.

The SNIFF block supports two methods of calculating SNIFF delta counts:

- Current Sample to Previous Sample (C2P)
  - The current sample and the immediate previous sample are subtracted to generate a delta
- Current Sample to Baseline (C2B)
  - The current sample and the first sample captured when entering SNIFF mode are subtracted to generate a delta.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x13 | SNIFFTH_C | SNIFF_ MODE | SNIFF_ AND_OR | SNIFF_TH[5] | SNIFF_TH[4] | SNIFF_TH[3] | SNIFF_TH[2] | SNIFF_TH[1] | SNIFF_TH[0] | 00000000 | RW |

| Bit | Name | Description | |
|---|---|---|---|
| **[5:0]** | SNIFF_TH[5:0] | This 6-bit field accesses six shadow registers behind address 0x13. Register 0x14 bits [2:0] control which register is accessed. | |
| | | **Reg 0x14 SNIFF_T_ADDR[2:0]** | **Reg 0x13 SNIFF_TH[5:0]** |
| | | 000 | None |
| | | 001 | SNIFF Threshold, X-axis<br>SNIFF_TH_X[5:0], unsigned threshold value 0 to 63 (independent from Y and Z thresholds). |

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| | | | |
|---|---|---|---|
| | | 010 | SNIFF Threshold, Y-axis<br>SNIFF_TH_Y[5:0], unsigned threshold value 0 to 63 (independent from X and Z thresholds). |
| | | 011 | SNIFF Threshold, Z-axis<br>SNIFF_TH_Z[5:0], unsigned threshold value 0 to 63 (independent from X and Y thresholds). |
| | | 100 | None |
| | | 101 | SNIFF Detection Count, X-axis<br>SNIFF_X_COUNT[5:0], unsigned SNIFF event count, 1 to 62 events, independent from other channels. The detection count is COUNT-1 for the desired number of events (for 1 event = 1-1 => 0 loaded into register). |
| | | 110 | SNIFF Detection Count, Y-axis<br>SNIFF_Y_COUNT[5:0], unsigned SNIFF event count, 1 to 62 events, independent from other channels. The detection count is COUNT-1 for the desired number of events (for 1 event = 1-1 => 0 loaded into register). |
| | | 111 | SNIFF Detection Count, Z-axis<br>SNIFF_Z_COUNT[5:0], unsigned SNIFF event count, 1 to 62 events, independent from other channels. The detection count is COUNT-1 for the desired number of events (for 1 event = 1-1 => 0 loaded into register). |

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| | | |
|---|---|---|
| **6** | SNIFF_AND_OR | Sets the logical mode for combining of X/Y/Z SNIFF wakeup events before an interrupt is generated. To remove one of the channels (axis) from the equation, use the corresponding axis PD bit in register 0x10 bits [6:4].<br>0: OR - SNIFF wakeup/interrupt is triggered when any of the active channels have met detection threshold and count requirements (default).<br>Sniff Wakeup = Δ(abs(X) – X Sniff Threshold) or<br>Δ(abs(Y) – Y Sniff Threshold) or<br>Δ(abs(Z) – Z Sniff Threshold)<br>1: AND - SNIFF wakeup/interrupt is triggered when all active channels have met detection threshold and count requirements.<br>Sniff Wakeup = Δ(abs(X) – X Sniff Threshold) and<br>Δ(abs(Y) – Y Sniff Threshold) and<br>Δ(abs(Z) – Z Sniff Threshold) |
| **7** | SNIFF_MODE | This bit determines how the SNIFF block computes its delta count.<br>0: C2P Mode (Current to Previous): The delta count between current and previous samples is a moving window. The SNIFF logic uses the current sample and the immediate previous sample to compute a delta (default).<br>1: C2B Mode (Current to Baseline): The delta count is generated from subtracting the current sample from the first sample stored when entering SNIFF mode. |

**Table 28. Sniff Threshold Control Register Settings**

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## 7.14 (0X14) SNIFF CONFIGURATION REGISTER

This register selects which of the six shadow registers is being accessed in register 0x13, and controls settings of the SNIFF hardware.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x14 | SNIFFCF_C | SNIFF_ RESET | SNIFF_ MUX[2] | SNIFF_ MUX[1] | SNIFF_ MUX[0] | SNIFF_ CNTEN | SNIFF_ THADR[2] | SNIFF_ THADR[1] | SNIFF_ THADR[0] | 00000 000 | RW |

| Bit | Name | Description | |
|---|---|---|---|
| **[2:0]** | SNIFF_ THADR[2:0] | **Bit Field** | **Register selected by 0x13[5:0]** |
| | | 000 | None |
| | | 001 | SNIFF Threshold, X-axis |
| | | 010 | SNIFF Threshold, Y-axis |
| | | 011 | SNIFF Threshold, Z-axis |
| | | 100 | None |
| | | 101 | SNIFF Detection Count, X-axis |
| | | 110 | SNIFF Detection Count, Y-axis |
| | | 111 | SNIFF Detection Count, Z-axis |
| **3** | SNIFF_ CNTEN | This bit enables the SNIFF detection counts for all channels.<br>0: Do not use SNIFF detection counters. (default)<br>1: Enable SNIFF detection counts, required for valid SNIFF wakeup | |
| **[6:4]** | SNIFF_ MUX[2:0] | This field determines which 6-bits of the 11-bit delta count will be compared against the 6-bit threshold value for each channel. Clamp logic allows any SNIFF delta exceeding the selected 6-bit range to still be detected as a valid event. See examples below. | |

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| | | Bit Field | Bit range selected |
|---|---|---|---|
| | | 000 | DELTA[5:0] |
| | | 001 | DELTA[6:1] |
| | | 010 | DELTA[7:2] |
| | | 011 | DELTA[8:3] |
| | | 100 | DELTA[9:4] |
| | | 101 | DELTA[10:5] |
| | | 110 | DELTA[10:5] |
| | | 111 | DELTA[10:5] |
| **7** | SNIFF_ RESET | This is the manual reset bit for the SNIFF block. This bit is not self-clearing, and can be used to re-enable the SNIFF block after a SNIFF event has been detected in SWAKE mode.<br>0: SNIFF block reset is not applied (default).<br>1: SNIFF block reset is applied. | |

**Table 29. Sniff Configuration Register Settings**

Some example settings for the SNIFF_MUX field are shown below:

| Sniff Noise/Power Configuration | Δg | Threshold [5:0] | Sniff Mux Sel [2:0] | Example Use Case |
|---|---|---|---|---|
| Ultra-Low Power | Low | 3 | 0 | Human motion detection @ SR = 6.5 Hz and Sniff Mode = “Current to Baseline” |
| | Med | 10 | 0 | |
| | High | 28 | 0 | Tap detection @ SR = 51 Hz and Sniff Mode = “Current to Previous” |
| Low Power | Low | 5 | 0 | |
| | Med | 5 | 0 | |
| | High | 56 | 0 | |
| Precision | X Low | 3 | 0 | |
| | Low | 37 | 0 | |
| | Med | 37 | 2 | |
| | High | 56 | 3 | |

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## 7.15 (0X15) RANGE AND RESOLUTION CONTROL REGISTER

The RANGE register sets the resolution and range options for the accelerometer. All numbers are sign-extended, 2's complement format. All results are reported in registers 0x02 to 0x07.

When the FIFO is enabled, only 6 to 12-bit resolutions are supported due to the 12-bit width of the FIFO.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x15 | RANGE_C | RESV | RANGE[2] | RANGE[1] | RANGE[0] | RESV | RES[2] | RES[1] | RES[0] | 00000000 | RW |

| Bit | Name | Description | |
|---|---|---|---|
| **[2:0]** | RES[2:0] | **Bit Field** | **Bit Width of Accelerometer Data** |
| | | 000 | 6 bits |
| | | 001 | 7 bits |
| | | 010 | 8 bits |
| | | 011 | 10 bits |
| | | 100 | 12 bits |
| | | 101 | 14 bits (only 12-bits if FIFO enabled) |
| | | 110 | Reserved |
| | | 111 | Reserved |
| **3** | RESV | Reserved | |
| **[6:4]** | RANGE[2:0] | **Bit Field** | **G Range Selection** |
| | | 000 | ±2g |
| | | 001 | ±4g |
| | | 010 | ±8g |
| | | 011 | ±16g |

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| | | | |
|---|---|---|---|
| | | 100 | ±12g |
| | | 101 | Reserved |
| | | 110 | Reserved |
| | | 111 | Reserved |
| **7** | RESV | Reserved | |

**Table 30. Range and Resolution Control Register Settings**

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## 7.16 (0X16) FIFO CONTROL REGISTER

This register selects the FIFO threshold level, operation mode, FIFO reset and enable. With the exception of FIFO_RESET, the FIFO_EN bit must be '1' for any FIFO interrupts, thresholds, or modes to be enabled. The FIFO flags in register 0x08 will continue to report FIFO defaults even if the FIFO_EN is '0'.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x16 | FIFO_C | FIFO_ RESET | FIFO_EN | FIFO_ MODE | FIFO_TH [4] | FIFO_TH [3] | FIFO_TH [2] | FIFO_TH [1] | FIFO_TH [0] | 00000000 | RW |

| Bit | Name | Description |
|---|---|---|
| **[4:0]** | FIFO_TH[4:0] | The FIFO threshold level selects the number of samples in the FIFO for different FIFO events. The threshold value may be 1 to 31 (00001 to 11111). |
| **5** | FIFO_MODE | 0: Normal operation, the FIFO continues to accept new sample data as long as there is space remaining (default)<br>1: Watermark, once the amount of samples in the FIFO reaches or exceeds the threshold level, the FIFO stops accepting new sample data. Any additional sample data is "dropped". |
| **6** | FIFO_EN | FIFO enable control. All FIFO operations are gated by this bit.<br>0: No FIFO operation, sample data written directly to output registers.<br>1: FIFO enabled, all sample data written to FIFO write port if there is room. The FIFO write clock is controlled by this enable, resulting in higher dynamic power. |
| **7** | FIFO_RESET | Asynchronous FIFO reset.<br>0: FIFO reset is disabled, normal operation (default)<br>1: FIFO read and write pointers are cleared, FIFO contents returned to 0 |

**Table 31. FIFO Control Register Settings**

MEMSIC

## 7.17 (0X17) INTERRUPT CONTROL REGISTER

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x17 | INTR_C | INT_ SWAKE | INT_FIFO_ THRESH | INT_FIFO_ FULL | INT_FIFO_ EMPTY | INT_ACQ | INT_ WAKE | IAH | IPP | 00000000 | RW |

| Bit | Name | Description |
|---|---|---|
| **0** | IPP | INTN pin interrupt pin mode control.<br>0: INTN pin is configured for open-drain mode (external pullup to VDDIO required) (default).<br>1: INTN pin is configured for active drive or “push-pull” mode. Drive level is to VDDIO. |
| **1** | IAH | Interrupt level control, sets the active drive level of the INTN pin.<br>0: Interrupt request is active low (default).<br>1: Interrupt request is active high. |
| **2** | INT_WAKE | WAKE interrupt (SNIFF to WAKE) enable<br>0: No interrupt is generated when SNIFF activity is detected and the device auto-transitions to CWAKE mode (default).<br>1: Generate an interrupt when activity is detected in SNIFF mode and the device auto-transitions to CWAKE mode. |
| **3** | INT_ACQ | Interrupt on sample or acquisition enable<br>0: No interrupt generated when new sample data is acquired (default).<br>1: Generate an interrupt when new sample data is acquired (applies to new data written to output registers or FIFO). This enable is paired with the NEW_DATA flag in register 0x08. |
| **4** | INT_FIFO_EMPTY | FIFO empty interrupt enable.<br>0: No interrupt is generated when the FIFO is empty or completely drained of sample data (default).<br>1: Generate an interrupt when the FIFO is empty. This interrupt is paired with the FIFO_EMPTY flag in register 0x08. Note that this interrupt is independent of the FIFO threshold level, and will only activate when the FIFO sample count has reached a value of 0. |

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| | | |
|---|---|---|
| **5** | INT_FIFO_FULL | FIFO full interrupt enable.<br>0: No interrupt is generated when the FIFO is empty or completely filled of sample data (default).<br>1: Generate an interrupt when the FIFO is full. This interrupt is paired with the FIFO_FULL flag in register 0x08. Note that this interrupt is independent of the FIFO threshold level, and will only activate when the FIFO sample count has reached a value of 32. |
| **6** | INT_FIFO_THRESH | FIFO threshold interrupt enable.<br>0: No interrupt is generated when the FIFO threshold level is reached (default).<br>1: Generate an interrupt when the FIFO threshold level is reached. |
| **7** | INT_SWAKE | This interrupt is valid only in SWAKE mode.<br>0: No interrupt generated when SNIFF activity is detected (default).<br>1: Generate an interrupt when SNIFF activity is detected. |

**Table 32. Interrupt Control Register Settings**

MEMSIC

## 7.18 (0X1A) INITIALIZATION REGISTER 3

Software must write a fixed value to this register immediately after power-up or reset.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x1A | INIT_3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00000000 | RW |

| Bit | Name | Description |
|---|---|---|
| **[7:0]** | INIT_3 | Software must write ‘0’ to these bits |

**Table 33. Initialization Register 3 Settings**

MEMSIC

## 7.19 (0X1B) SCRATCHPAD REGISTER

This register can store any 8-bit value and has no effect on hardware.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x1B | SCRATCH | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00000000 | RW |

| Bit | Name | Description |
|---|---|---|
| **[7:0]** | SCRATCH | Any value can be written and read-back. |

**Table 34. Scratchpad Register**

MEMSIC

## 7.20 (0X1C) POWER MODE CONTROL REGISTER

This register selects the power setting for CWAKE, SWAKE and SNIFF modes.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x1C | PMCR | SPI_HS_EN | SPM[2] | SPM[1] | SPM[0] | RESV | CSPM[2] | CSPM[1] | CSPM[0] | 00000000 | RW |

| Bit | Name | Description |
|---|---|---|
| **[2:0]** | CSPM | **CWAKE, SWAKE Power Mode**<br>000: Low Power Mode (nominal noise levels) (default)<br>001: Reserved<br>010: Reserved<br>011: Ultra-Low Power Mode (highest noise levels)<br>100: Precision Mode (lowest noise levels)<br>101: Reserved<br>110: Reserved<br>111: Reserved |
| **3** | RESV | Reserved |
| **[6:4]** | SPM | **SNIFF Power Mode**<br>000: Low Power Mode (nominal noise levels) (default)<br>001: Reserved<br>010: Reserved<br>011: Ultra-Low Power Mode (highest noise levels)<br>100: Precision Mode (lowest noise levels)<br>101: Reserved<br>110: Reserved<br>111: Reserved |
| **7** | SPI_HS_EN | **SPI High-Speed Enable**<br>0: This bit will always return a '0' when read. Software must keep track of the state of this bit. |

MEMSIC

| | | |
|---|---|---|
| | | Follow sequence from 6.12 SPI High-Speed Mode to enable high-speed SPI mode. |

**Table 35. Power Mode Control Register Settings**

MEMSIC

## 7.21 (0X20) DRIVE MOTION X REGISTER

This register controls the test mode which moves the sensor in the X axis direction and initializes specific hardware bits.

**NOTE: Software must always write 0 to bits [7:4] and 1.**

**NOTE: Software must always write 1 to bit 0.**

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x20 | DMX | 0 | 0 | 0 | 0 | DNX | DPX | 0 | 1 | 00000000 | W |

| Bit | Name | Description |
|---|---|---|
| **0** | 1 | **Reserved. Always write 1 to this bit** |
| **1** | 0 | **Reserved. Always write 0 to this bit.** |
| **2** | DPX | 0: Disabled (default)<br>1: Move the sensor in X Positive direction |
| **3** | DNX | 0: Disabled (default)<br>1: Move the sensor in X Negative direction |
| **[7:4]** | 0000 | **Reserved. Always write 0 to these bits.** |

**Table 36. Drive Motion X Register Settings**

MEMSIC

## 7.22 (0X21) DRIVE MOTION Y REGISTER

This register controls the test mode which moves the sensor in the Y axis direction and initializes specific hardware bits.

**NOTE: Software must always write 0 to bits [6:4] and [1:0].**

**NOTE: Software must always write 1 to bit 7 after writing to register 0x20[0].**

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x21 | DMY | 1 | 0 | 0 | 0 | DNY | DPY | 0 | 0 | (See table) | RW |

| Mode (MCTLR[2:0] bits in MODE_C Register 0x10) | Read-back Value |
|---|---|
| **SNIFF, CWAKE, SWAKE, TRIG** | 0x80 |
| **SLEEP, STANDBY** | 0x00 |

**Table 37. Register 0x21 Read-Back Value**

| Bit | Name | Description |
|---|---|---|
| **[1:0]** | 00 | **Reserved. Always write 0 to these bits.** |
| **2** | DPY | 0: Disabled (default)<br>1: Move the sensor in Y Positive direction |
| **3** | DNY | 0: Disabled (default)<br>1: Move the sensor in Y Negative direction |
| **[6:4]** | 000 | **Reserved. Always write 0 to these bits.** |
| **7** | 1 | **Reserved. Always write 1 to this bit.** |

**Table 38. Drive Motion Y Register Settings**

MEMSIC

## 7.23 (0X22) DRIVE MOTION Z REGISTER

This register controls the test mode which moves the sensor in the Z axis direction.

**NOTE: Software must always write 0 to bits [7:4] and [1:0].**

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x22 | DMZ | 0 | 0 | 0 | 0 | DNZ | DPZ | 0 | 0 | 00000000 | RW |

| Bit | Name | Description |
|---|---|---|
| **[1:0]** | 00 | **Reserved. Always write 0 to these bits.** |
| **2** | DPZ | 0: Disabled (default)<br>1: Move the sensor in Z Positive direction |
| **3** | DNZ | 0: Disabled (default)<br>1: Move the sensor in Z Negative direction |
| **[7:4]** | 0000 | **Reserved. Always write 0 to these bits.** |

**Table 39. Drive Motion Z Register Settings**

MEMSIC

## 7.24 (0X24) RESET REGISTER

This register can be used to reset the device. Anytime there is a reset to the device, a POR event, or a power cycle the SPI 3-wire configuration will reset to 4-wire mode.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x24 | RESET | RELOAD | RESET | RESV | RESV | RESV | RESV | RESV | RESV | 00000000 | RW |

| Bit | Name | Description |
|---|---|---|
| **[5:0]** | Reserved | Reserved |
| **6** | RESET | 0: Normal operation (default)<br>1: Force a power-on-reset (POR) sequence.<br>OTP contents are reloaded into registers, AOFS contents are decompressed, and any other registers are returned to their default. This bit is self-clearing. |
| **7** | RELOAD | 0: Normal operation (default)<br>1: Reloads the registers from OTP.<br>A RELOAD operation enables OTP core for reading, performs a complete read of OTP into the register file, and then disables the OTP. Use register 0x01 bit 5 to monitor the OTP_BUSY bit. This bit must be cleared by software |

**Table 40. Reset Register Settings**

MEMSIC

## 7.25 (0X28) INITIALIZATION REGISTER 2

Software must write a fixed value to this register immediately after power-up or reset.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x28 | INIT_2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00000000 | RW |

| Bit | Name | Description |
|---|---|---|
| [7:0] | INIT_2 | Software must write '0' to these bits |

**Table 41. Initialization Register 2 Settings**

MEMSIC

## 7.26 (0X29) TRIGGER COUNT REGISTER

This register selects the number of samples to be taken after the one-shot trigger is started.

| Addr | Name | Bit | | | | | | | | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x29 | TRIGC | TRIGC[7] | TRIGC[6] | TRIGC[5] | TRIGC[4] | TRIGC[3] | TRIGC[2] | TRIGC[1] | TRIGC[0] | 00000000 | RW |

| Bit | Name | Description |
|---|---|---|
| **[7:0]** | TRIGC[7:0] | Selects the number of samples to be captured after the one-shot trigger is started. Range from 1 to 254. When value 255 is chosen, the device will run continuously until the mode in register 0x10 is changed. |

**Table 42. Trigger Register Settings**

MEMSIC

## 7.27 (0X2A – 0X2B) X-AXIS OFFSET REGISTERS

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the acceleration values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x2A | XOFFL | **XOFF[7]** | **XOFF[6]** | **XOFF[5]** | **XOFF[4]** | **XOFF[3]** | **XOFF[2]** | **XOFF[1]** | **XOFF[0]** | Per chip | W |
| 0x2B | XOFFH | XGAIN[8] | **XOFF[14]** | **XOFF[13]** | **XOFF[12]** | **XOFF[11]** | **XOFF[10]** | **XOFF[9]** | **XOFF[8]** | Per chip | W |

**Table 43. X-Axis Offset Registers**

MEMSIC

## 7.28 (0X2C – 0X2D) Y-AXIS OFFSET REGISTERS

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the acceleration values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x2C | YOFFL | **YOFF[7]** | **YOFF[6]** | **YOFF[5]** | **YOFF[4]** | **YOFF[3]** | **YOFF[2]** | **YOFF[1]** | **YOFF[0]** | Per chip | W |
| 0x2D | YOFFH | YGAIN[8] | **YOFF[14]** | **YOFF[13]** | **YOFF[12]** | **YOFF[11]** | **YOFF[10]** | **YOFF[9]** | **YOFF[8]** | Per chip | W |

**Table 44. Y-Axis Offset Registers**

MEMSIC

## 7.29 (0X2E – 0X2F) Z-AXIS OFFSET REGISTERS

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the acceleration values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x2E | ZOFFL | **ZOFF[7]** | **ZOFF[6]** | **ZOFF[5]** | **ZOFF[4]** | **ZOFF[3]** | **ZOFF[2]** | **ZOFF[1]** | **ZOFF[0]** | Per chip | W |
| 0x2F | ZOFFH | ZGAIN[8] | **ZOFF[14]** | **ZOFF[13]** | **ZOFF[12]** | **ZOFF[11]** | **ZOFF[10]** | **ZOFF[9]** | **ZOFF[8]** | Per chip | W |

**Table 45. Z-Axis Offset Registers**

MEMSIC

## 7.30 (0X2B & 0X30) X-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x2B | XOFFH | **XGAIN[8]** | XOFF[14] | XOFF[13] | XOFF[12] | XOFF[11] | XOFF[10] | XOFF[9] | XOFF[8] | Per chip | W |
| 0x30 | XGAIN | **XGAIN[7]** | **XGAIN[6]** | **XGAIN[5]** | **XGAIN[4]** | **XGAIN[3]** | **XGAIN[2]** | **XGAIN[1]** | **XGAIN[0]** | Per chip | W |

**Table 46. X-Axis Gain Registers**

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## 7.31 (0X2D & 0X31) Y-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x2D | YOFFH | **YGAIN[8]** | YOFF[14] | YOFF[13] | YOFF[12] | YOFF[11] | YOFF[10] | YOFF[9] | YOFF[8] | Per chip | W |
| 0x31 | YGAIN | **YGAIN[7]** | **YGAIN[6]** | **YGAIN[5]** | **YGAIN[4]** | **YGAIN[3]** | **YGAIN[2]** | **YGAIN[1]** | **YGAIN[0]** | Per chip | W |

**Table 47. Y-Axis Gain Registers**

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## 7.32 (0X2F & 0X32) Z-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x2F | ZOFFH | **ZGAIN[8]** | ZOFF[14] | ZOFF[13] | ZOFF[12] | ZOFF[11] | ZOFF[10] | ZOFF[9] | ZOFF[8] | Per chip | W |
| 0x32 | ZGAIN | **ZGAIN[7]** | **ZGAIN[6]** | **ZGAIN[5]** | **ZGAIN[4]** | **ZGAIN[3]** | **ZGAIN[2]** | **ZGAIN[1]** | **ZGAIN[0]** | Per chip | W |

**Table 48. Z-Axis Gain Registers**

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# 9 REVISION HISTORY

| Date | Revision | Description |
|---|---|---|
| 2015-10 | APS-048-0044v1.0 | First release. |
| 2015-12 | APS-048-0044v1.1 | Added register details. |
| 2015-12 | APS-048-0044v1.2 | Updated SPI clock speed parameters. Corrected pinouts in table. Added scratchpad register. Corrected some typos. |
| 2016-02 | APS-048-0044v1.3 | Updated 5.3 initialization sequence. Updated Rate 15 sequences for CWAKE and SNIFF. |
| 2017-03 | APS-048-0044v1.4 | Updated SPI clock speed and added description of sequence. |
| 2017-09 | APS-048-0044v1.5 | • Added soldering profile, shipping and handling guidelines, moisture sensitivity level control<br>• Fixed a typo by changing “Sensitivity Temperature Coefficient” from 0.15 to 0.015 %/$^0$C<br>• Updated Zero-g Offset condition |
| 2019-02 | APS-048-0044v1.6 | • Updated SPI initialization sequence (Table 11) |
| 2019-11 | APS-048-0044v1.7 | • Add MSL3 spec to section 3.8. |
| 2020-06 | APS-048-0044v1.8 | • Change to MEMSIC format based on the License Agreement with mCube |

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