Wide Bandwidth Yaw Rate Gyroscope with SPI

Data Sheet

ADIS16060

FEATURES

- Complete angular rate digital gyroscope
  - 14-bit resolution
- Scalable measurement range
  - Initial range: ±80°/sec (typical)
  - Increase range with external resistor
- Z-axis (yaw rate) response
- SPI digital output interface
- High vibration rejection over wide frequency
- 2000 g-powered shock survivability
- 1 kHz bandwidth
  - Selectable using external capacitor
- Externally controlled self-test
- Internal temperature sensor output
- Dual auxiliary 14-bit ADC inputs
- Absolute rate output for precision applications
- 5 V single-supply operation
- 8.2 mm × 8.2 mm × 5.2 mm package
- –40°C to +105°C operation
- RoHS compliant

APPLICATIONS

- Platform stabilization
- Image stabilization
- Guidance and control
- Inertial measurement units
- Robotics

GENERAL DESCRIPTION

The ADIS16060 is a yaw rate gyroscope with an integrated serial peripheral interface (SPI). It features an externally selectable bandwidth response and scalable dynamic range.

The SPI port provides access to the rate sensor, an internal temperature sensor, and two external analog signals (using internal ADC). The digital data available at the SPI port is proportional to the angular rate about the axis that is normal to the top surface of the package.

An additional output pin provides a precision voltage reference. A digital self-test function electromechanically excites the sensor to test the operation of the sensor and the signal-conditioning circuits.

The ADIS16060 is available in an 8.2 mm × 8.2 mm × 5.2 mm, 16-terminal, peripheral land grid array (LGA) package.

FUNCTIONAL BLOCK DIAGRAM

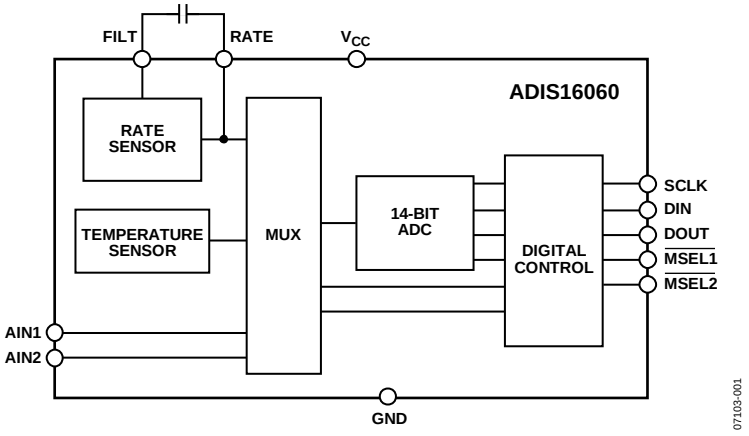


Figure 1.

Rev. A
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REVISION HISTORY

4/12—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Applications Section ... 1
Changes to Note 1 in Figure 4 ... 7
Changes to Supply and Common Considerations Section, Setting Bandwidth Section, and Figure 14 Caption ... 11

1/08—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{CC} = 5 V, angular rate = 0°/sec, C_{OUT} = 0.01 µF, ±1 g, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min[1]	Typ	Max	Unit
SENSITIVITY					
Dynamic Range[2]	Full-scale range over specifications range	±50	±80		°/sec
Initial	Clockwise rotation is positive output, T_A = −40°C to +85°C	0.0110	0.0122	0.0134	°/sec/LSB
Change Over Temperature[3]	V_{CC} = 4.75 V to 5.25 V		±3		%
Nonlinearity	Best fit straight line		0.1		°/sec
NULL					
Initial	Nominal 0°/sec output is 8192 LSB	−44		+44	°/sec
Change Over Temperature[3]	V_{CC} = 4.75 V to 5.25 V		±0.11		°/sec/°C
Turn-On Time	Power on to ±0.5°/sec of final value		10		ms
Linear Acceleration Effect	Any axis		±0.1		°/sec/*g*
Voltage Sensitivity	V_{CC} = 4.75 V to 5.25 V		±0.5		°/sec/V
NOISE PERFORMANCE					
Rate Noise Density	@ 25°C		0.04		°/sec/√Hz
FREQUENCY RESPONSE					
3 dB Bandwidth (User-Selectable)[4]	C_{OUT} = 0 µF	1		1000	Hz
Sensor Resonant Frequency			14.5		kHz
SELF-TEST RESPONSE					
Positive Self-Test[5]	See Table 5		+6226		LSB
Negative Self-Test[5]	See Table 5		−6226		LSB
TEMPERATURE SENSOR					
Reading at 298 K		7700	8192	8684	LSB
Scale Factor	Proportional to absolute temperature		0.034		K/LSB
LOGIC INPUTS					
Input High Voltage, V_{INH}		0.7 × V_{CC}			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}	Typically 10 nA	−1		+1	µA
Input Capacitance, C_{IN} (DIN)			8		pF
Input Capacitance, C_{IN} ($\overline{MSEL1}$, $\overline{MSEL2}$)			5		pF
ANALOG INPUTS	For V_{IN} < V_{CC}				
Resolution			14		Bits
Integral Nonlinearity	Best fit straight line	−6		+6	LSB
Differential Nonlinearity	No missing codes to 13 bits	−1		+6	LSB
Offset Error		−10		+10	mV
Offset Error Temperature Drift			±0.3		ppm/°C
Gain Error		−40		+40	mV
Gain Error Temperature Drift			±0.3		ppm/°C
Input Voltage Range		0		V_{CC}	V
Leakage Current			1		nA
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 500 µA	V_{CC} − 0.3			V
Output Low Voltage, V_{OL}	I_{SINK} = 500 µA			0.4	V
CONVERSION RATE					
Conversion Time				10	µs
Throughput Rate				100	kSPS

Parameter	Test Conditions/Comments	Min[1]	Typ	Max	Unit
POWER SUPPLY	All at T_A = −40°C to +85°C				
V_{CC}		4.75	5	5.25	V
V_{CC} Quiescent Supply Current	V_{CC} @ 5 V, 50 kSPS sample rate		4.3	6.5	mA
Power Dissipation	V_{CC} @ 5 V, 50 kSPS sample rate		22	33	mW
TEMPERATURE RANGE	Operation	−40		+105	°C

[1] All minimum and maximum specifications are guaranteed. Typical specifications are neither tested nor guaranteed.
[2] Dynamic range is the maximum full-scale measurement range possible, including output swing range, initial offset, sensitivity, offset drift, and sensitivity drift at 5 V supply.
[3] Defined as the output change from ambient to maximum temperature, or ambient to minimum temperature.
[4] Frequency at which the response is 3 dB down from dc response. Bandwidth = $1/(2 \times \pi \times 200\ k\Omega \times C_{OUT})$. For C_{OUT} = 0.01 µF, bandwidth = 80 Hz.
[5] Self-test response varies with temperature.

TIMING SPECIFICATIONS

T_A = 25°C, angular rate = 0°/sec, unless otherwise noted.[1]

Table 2. Read/Output Sequence

Parameter	Figure Reference	Symbol	Min	Typ	Max	Unit
Serial Clock Frequency					2.9	MHz
Throughput Rate	See Figure 2	t_{CYC}			100	kHz
$\overline{MSEL1}$ Falling to SCLK Low	See Figure 2	t_{CSD}			0	µs
$\overline{MSEL1}$ Falling to SCLK Rising	See Figure 2	t_{SUCS}	20			ns
SLCK Falling to Data Remains Valid	See Figure 2	t_{HDO}	5	16		ns
$\overline{MSEL1}$ Rising Edge to D_{OUT} High Impedance	See Figure 2	t_{DIS}		14	100	ns
SCLK Falling to Data Valid	See Figure 2	t_{EN}		16	50	ns
Acquisition Time	See Figure 2	t_{ACQ}	400			ns
D_{OUT} Fall Time	See Figure 2	t_F		11	25	ns
D_{OUT} Rise Time	See Figure 2	t_R		11	25	ns
Data Setup Time	See Figure 3	t_5	5	5		ns
SCLK Falling Edge to $\overline{MSEL2}$ Rising Edge	See Figure 3	t_7	0	0		ns
Data Hold Time	See Figure 3	t_6	4.5			ns

[1] Guaranteed by design. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.

Timing Diagrams

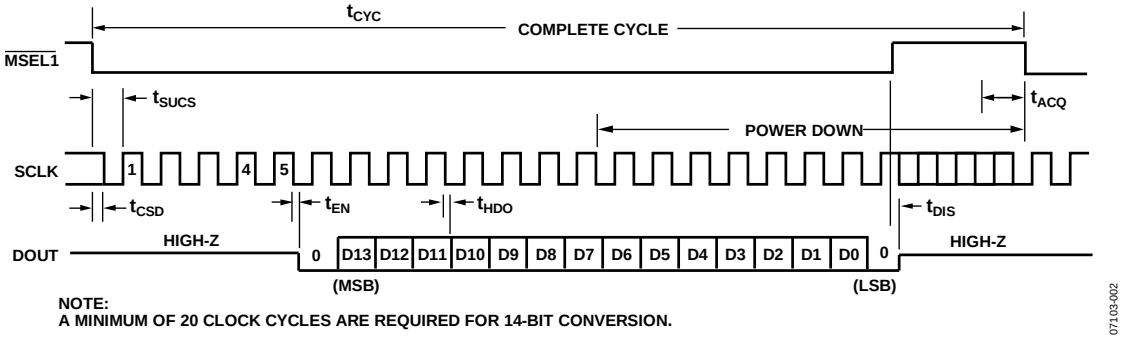


Figure 2. Serial Interface Timing Diagram—Read/Output Sequence (CPOL = 0, CPHA = 0)

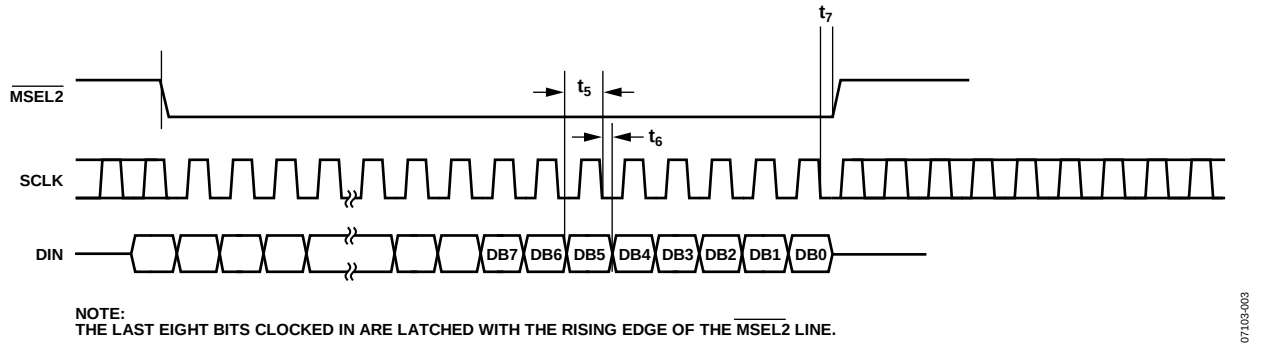


Figure 3. Serial Interface Timing—Input/Configuration Sequence (CPOL = 0, CPHA = 1)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration (Any Axis, Unpowered, 0.5 ms)	2000 *g*
Acceleration (Any Axis, Powered, 0.5 ms)	2000 *g*
V_{CC} to GND	−0.3 V to +6.0 V
V_{CC} to GND	−0.3 V to V_{CC} + 0.3 V
Analog Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7.0 V
Digital Output Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

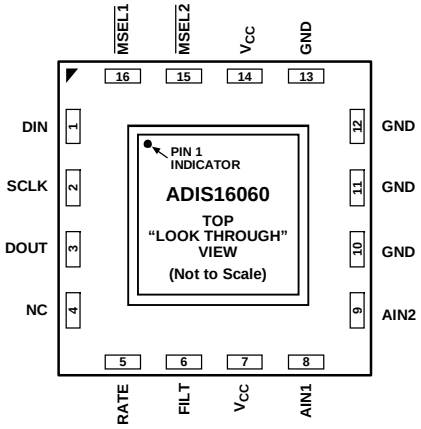
Drops onto hard surfaces can cause shocks of greater than 2000 *g* and exceed the absolute maximum rating of the device. Care should be exercised in handling the device to avoid damage.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BACAUSE NOISE COUPLING MAY RESULT.
2. THIS IS NOT AN ACTUAL "TOP VIEW," AS THE PINS ARE NOT VISIBLE FROM THE TOP. THIS IS A LAYOUT VIEW, WHICH REPRESENTS THE PIN CONFIGURATION, IF THE PACKAGE IS LOOKED THROUGH FROM THE TOP. THIS CONFIGURATION IS PROVIDED FOR PCB LAYOUT PURPOSES.

Figure 4. Pin Configuration

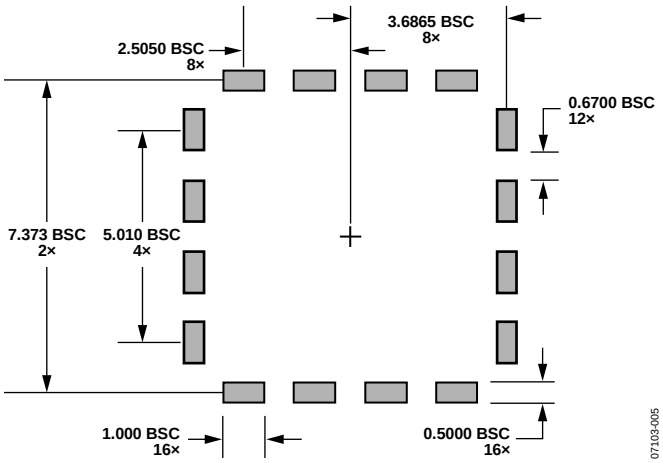


Figure 5. Second-Level Assembly Pad Layout

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	DIN	I	SPI Data Input.
2	SCLK	I	SPI Serial Clock.
3	DOUT	O	SPI Data Output.
4	NC		This pin is not connected internally (see Figure 4).
5	RATE	O	Buffered Analog Output. Represents the angular rate signal.
6	FILT	I	External Capacitor Connection to Control Bandwidth.
7	V_{CC}	S	Power Supply.
8	AIN1	I	External Analog Input Channel 1.
9	AIN2	I	External Analog Input Channel 2.
10	GND	S	Ground.
11	GND	S	Ground.
12	GND	S	Ground.
13	GND	S	Ground.
14	V_{CC}	S	Power Supply.
15	$\overline{\text{MSEL2}}$	I	SPI, Mode Select 2. User for data input functions.
16	$\overline{\text{MSEL1}}$	I	SPI, Mode Select 1. Used for data output functions.

[1] I = input; O = output; S = power supply.

TYPICAL PERFORMANCE CHARACTERISTICS

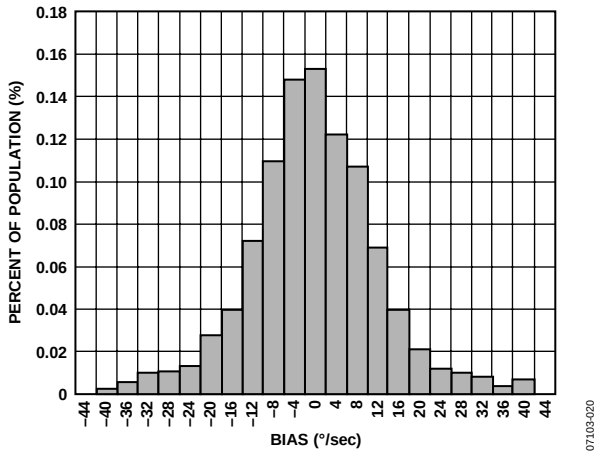


Figure 6. Initial Bias Error Distribution, 25°C, V_{CC} = 5 V

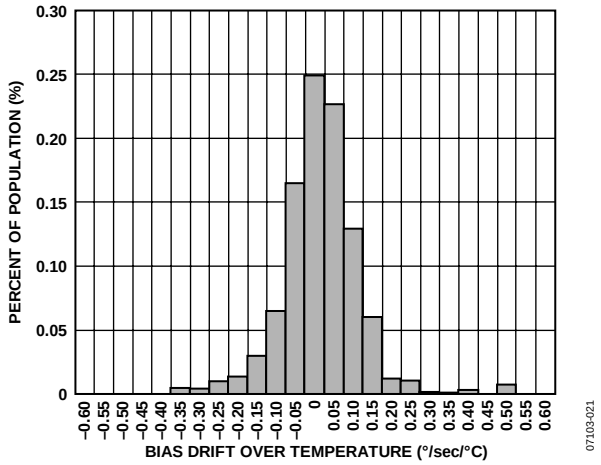


Figure 7. Bias Drift Over −40°C to +85°C, V_{CC} = 5 V

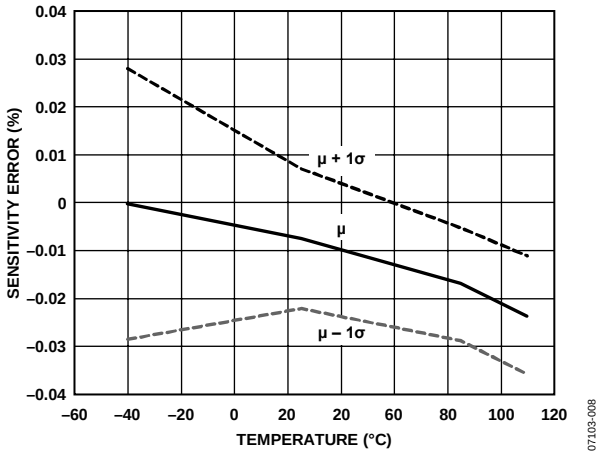


Figure 8. Sensitivity Drift vs. Temperature, V_{CC} = 5 V

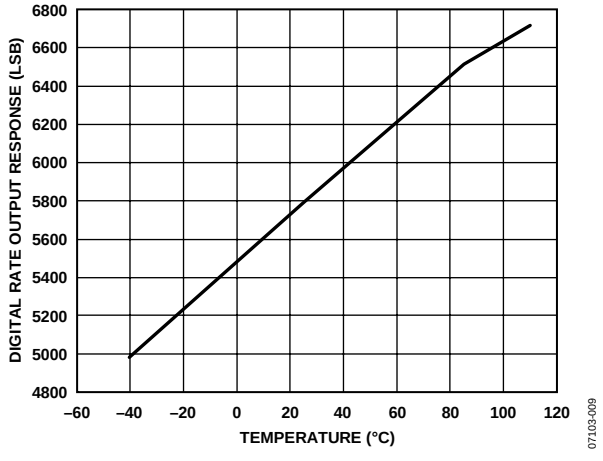


Figure 9. Positive Self-Test Response vs. Temperature, V_{CC} = 5 V

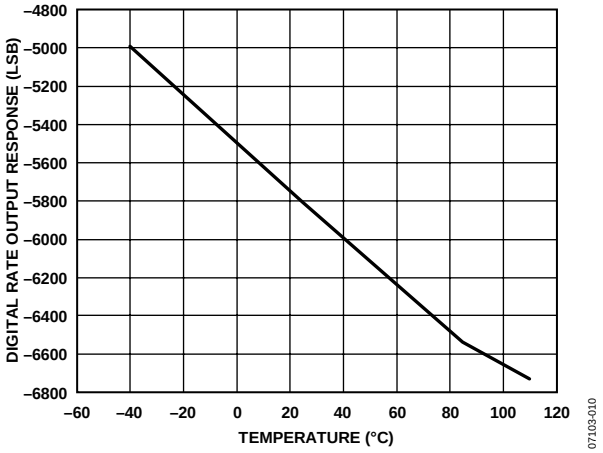


Figure 10. Negative Self-Test Output Response vs. Temperature, V_{CC} = 5 V

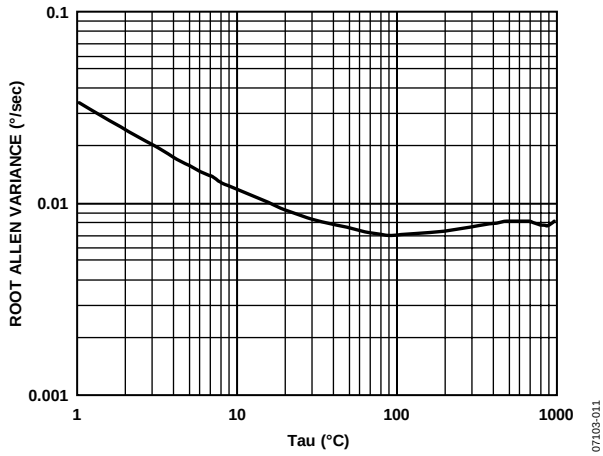


Figure 11. Allen Variance, 25°C, V_{CC} = 5 V

THEORY OF OPERATION

The ADIS16060 operates on the principle of a resonator gyroscope. Two polysilicon sensing structures each contain a dither frame that is electrostatically driven to resonance. This generates the necessary velocity element to produce a Coriolis force while rotating. At two of the outer extremes of each frame, orthogonal to the dither motion, are movable fingers that are placed between fixed pickoff fingers to form a capacitive pickoff structure that senses Coriolis motion.

The resulting signal is fed to a series of gain and demodulation stages that produce the electrical rate signal output. The rate signal is then converted to a digital representation of the output on the SPI pins. The dual-sensor design provides linear acceleration (vibration, shock) rejection. Fabricating the sensor with the signal-conditioning electronics preserves signal integrity in noisy environments.

The electrostatic resonator requires 14 V to 16 V for operation. Because only 5 V is typically available in most applications, a charge pump is included on chip. After the demodulation stage, a single-pole, low-pass filter on the chip is used to limit high frequency artifacts before final amplification. The frequency response is dominated by the second low-pass filter, which is set by adding capacitance across RATE and FILT.

ANALOG-TO-DIGITAL CONVERTER INPUT

Figure 12 shows an equivalent circuit of the input structure of the ADIS16060 auxiliary ADC.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, AINx (AIN1 and AIN2). Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 0.3 V, because exceeding this level causes these diodes to become forward-biased and to start conducting current. However, these diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions may eventually occur when the input signals exceed either VCC or GND.

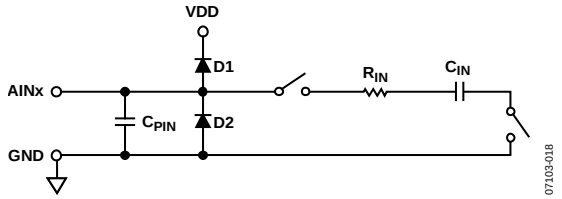


Figure 12. Equivalent Analog Input Circuit

During the acquisition phase, the impedance model for AINx is a parallel combination of the capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 600 Ω and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and mainly functions as the ADC sampling capacitor.

During the conversion phase, when the switches are open, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the ADC input can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance.

RATE SENSITIVE AXIS

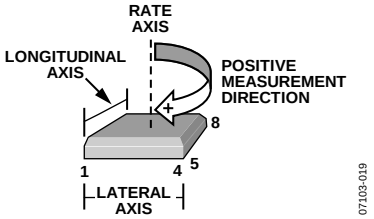


Figure 13. Rate Signal Increases with Clockwise Rotation

BASIC OPERATION

The ADIS16060 is designed for simple integration into industrial system designs, requiring only a 5 V power supply, two mode select lines, and three serial communications lines. The SPI handles all digital I/O communication in the ADIS16060.

SERIAL PERIPHERAL INTERFACE (SPI)

The ADIS16060 SPI port includes five signals: Mode Select 1 ($\overline{\text{MSEL1}}$), Mode Select 2 ($\overline{\text{MSEL2}}$), serial clock (SCLK), data input (DIN), and data output (DOUT). The $\overline{\text{MSEL1}}$ line is used when reading data out of the sensor (DOUT), and the $\overline{\text{MSEL2}}$ line is used when configuring the sensor (DIN).

Selecting Output Data

Refer to Table 5 to determine the appropriate DIN bit sequence based on the required data source. Table 2 and Table 3 provide the necessary timing details for the input configuration sequence. After the $\overline{\text{MSEL2}}$ goes high, the last eight DIN bits are loaded into the internal control register, which represents DB0 to DB7 in Table 5.

Output Data Access

Use Table 2 and Figure 2 to determine the appropriate timing considerations for reading output data.

OUTPUT DATA FORMATTING

All of the output data is in an offset-binary format, which in this case, means that the ideal output for a zero rate condition is 8192 codes. If the sensitivity is equal to +0.0122°/sec/LSB, a rate of +10°/sec results in a change of 820 codes, and a digital rate output of 9012 codes. If an offset error of −20°/sec is introduced, the output is reduced by 1639 codes (if typical sensitivity is assumed), resulting in a digital rate output of 6552 codes.

ADC CONVERSION

The internal successive approximation ADC begins the conversion process on the falling edge of $\overline{\text{MSEL1}}$ and starts to place data MSB first on the DOUT line at the 6th falling edge of SCLK, as shown in Figure 2. The entire conversion process takes 20 SCLK cycles. After $\overline{\text{MSEL1}}$ goes high, the acquisition process starts in preparation for the next conversion cycle.

Table 5. DIN Configuration Bit Assignments

Action	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Measure Angular Rate (Gyro)	0	0	1	0	0	0	0	0
Measure Temperature	0	0	0	1	0	0	0	0
Measure AIN2	1	0	0	0	0	0	0	0
Measure AIN1	0	1	0	0	0	0	0	0
Set Positive Self-Test and Output for Angular Rate	0	0	1	0	0	0	1	0
Set Negative Self-Test and Output for Angular Rate	0	0	1	0	0	0	0	1

APPLICATIONS INFORMATION

SUPPLY AND COMMON CONSIDERATIONS

Power supply noise and transient behaviors can influence the accuracy and stability of any sensor-based measurement system. Power supply stability and source impedance can influence performance. While the ADIS16060 provides 0.2 µF of capacitance on the V_{CC} pin, additional capacitors will support optimum performance.

SETTING BANDWIDTH

External Capacitor C_{OUT} is used in combination with the on-chip R_{OUT} resistor to create a low-pass filter to limit the bandwidth of the ADIS16060 rate response. The −3 dB frequency set by R_{OUT} and C_{OUT} is

$$f_{OUT} = \frac{1}{(2 \times \pi \times R_{OUT} \times C_{OUT})}$$

and can be well controlled because R_{OUT} has been trimmed during manufacturing to be 200 kΩ ± 5%. Setting the range with an external resistor impacts R_{OUT} as follows:

$$R_{OUT} = \frac{(200\ \text{k}\Omega \times R_{EXT})}{(200\ \text{k}\Omega + R_{EXT})}$$

In general, additional filter poles (analog or digital) can contribute to reducing the noise associated with the demodulation spikes (~14 kHz) in Figure 14.

INCREASING MEASUREMENT RANGE

Scaling the measurement range requires the addition of a single resistor, connected across the RATE and FILT pins. The following equation provides the proper relationship for selecting the appropriate resistor:

$$R_{EXT} = \frac{200\ \text{k}\Omega}{\Delta - 1}$$

where Δ is the increase in range.

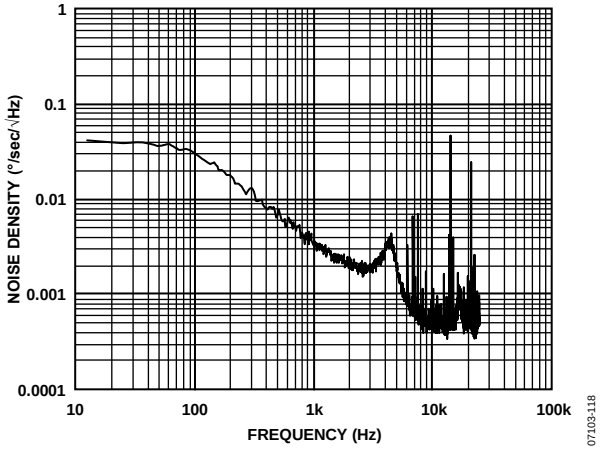


Figure 14. Spectral Noise Density, fs = 50 kHz, 80 Hz, Single-Pole Filter

DYNAMIC DIGITAL SENSITIVITY SCALING

This device supports in-system, dynamic, digital sensitivity scaling.

TEMPERATURE MEASUREMENTS

When using the temperature sensor, an acquisition time of greater than 40 µs helps to ensure proper setting and measurement accuracy. See Table 2 and Figure 2 for details on the definition of acquisition time.

SELF-TEST FUNCTION

Exercising the self-test function is simple, as shown in this example.

1. Configure using DIN = 00100010 (positive self-test, rate selected).
2. Read output.
3. Configure using DIN = 00100000 (positive self-test off, rate selected).
4. Read output.
5. Calculate the difference between Step 2 and Step 4, and compare this with the specified self-test output changes in the Specifications section.

Exercising the negative self-test requires changing the sequence in Step 1 to DIN = 00100001.

OUTLINE DIMENSIONS

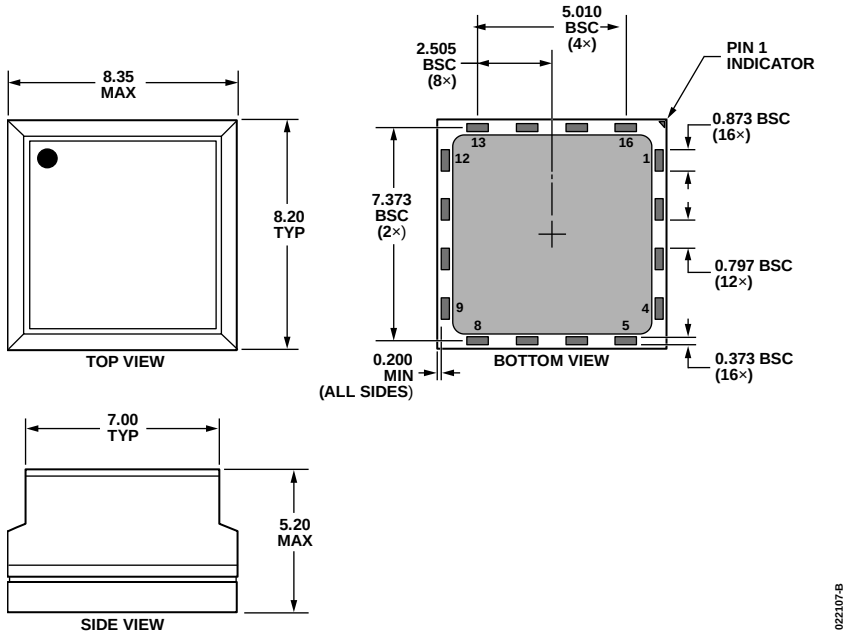


Figure 15. 16-Terminal Stacked Land Grid Array [LGA]
(CC-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16060BCCZ	−40°C to +105°C	16-Terminal Stacked Land Grid Array (LGA)	CC-16-1
ADIS16060/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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