Data Sheet | November 12, 2004 | FN9004.2

Single Supply Integrated Current Limiting Controller

The ISL6121 is a single supply Overcurrent (OC) fault protection IC for 2.5V to 5V applications where 2A current limiting is desired. This device features internal current monitoring and limiting along with a 50mΩ integrated power switch and a current limited time out to latch-off feature for system protection. The time to latch-off is independent of device temperature, and magnitude of OC.

Each ISL6121 incorporates in a 8 lead SOIC package a 50mΩ N-channel MOSFET power switch for power control. The switch is driven by a constant current source giving a controlled ramp up of the output voltage. This provides a soft start turn-on eliminating bus voltage drooping caused by in-rush current while charging heavy load capacitances. (Enable high (ISL6121H) and enable low (ISL6121L) options are) available with a fault reporting output compatible with 3V and 5V logic level signals allowing for external control and monitoring.

The Under Voltage (UVLO) lockout feature prevents turn-on of the output unless the correct ENABLE signal and VIN > 2.5V are both present. During initial turn-on the ISL6121 design prevents a fault from being presented by blanking the fault signal, unlike other vendor devices needing additional external circuitry to accomplish this. Rising and falling output is a current-limited voltage ramp so that both the inrush current and voltage slew rate are limited, independent of load. This reduces supply droop due to surge and eliminates the need for external EMI filters. During operation once an OC condition is detected the output is current limited to 2A to allow for a transient condition to pass. If still in current limit after the current limit period has elapsed the output is latched off and the fault is reported by pulling the $\overline{FAULT}$ low. The $\overline{FAULT}$ signal is latched low until reset by the enable signal being deasserted at which time the $\overline{FAULT}$ signal will clear.

See Figure 1 for typical application configuration.

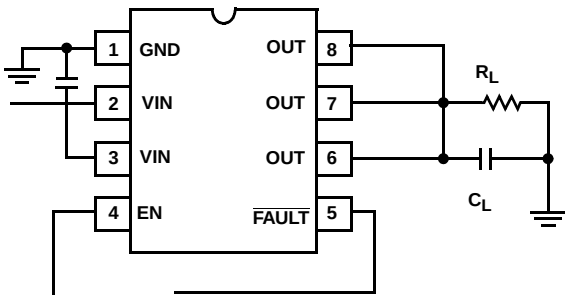


FIGURE 1. ISL6121 TYPICAL APPLICATION

Features

- 0.05Ω Integrated Power N-channel MOSFET Switch
- Accurate Current Sensing and Limiting
- 12ms Timed Fault Latch-Off, No thermal Dependency
- 2.5V to 5.5V Operating Range
- Under Voltage Lockout
- Disabled Output Internally Pulled Low
- Controlled Turn On/Off Ramp Times
- Fault Output Signal
- Logic Level Enable High Inputs (ISL6121H) or Enable Low Inputs (ISL6121L)
- Logic Level Compatible Enable Input and Fault Output
- Pb-Free Available (RoHS Compliant)

Applications

- Fibre Channel
- Industrial Power Control
- Hot Plug

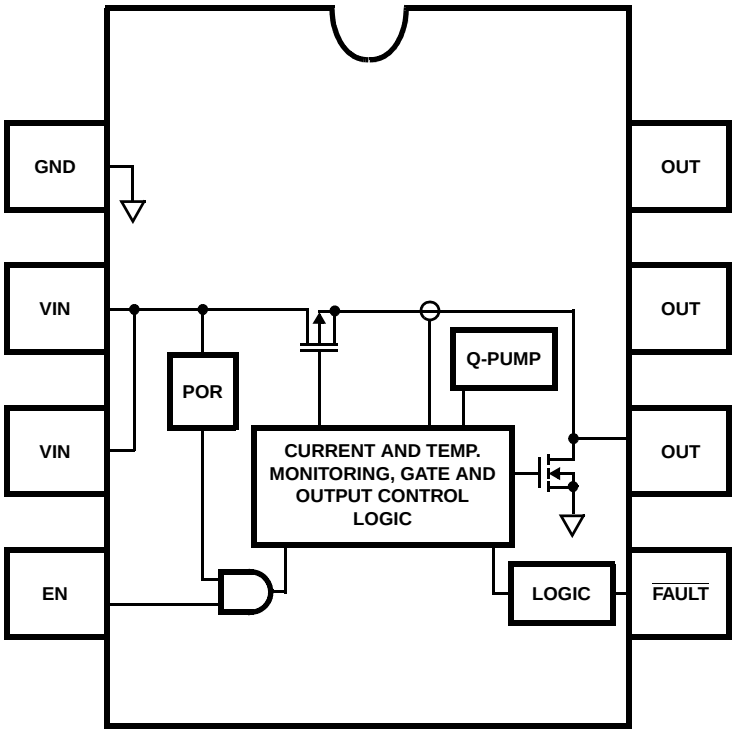
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6121HIB	-40 to 85	8 Ld SOIC	M8.15
ISL6121HIBZA (See Note)	-40 to 85	8 Ld SOIC (Pb-free)	M8.15
ISL6121HIB-T	-40 to 85	8 Ld SOIC Tape and Reel	
ISL6121HIBZA-T (See Note)	-40 to 85 (Pb-free)	8 Ld SOIC Tape and Reel	
ISL6121LIB	-40 to 85	8 Ld SOIC	M8.15
ISL6121LIBZA (See Note)	-40 to 85	8 Ld SOIC (Pb-free)	M8.15
ISL6121LIB-T	-40 to 85	8 Ld SOIC Tape and Reel	
ISL6121LIBZA-T (See Note)	-40 to 85	8 Ld SOIC Tape and Reel (Pb-free)	
ISL6121HEVAL1	Evaluation Platform		

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 321-724-7143 | Intersil and Design is a trademark of Intersil Americas Inc.
Copyright © Intersil Americas Inc. 2001, All Rights Reserved

Simplified Block Diagram



Pin Descriptions

PIN #	SYMBOL	FUNCTION	DESCRIPTION
1	GND	IC GND Reference	
2, 3	VIN	Chip Bias, Controlled Supply Input, Undervoltage Lock-Out	VIN provides chip bias voltage. At VIN < 2.5V chip functionality is disabled, $\overline{\text{FAULT}}$ latch is cleared and floating. OUT is pulled and held low.
4	ENABLE / $\overline{\text{ENABLE}}$	Enable / Enable Not Input	Enables chip when VIN and ENABLE > 2.5V or $\overline{\text{ENABLE}}$ < 0.6V
5	FAULT	Over Current Fault Indicator	Overcurrent fault indicator. $\overline{\text{FAULT}}$ is disabled for 12ms after turn-on. This output is pulled low to GND after the current limit time-out period has expired and stays latched until ENABLE is deasserted.
6, 7, 8	VOUT	Controlled Supply Output	Voltage output, connect to load to protect. Upon an overcurrent condition VOUT is current limited to 2A. Current limit response time is within 200µS. This output will remain in current limit for approximately 12ms before being latched off.

Absolute Maximum Ratings

Supply Voltage (V+ to V-) 6.0V
EN, FAULT . . . . . -0.3V to 6V
OUT . . . . . GND-0.3V to VIN +0.3V
DC Input Voltage . . . . . V_{SUPPLY}
Output Current . . . . . Short Circuit Protected
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3KV

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage Range (Typical) . . . . . 2.5V to 5.5V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
8 Lead SOIC	116

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

V_{SUPPLY} = 5V, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SWITCH						
ISL6121 On Resistance at 2.7V	$r_{DS(ON)_27}$	VIN = 2.7V, IOUT = 0.8A, $T_A = T_J = 25^oC$	-	60	70	mΩ
		$T_A = T_J = 85^oC$	-	-	80	mΩ
ISL6121 On Resistance at 3.3V	$r_{DS(ON)_33}$	VIN = 3.3V, IOUT = 0.8A, $T_A = T_J = 25^oC$	-	50	60	mΩ
		$T_A = T_J = 85^oC$	-	-	75	mΩ
ISL6121 On Resistance at 5.0V	$r_{DS(ON)_50}$	VIN = 5V, IOUT = 0.8A, $T_A = T_J = 25^oC$	-	50	60	mΩ
		$T_A = T_J = 85^oC$	-	-	75	mΩ
Disabled Output Voltage	V_{OUT_DIS}	VIN = 5V, Switch Disabled, 50µA Load	-	300	450	mV
Output Voltage Rising Rate	t_vout_rt	R_L = 10Ω, C_L = 0.1µF, 10%-90%	-	10	-	V/ms
Slow VOUT Turn-off Rate	t_svout_offt	R_L = 10Ω, C_L = 0.1µF, 90%-10%	-	10	-	V/ms
Fast VOUT Turn-off Rate	t_fvout_offt	R_L = 1Ω, C_L = 0.1µF, 90%-10%	-	3	-	V/µs
CURRENT CONTROL						
Current Limit, VIN = 5V	Ilim	VOUT = 3.3V	1.5	2	2.5	A
OC Regulation Settling Time	$tsett_{Ilim}$	R_L = 1.6Ω, C_L = 0.1µF to Within 10% of CR	-	1	-	ms
Severe OC Regulation Settling Time	$tsett_{Ilim_sev}$	R_L< 1Ω, C_L = 0.1µF to Within 10% of CR	-	100	-	µs
Over Current Latch-off Time	t_{OC_loff}	$T_J = 25^oC$	-	12	-	ms
I/O PARAMETERS						
Fault Output Voltage	Vfault	Fault Output Current = 10mA	-	-	0.4	V
ENABLE High Threshold	Ven_vih	VIN = 5.5V	2.0	-	-	V
ENABLE Low Threshold	Ven_vil	VIN = 2.7V	-	-	0.6	V
ENABLE Low Threshold	Ven_vil	VIN = 4.5V	-	-	0.8	V
ENABLE Input Current	Ien_i	ENABLE = 0V to 5V, VIN = 5V, $T_J > 25^oC$	-0.5	0	0.5	µA
BIAS PARAMETERS						
Enabled VIN Current	I_{VDD}	Switch Closed, OUTPUT = OPEN, $T_J > 0^oC$	-	120	200	µA
Disabled VIN Current	I_{VDD}	Switch Open, OUTPUT = OPEN	-	-	5	µA
Under Voltage Lockout Threshold	V_{UVLH}	VIN Rising, Switch Enabled	1.7	2.25	2.5	V
UV Hysteresis	UV_{HYS}		50	100	-	mV
Over Temperature Disable	Temp_dis		-	150	-	^oC

Introduction

The ISL6121 is a single channel Overcurrent (OC) fault protection IC for the +2.5V to +5V environment. Each ISL6121 incorporates in a single 8 lead SOIC package a 50mΩ N channel MOSFET power switch for power control. See Figure 3 for switch resistance curves. With an enabling input and fault reporting output compatible with 3V and 5V logic allowing for external control and monitoring. See Figure 2 for IC operational waveforms. This device features internal current monitoring, consistent current limiting and an integrated power switch with a current limiting timed delay to latch-off feature for system protection.

Key Feature Description and Operation

UV Lock Out

The ISL6121 undervoltage lockout feature prevents functionality of the device unless the correct ENABLE state and VIN > 2.5V are present.

Soft Start

A constant 500nA current source ramps up the switch's gate causing a voltage follower effect on the output voltage. This provides a soft start turn-on and eliminates bus voltage drooping caused by inrush current charging heavy load capacitances. The rising and falling output is a current limited voltage ramp so that both the inrush current and voltage slew rate are limited, independent of load. This reduces supply droop due to surge and also eliminates the need for external EMI filters necessary on other IC products. See Figure 4 for turn-on wave forms.

Fault Blanking On Start-Up

During initial turn-on the ISL6121 prevents nuisance faults being reported to the system controller by blanking the fault signal for 12ms. This blanking eliminates the need for external RC filters necessary for other vendor products that assert a fault signal upon initial turn-on into a temporary high current condition. See Figures 11 through 13 for waveform examples.

Current Regulation

The ISL6121 has integrated current sensing on the power MOSFET that allows for rapid control of OC events. Once an OC is detected the ISL6121 goes into its Current Regulation (CR) control mode. The ISL6121 CR level is set to a nominal 2A. This current regulation is ±20% over the full operating temperature and voltage bias range. See Figures 5 and 6 for illustrative curves.

The speed of this control is proportional to the magnitude of the OC fault. Thus a hard over current is more quickly controlled than a marginal condition. See Figure 7 for waveforms illustrating this and Figure 8 for an accompanying graph.

Latch-Off Time Delay

The primary function of any OC protection device is to quickly isolate the voltage bus from a faulty load. Unlike many other manufacturers' IC products that sense the IC thermal condition (the monitored IC junction temperature depends on a number of factors the most important of which are power dissipation of the faulted switch and the package temp) to isolate a faulty load, the ISL6121 uses an internal 12ms timer that starts upon OC detection. Once an OC condition is detected the output is current limited for a nominal 12ms to allow transient conditions to pass before latch-off. The time to latch-off is independent of the device's thermal condition.

If, after the ISL6121 has latched off, and the fault has asserted and the enable is not deasserted but the OC condition still exists, the ISL6121 unlike other IC devices does not send to the controller a continuous string of fault pulses. The ISL6121's single fault signal is sent at the time of latch off.

Slow And Fast Shutdown

The ISL6121 has two shutdown modes. When disabled with a Load Current less than the CR level the ISL6121 shuts down in a controlled manner using a 500nA constant current source controlled ramp. When latched-off during CR or if the timer has expired the ISL6121 quickly pulls down the output thereby quickly removing the faulted load from the voltage bus. See Figures 9 and 10 for waveforms of each mode.

Temperature Shutdown

Although the ISL6121 has a thermal shutdown feature, because of the 12ms timed shutdown this will only be invoked in extremely high ambient temperatures.

Active Output Pulldown

Another unique ISL6121 feature is the active pull down on the outputs to within 300mV of GND when the device is disabled.

Typical Performance Curves

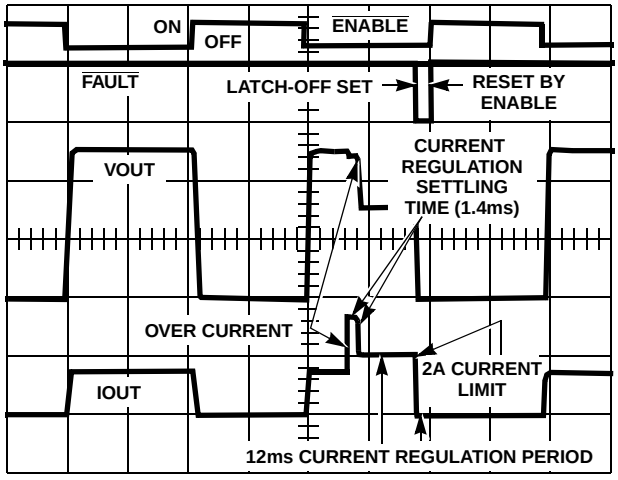


FIGURE 2. OPERATIONAL WAVEFORMS

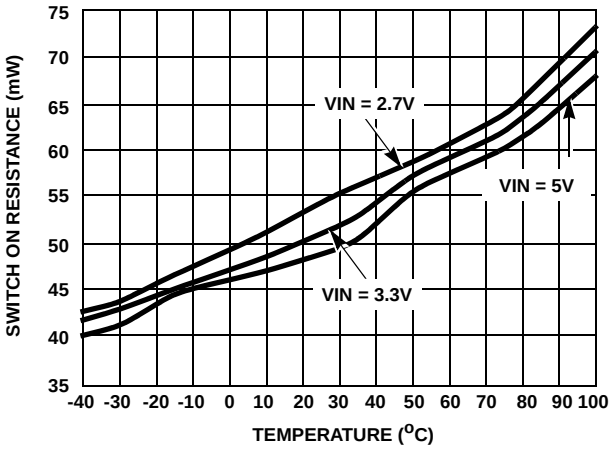


FIGURE 3. SWITCH RESISTANCE AT 1A

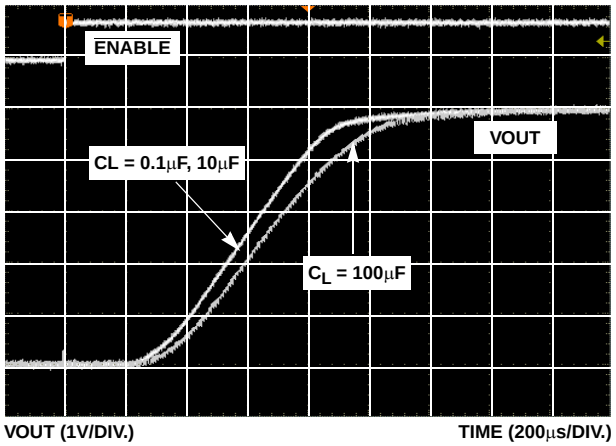


FIGURE 4. VOUT SOFT START vs CLOAD

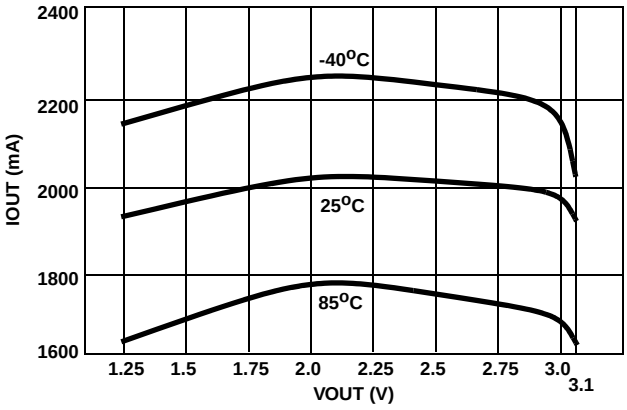


FIGURE 5. CURRENT REGULATION vs VOUT (VIN = 3.3V)

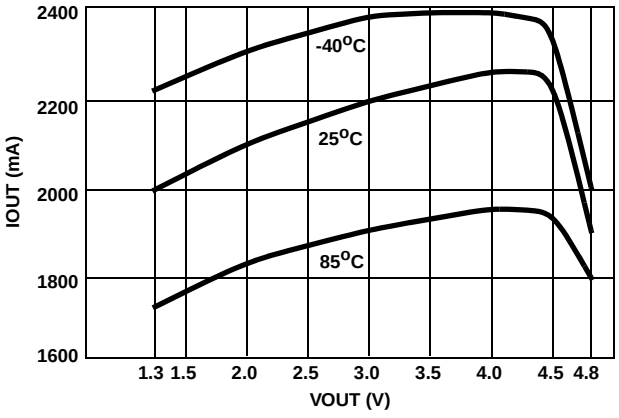


FIGURE 6. CURRENT REGULATION vs VOUT (VIN = 5.0V)

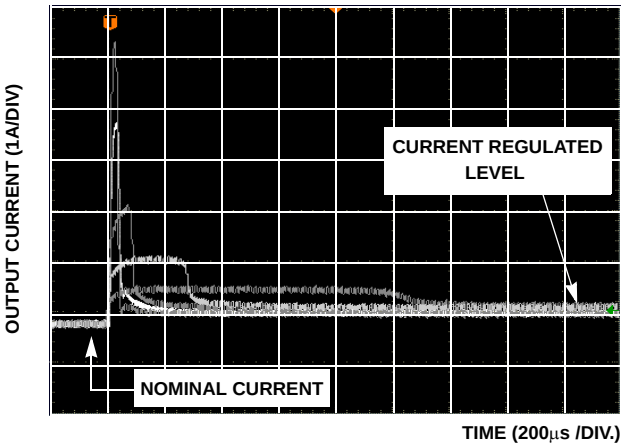


FIGURE 7. OC TO CR SETTLING TIME WAVEFORMS

Typical Performance Curves (Continued)

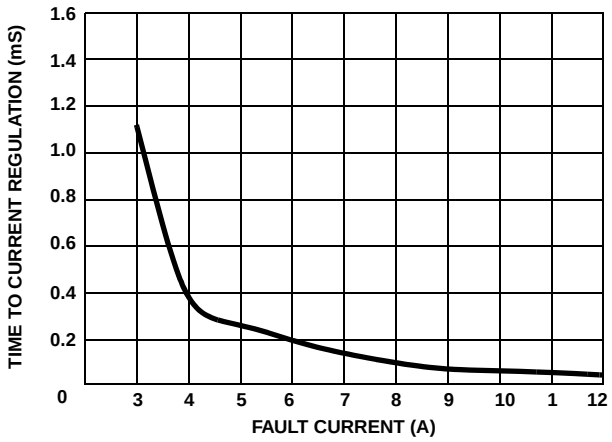


FIGURE 8. CR SETTLING TIME vs FAULT CURRENT

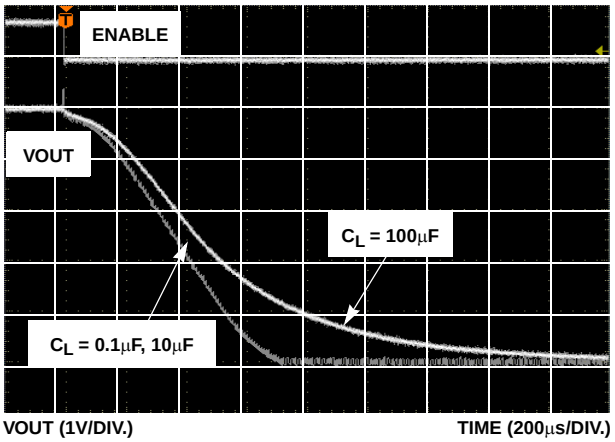


FIGURE 9. SLOW TURN-OFF vs C_{LOAD}

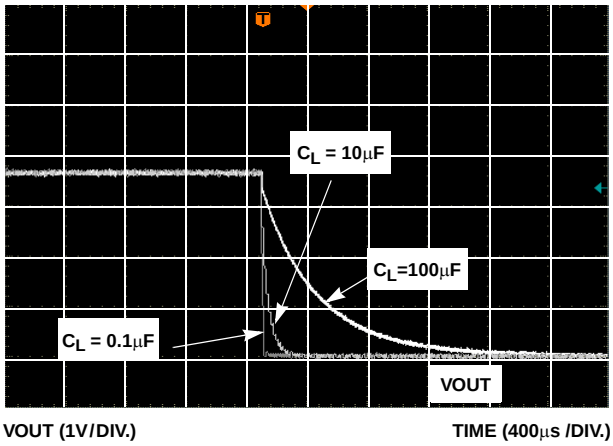


FIGURE 10. FAST TURN-OFF vs C_{LOAD}

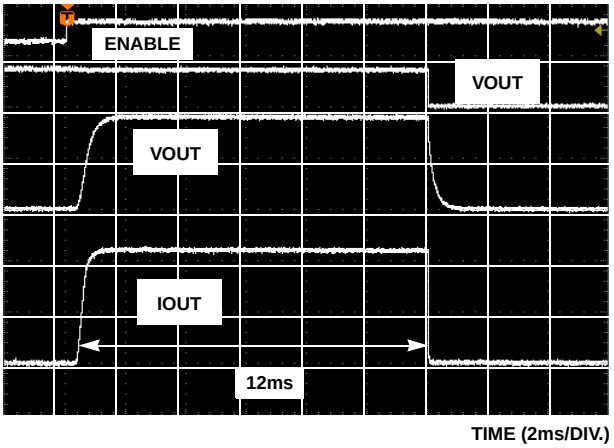


FIGURE 11. ISL6121 TURN-ON INTO 3A OC

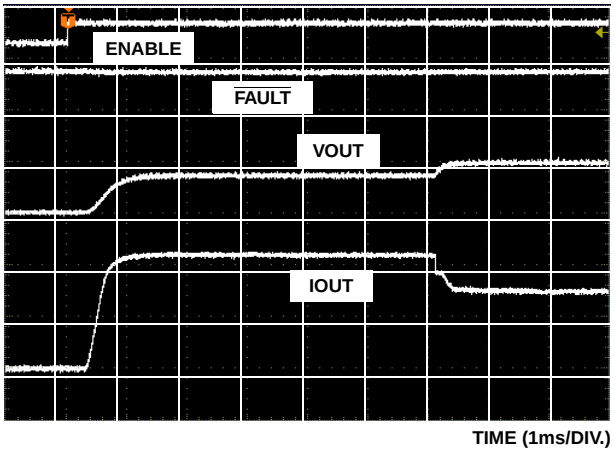


FIGURE 12. ISL6121 TURN-ON INTO A 6ms MOMENTARY OC

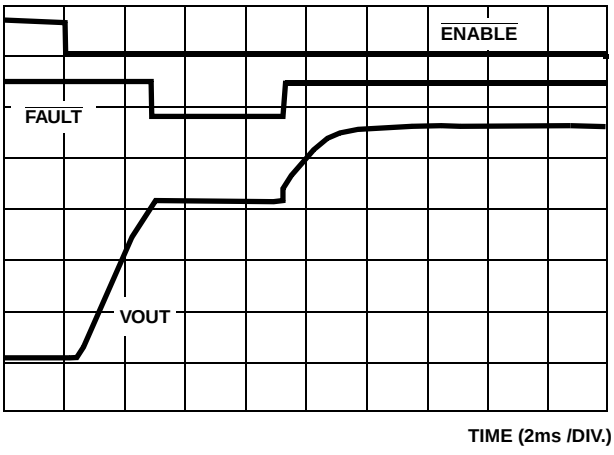


FIGURE 13. VENDOR TURN-ON INTO A 6ms MOMENTARY OC

Using the ISL6121EVAL1 Platform

General and Biasing Information

The ISL6121EVAL1 platform, Figure 17, allows evaluation of the ISL6121 power supply control IC and comparison against a suitably sized (1.85A hold current rating) PPTC component. The evaluation platform is biased and monitored through numerous test points (TP#). See Table 1 for test point assignments and descriptions.

TABLE 1. ISL6121EVAL1 TEST POINT ASSIGNMENTS

TP #	DESCRIPTION
TP1	Eval Board and IC GND
TP2	Eval Board +5V Bias
TP4	Enable
TP5	Fault
TP6	VOUT
TP9	IC VIN Pin
TP10	PPTC Load Side
TP11	Invoke Over Current

Upon proper bias the PPTC, F1, has a nominal 1.5A load current passing through it which is the below the hold current rating for that particular device. Removal of the PPTC is necessary to isolate the ISL6121 as the PPTC load current is common to the ISL6121EVAL1 bias connections.

By enabling the ISL6121H switches by signaling TP4 high (> 2.4V) the IC is also loaded with a nominal 1.5A current.

Provided test points enable the evaluation of voltage loss across the PPTC (TP9 - TP10) and likewise across the ISL6121 enabled switch (TP9 - TP6). Expect to see 10% - 30% greater voltage loss across the PPTC than the ISL6121.

An Overcurrent (OC) condition can be invoked on both the ISL6121 and the PPTC by driving TP11 to +6V, causing SW1 to close and a nominal 3A load is imposed on each. This represents a current overload to the ISL6121 and is thus quickly current regulated to the 2A limit. If the OC duration extends beyond the nominal 12ms of the internal ISL6121 timer then the output is latched off and the fault output is asserted by being pulled low, turning on the FAULT_ LED.

The primary function of any OC protection device is to quickly isolate the voltage bus from a faulty load. Unlike the PPTC and some other vendor available IC products, the ISL6121 internal timer that starts upon OC detection provides consistent protection that is independent of temperature. Figures 14 through 16 illustrate the comparative efficiency and effectiveness of the ISL6121 vs the PPTC in protecting and isolating a faulty load capable from drooping the system bus in that system.

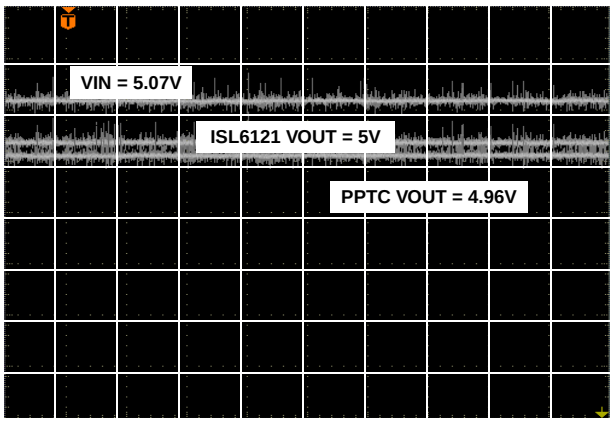


FIGURE 14. ISL6121 vs PPTC INTO 3.3Ω LOAD

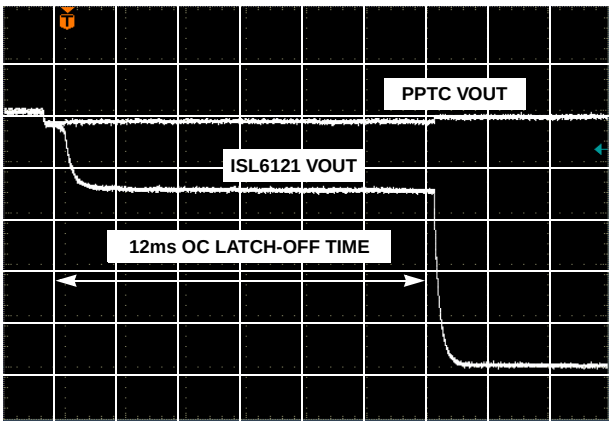


FIGURE 15. ISL6121 vs PPTC INTO 1.6Ω LOAD

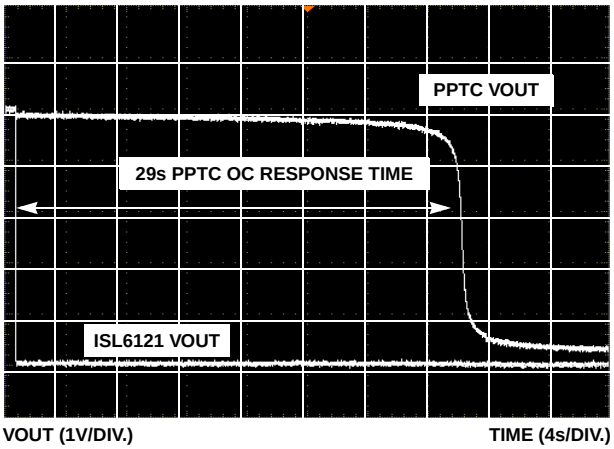


FIGURE 16. ISL6121 vs PPTC WITH EXTENDED 1.6Ω LOAD

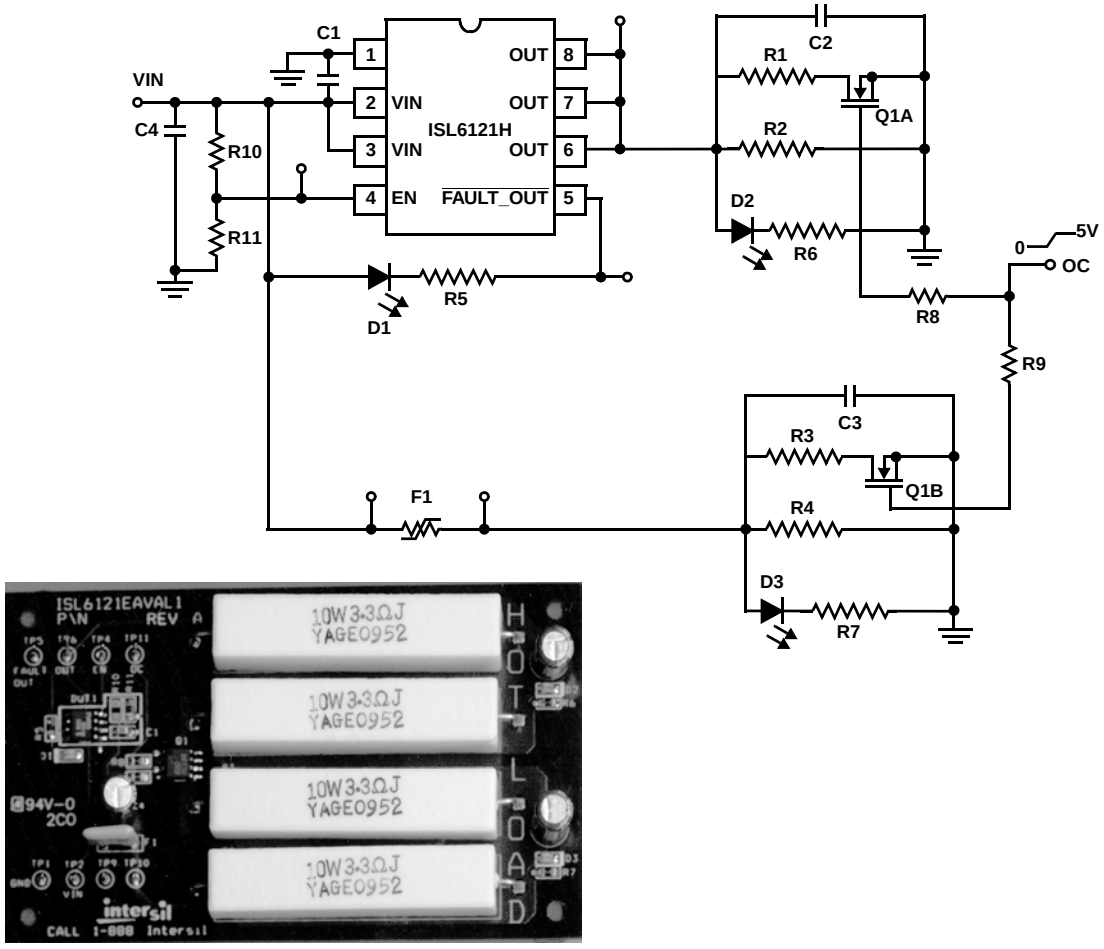


FIGURE 17. ISL6121EVAL1 SCHEMATIC AND PHOTOGRAPH

TABLE 2. ISL6121EVAL1 BOARD COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
DUT1	ISL6121H	Intersil, ISL6121H, Integrated FET Hot Plug Controller
R1 - R4	Load Resistors	YAGEO, 3.3Ω 5%, 10W, 3.3W-10-ND
R5-R7	LED Current Limiting Resistor	470Ω, 0805
C1	Chip Decoupling Capacitor	0.1μF, 0805
C2 - C3	Load Capacitor	100μF 16V Electrolytic, Radial Lead
D1 - D3	Indicating LEDs	0805, SMD LEDs Red
F1	1.85A Hold Current Poly-Fuse	Raychem, RUSB185 or Equivalent
C4	Bulk Filter Capacitor	100μF 16V Electrolytic, Radial Lead
Q1	Over Current Switch	Intersil, ITF86110DK8T, 7.5A, 30V, 0.025Ω Dual N-Channel MOSFETs
R8 - R9	Gate Series Resistors	47Ω, 0805
R10 - R11	Enable Pullup/Pulldown Resistors	1.2KΩ, 0805, R10 Not Populated

Implementing Autoreset on the ISL6121 Hot Swap Controller.

Abstract

In applications where the cost, complexity or requirement for a system controller is avoided and an autonomous power control function is desired, a device that can monitor and protect against excessive current failures is needed. This tech brief shows how to implement such an autonomous controller using the ISL6121HIB. This application works only with the ‘H’ version of this device. The ‘H’ version refers to the enable function being asserted upon a high input.

Introduction

The ISL6118, ISL6119 and ISL6121 are all 2.5V to 5V power supply controllers, each having a different level of current regulation (CR). The ISL6118 and ISL6119 have 2 independent controllers with CR levels of 0.6A and 1.0A respectively whereas the ISL6121 is a single supply controller with a 2A CR level. Each of these devices features integrated power switch(es) for power control. Each switch is driven by a constant current source giving a controlled ramp up of the output voltage. This provides a soft start turn-on eliminating bus voltage drooping caused by in-rush current while charging heavy load capacitances. The independent enabling inputs and fault reporting outputs for each channel are available and necessary for the autonomous autoreset application.

The undervoltage (UV) feature prevents turn-on of the outputs unless the ENABLE pin and VIN are > 2.5V. During initial turn-on the ISL6121 prevents fault reporting by blanking the fault signal. Rising and falling outputs are current-limited voltage ramps so that both the inrush current and voltage slew rate are limited, independent of load. This reduces supply droop due to surge and eliminates the need for external EMI filters. During operation, once an OC condition is detected the appropriate output is current limited to the appropriate level for 10ms to allow transient conditions to pass. If still in current limit after the current limit period has elapsed, the output is latched off and the fault is reported by pulling the corresponding $\overline{\text{FAULT}}$ low. The $\overline{\text{FAULT}}$ signal is latched low until reset by the ENABLE signal being de-asserted at which time the $\overline{\text{FAULT}}$ signal will clear.

It is this described sequence of events that allows for the autoreset function to be implemented in a cost efficient manner requiring the addition of only an RC network per channel to the typical application.

Figure 18 illustrates the RC network needed with suggested component values and the configuration of the relevant pins for each autoreset channel.

Description of Operation

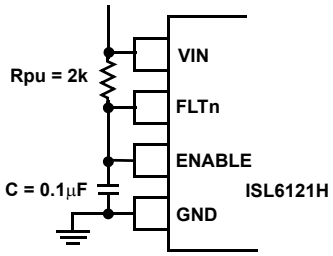


FIGURE 18.

Initially as voltage is applied to VIN, the pull up resistor (Rpu) provides for pull up to VIN on both the ENABLE pin asserting the output once VIN > 2.5V and on the FLTn pin. Once turned on and an overcurrent (OC) condition occurs the IC provides CR protection for 10ms and then the FLTn pin pulls low through Rpu and also pulling the ENABLE low thus resetting the device fault condition. At this time the Rpu charges the cap and the voltage on the ENABLE / FLTn node rises until the ENABLE > 2.0 and the output is asserted on once again. This automatic reset cycle will continue until the OC fault no longer exists on the output. After several seconds in this mode of operation the IC thermal protection invokes adjusting the timing of the on-off cycle to prevent excessive thermal dissipation in the power switch protecting itself and surrounding circuitry. See Figure 19 for operation waveform.

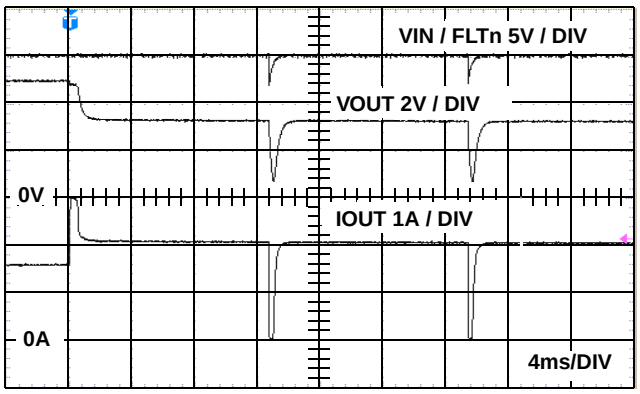
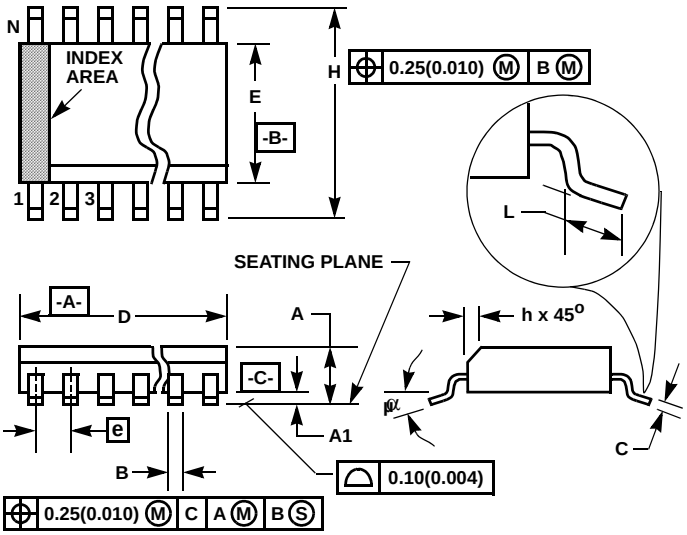


FIGURE 19. AUTO RESET OPERATION

Applications

- USB
- 2.5V to 5V up to 10W power port protection

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation’s quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com