Very Fast Infrared Transceiver Module (VFIR, 16 Mbit/s) IrDA® Serial Interface Compatible 2.7 V to 5.5 V Supply Voltage Range

Description

The TFDU8108 transceiver is part of a family of low power consumption infrared transceiver modules. It is compliant to the IrDA physical layer standard for VFIR infrared data communication, supporting IrDA speeds up to 16 Mbit/s (VFIR) and carrier based remote control modes up to 2 MHz. Integrated within the transceiver module are a PIN photodiode, an infrared emitter (IRED), and a low-power control IC.

At a minimum, a Vcc bypass capacitor is the only external component required implementing a complete solution. For limiting the transceiver's internal power dissipation one additional resistor might be necessary. The transceiver can be operated with logic I/O voltages as low as 1.8 V.



Features

- Compliant to the latest IrDA physical layer standard (up to 16 Mbit/s), HP-SIR®, Sharp ASK® and TV Remote Control
- Compliant to the IrDA "Serial Interface Specification for Transceivers"
- Surface mount Soldering to side and top view orientation
- Surface Mount package 9.7 x 4.7 x 4.0 mm^3 for side view and top view applications
- Operating supply voltage from 2.7 V to 5.5 V
- Compliant to all logic levels between 1.8 V and 5 V
- TV Remote Control support
- Low Power consumption (2 mA idle supply current)
- Power Shutdown mode (1 µA shutdown current)
- Tri-State-receiver output, weak pull-up when in output is disabled
- Built - In EMI Protection - No external shielding necessary
- Pin to Pin compatible to legacy Vishay SIR and FIR infrared transceivers
- Eye safety class 1 (IEC60825-1, ed. 2001), limited LED on-time, LED current is controlled, no single fault to be considered
- Lead (Pb)-free device
- Qualified for lead (Pb)-free and Sn/Pb processing (MSL4)
- Device in accordance with RoHS 2002/95/EC and WEEE 2002/96/EC
- Split power supply, can be driven by a separate power supply not loading the regulated supply. U.S. Pat. No. 6,157,476

Applications

- Notebook Computers, Desktop PCs, Palmtop computers (Win CE, Palm PC), PDAs
- Digital still and video cameras
- Printers, fax machines, photocopiers, screen projectors
- MP3 players
- Telecommunication products (Cellular Phones, Pagers)
- Internet TV boxes, Video Conferencing Systems
- External infrared adapters (dongles)
- Medical and industrial data collection devices

Package



TFDU8108
Baby Face
(Universal)
weight 200 mg

19497

Ordering Information

Part Number	Description	Qty / Reel
TFDU8108-TR3	Oriented in carrier tape for side view surface mounting	1000 pcs
TFDU8108-TT3	Oriented in carrier tape for top view surface mounting	1000 pcs
TFDU8108	In tube	50 pcs

Functional Block Diagram

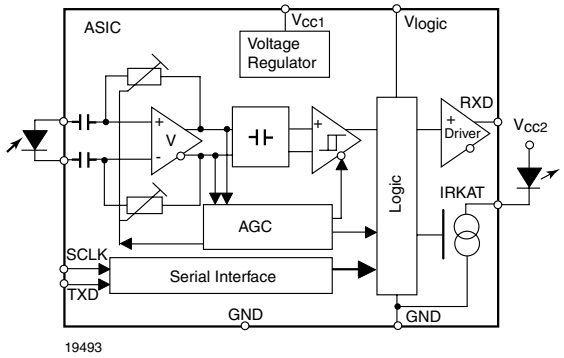


Figure 1. Functional Block Diagram

V_{CC1}: Analog supply voltage
V_{logic}: Digital supply voltage, I/O reference voltage
V_{CC2}: Independent supply voltage for the LED driver

Serial Interface according the IrDA standard "Serial Interface for Transceiver Control"
SCLK: Clock line as timing reference*)
TXD: TX/SWDAT - line*)
RXD: RX/SRDAT - line*)

*) see Appendix A for definitions

Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:

- SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0
- MIR: 576 kbit/s to 1152 kbit/s
- FIR: 4 Mbit/s
- VFIR: 16 Mbit/s

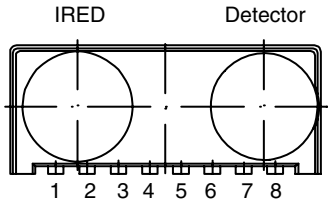
MIR and FIR were implement with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any case obsoletes the former version.

Pin Description

Pin Number	Function	Description	I/O	Active
1	IRED Anode	IRED anode to be externally connected to V_{CC2} This pin is allowed to be supplied from an uncontrolled power supply seperated from the controlled V_{CC1} - supply.		
2	IRED Cathode	IRED Cathode, internally connected to driver transistor		
3	TXD	Transmit Data Input, dynamically loaded	I	HIGH
4	RXD	Received Data Output, Tri-State CMOS driver output capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. Pin is current limited for protection against programming errors. The output is loaded with a weak 500 kΩ pull-up, when in SD mode. The RXD echoes the optical TXD signal duration transmission.	O	LOW
5	SCLK	Serial Clock, dynamically loaded	I	HIGH
6	V_{CC}	Supply Voltage		
7	V_{logic}	Supply voltage for digital part, 1.8 V to 5.5 V, defines logic swing for TXD, SCLK, and RXD		
8	GND	Ground		

BabyFace (Universal)

"U" Option BabyFace (Universal)



17087

Figure 2. Pinning

Absolute Maximum Ratings

Reference point Ground (pin 8) unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage range, transceiver	0 V < V_{CC2} < 6 V	V_{CC1}	- 0.5		6	V
Supply voltage range, transmitter	0 V < V_{CC1} < 6 V	V_{CC2}	- 0.5		6	V
Supply voltage range, transceiver logic	0 V < V_{CC1} < 6 V	V_{logic}	- 0.5		6	V
IRED anode voltage		V_{IREDA}	- 0.5		6	V
Transmitter data input voltage		V_{TXD}	- 0.5		V_{logic} + 0.5	V
Receiver data output voltage		V_{RXD}	- 0.5		V_{logic} + 0.5	V
Input currents	For all pins, except IRED anode pin				10	mA
Output sinking current					25	mA
Power dissipation	See derating curve, figure 7	P_D			350	mW
Junction temperature		T_J			125	°C
Ambient temperature range (operating)		T_{amb}	0		+ 85	°C
Storage temperature range		T_{stg}	- 40		+ 100	°C
Soldering temperature	See recommended solder profile (see figures 4 to 6)				260	°C
Average output current		I_{IRED} (DC)			130	mA
Repetitive pulse output current	< 90 µs, t_{on} < 20 %	I_{IRED} (RP)			600	mA
Virtual source size	Method: (1 - 1/e) encircled energy	d	2.5	2.8		mm
Maximum Intensity for Class 1 Operation of IEC825-1 or EN60825-1, edition Jan. 2001 IrDA® specified maximum limit					Internal limitation to class 1 500	 mW/sr

Due to the internal limitation measures the device is a "class1" device. It will not exceed the IrDA® intensity limit of 500 mW/sr.

Electrical Characteristics

Transceiver

T_{amb} = 25 °C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply voltage V_{CC1}		V_{CC1}	2.7		5.5	V
Supply voltage V_{logic}		V_{logic}	1.8		5.5	V
Dynamic supply current	Receive mode only. In transmit mode, add the averaged programmed current of IRED current as I_{CC2}					
Dynamic supply current	Active, SIR, E_e = 0 klx (idle) T = - 25 °C to 85 °C	I_{CC1}		0.8	2.5	mA
Dynamic supply current	Active, VFIR, E_e = 0 klx, (idle) T = - 25 °C to 85 °C	I_{CC1}			10	mA
Dynamic supply current	active, no load E_e = 0 klx, (idle) T = - 25 °C to 85 °C	I_{logic}			5	µA
Dynamic supply current	E_e = 1 klx*) receive mode, E_{Eo} = 100 mW/m^2 (9.6 kbit/s to 4.0 Mbit/s), R_L = 10 kΩ to V_{logic} = 5 V, C_L = 15 pF T = - 25 °C to 85 °C	I_{logic}			1	mA
Standby supply current	Inactive, set to shutdown mode T = 25 °C, E_e = 0 klx T = 25 °C, E_e = 1 klx*) **)	I_{SD}			 2 2	 µA µA
Standby supply current	Shutdown mode, **) T = 85 °C	I_{SD}			5	µA
Operating temperature range		T_A	0		+ 85	°C
Output voltage low	C_{load} = 15 pF, V_{logic} = 3 V, I_{OLO} < + 500 µA	V_{OLO}			0.4	V
Output voltage high	C_{load} = 15 pF, V_{logic} = 5 V, I_{OHI} < - 250 µA	V_{OHI}	0.8 x V_{logic}			V
Input voltage high (TXD, SCLK)		V_{IL}	- 0.5		0.5	
Input voltage high (TXD, SCLK)		V_{IH}	V_{logic} - 0.3		6	V
logic decision level (TXD, SCLK) ***)		V_{IL}		0.5 x V_{logic}		V
Input leakage current (TXD, SCLK)		I_L	- 10		+ 10	µA
Input capacitance		C_I			5	pF

*) Standard illuminant A.

**) In shutdown condition the device is not ambient light sensitive.

***) The device will work with less tight levels than specified min/max values of the logic input voltage. It is recommended to use the specified min/max values to minimize operating/standby supply currents.

Optoelectronic Characteristics

Receiver

T_{amb} = 25 °C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Minimum detection threshold irradiance	9.6 kbit/s to 115.2 kbit/s, SIR λ = 850 nm to 900 nm	E_e		25	40	mW/m^2
Minimum detection threshold irradiance	1.152 Mbit/s, MIR λ = 850 nm to 900 nm	E_e		65	90	mW/m^2
Minimum detection threshold irradiance	4 Mbit/s, FIR λ = 850 nm to 900 nm	E_e		85	90	mW/m^2
Minimum detection threshold irradiance	16 Mbit/s, VFIR λ = 850 nm to 900 nm	E_e		160	200	mW/m^2
Maximum detection threshold irradiance	λ = 850 nm to 900 nm	E_e	5	10		kW/m^2
Logic LOW receiver input irradiance		E_e	4			mW/m^2
RXD pulse width of output signal, 50 % SIR mode	Input pulse length 20 µs, 9.6 kbit/s	t_{PW}	1.3		2.6	µs
RXD pulse width of output signal, 50 % SIR mode	Input pulse length 1.41 µs, 115.2 kbit/s	t_{PW}	1.3		2.6	µs
RXD pulse width of output signal, 50 % MIR mode	Input pulse length 217 ns, 1.152 Mbit/s	t_{PW}	200		260	ns
RXD pulse width of output signal, 50 % FIR mode	Input pulse length 125 ns, 4 Mbit/s	t_{PW}	105	125	145	ns
RXD pulse width of output signal, 50 % FIR mode	Input pulse length 250 ns, 4 Mbit/s	t_{PW}	225		285	ns
RXD pulse width of output signal, 50 %	Input pulse length 16 Mbit/s, VFIR 39.5 ns < P_{wopt} < 43 ns	t_{PW}	32	42	52	ns
RXD rise time of output signal	20 % to 80%, C_L = 15 pF	$t_{r\ (RXD)}$	2	5	15	ns
RXD fall time of output signal	20 % to 80%, C_L = 15 pF	$t_{r\ (RXD)}$	2	5	15	ns
RXD fall time of output signal	90 % to 10%, C_L = 15 pF	$t_{r\ (RXD)}$	5		30	ns
RXD Jitter, leading edge, SIR mode	Input irradiance = 40 mW/m^2, 115.2 kbit/s				350	ns
RXD Jitter, leading edge, MIR mode	Input irradiance = 100 mW/m^2, 1.152 Mbit/s				40	ns
RXD Jitter, leading edge, FIR mode	Input irradiance = 100 mW/m^2, 4 Mbit/s				20	ns
RXD Jitter, leading edge	Input irradiance = 200 mW/m^2, 16 Mbit/s, VFIR mode			5	7	ns
RXD output pulse delay		t_{RXDdel}			1	µs
Latency		t_{LAT}		55	100	µs
Receiver Startup Time		t_{POR}		100	500	µs

Transmitter

T_{amb} = 25 °C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
IRED operating current internally controlled*)	V_{CC1} = 3.3 V, the maximum current is limited internally. An external resistor can be used to reduce the power dissipation at higher operating voltages, see derating curve.	I_D		8 16 32 64 128 256 512	 600	mA
Max. output radiant intensity	V_{CC} = 3.3 V, α = 0°,15° TXD = High, R1 = 0 Ω programmed to max. power level	I_e		0.3		mW/sr/mA
Output radiant intensity	V_{CC} = 5.0 V, α = 0°, 15° TXD = Low, programmed to shutdown mode	I_e			0.04	mW/sr
TXD pulse width of output signal, 50 %	Input pulse length 1.63 µs, 115.2 kbit/s	t_{PW}	1.45		2.20	µs
TXD pulse width of output signal, 50 %	Input pulse width 0.1 µs < t_{TXD} < 60 µs	t_{PW}		t_{TXD}		
	Input pulse width $t_{TXD} \geq$ 60 µs		20		60	µs
TXD pulse width of output signal, 50 %	Input pulse length 250 ns, (FIR, double pulse)	t_{PW}	240		260	ns
TXD pulse width of output signal, 50 %	Input pulse length 217.0 (MIR)	t_{PW}	115		260	ns
TXD pulse width of output signal, 50 % FIR mode	Input pulse length 125 ns (FIR)	t_{PW}	115	125	135	ns
TXD pulse width of output signal, 50 %	Input pulse length 41.7 ns	t_{PW}	38.3		45.0	ns
Output radiant intensity, angle of half intensity		α		± 24		°
Peak - emission wavelength		λ_p	870		900	nm
Spectral bandwidth				40		nm
Optical rise time, fall time		t_{ropt}, t_{fopt}			19	ns
Optical overshoot					15	%

*) Programmable using the"serial interface“ programming sequence, see Appendix A for implementation guidance and Appendix B for intensity values and range.

Recommended Circuit Diagram

Operated with a low impedance power supply the TFDU8108 series devices need no external components. However, depending on the entire system design and board layout, additional components may be required (see figure 3).

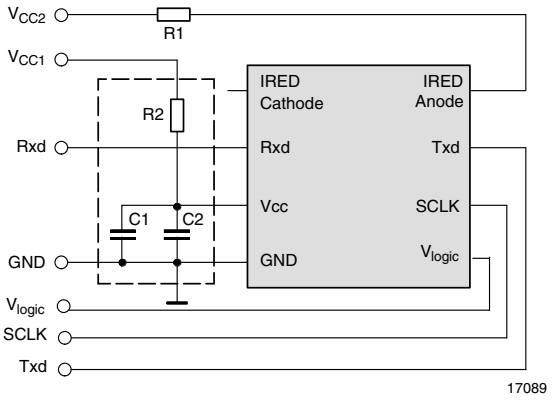


Figure 3. Recommended Application Circuit
All external components (R, C) are optional

Vishay transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring must be avoided. The inputs (TXD, SCLK) and the output RXD should be directly DC-coupled to the I/O circuit.

R1 is used for reducing the power dissipation when operating the device at a supply voltage of $V_{CC2} > 4$ V. For increasing the max. output power of the IRED, the value of the resistor should be reduced. It should be dimensioned to keep the IRED anode voltage below 4 V for using the full temperature range. For device and eye protection the pulse duration and current are internally limited.

R2, C1 and C2 are optional and dependent on the quality of the supply voltage V_{CC1} and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

The placement of these parts is critical. It is strongly recommended to position C2 as near as possible to the transceiver power supply pins. An electrolytic capacitor should be used for C1 while a ceramic capacitor is used for C2.

Recommended Application Circuit Components

Component	Recommended Value
C1	4.7 µF, 16 V
C2	0.1 µF, Ceramic
R1	**Recommended for $V_{CC2} \geq 4$ V** Depending on current limit
R2	< 10 Ω, 0.125 W

I/O and Software

For operating the device from a Controller I/O a driver software must be implemented.

Mode Switching and Programming

The generic IrDA "Serial Interface programming" needs no special settings for the device. Only the current control table must be taken into account. For the description see the Appendix A, B and C and the IrDA document "Serial Interface specification for transceivers"

Recommended Solder Profiles

Solder Profile for Sn/Pb Soldering

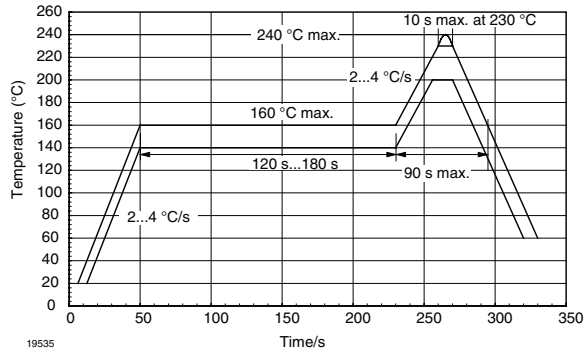


Figure 4. Recommended Solder Profile for Sn/Pb soldering

Lead (Pb)-Free, Recommended Solder Profile

The TFDU8108 is a lead (Pb)-free transceiver and qualified for lead (Pb)-free processing. For lead (Pb)-free solder paste like Sn (3.0 - 4.0) Ag (0.5 - 0.9) Cu, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 5 and 6 are VISHAY's recommended profiles for use with the TFDU8108 transceivers. For more details please refer to the application note
“SMD Assembly Instructions”
(http://www.vishay.com/docs/82602/82602.pdf).

A ramp-up rate less than 0.9 °C/s is not recommended. Ramp-up rates faster than 1.3 °C/s could damage an optical part because the thermal conductivity is less than compared to a standard IC.

Wave Soldering

For TFDUxxxx and TFBSxxxx transceiver devices wave soldering is not recommended.

Manual Soldering

Manual soldering is the standard method for lab use. However, for a production process it cannot be recommended because the risk of damage is highly dependent on the experience of the operator. Nevertheless, we added a chapter to the above mentioned application note, describing manual soldering and desoldering.

Storage

The storage and drying processes for all VISHAY transceivers (TFDUxxxx and TFBSxxx) are equivalent to MSL4.

The data for the drying procedure is given on labels on the packing and also in the application note "Taping, Labeling, Storage and Packing"
(http://www.vishay.com/docs/82601/82601.pdf).

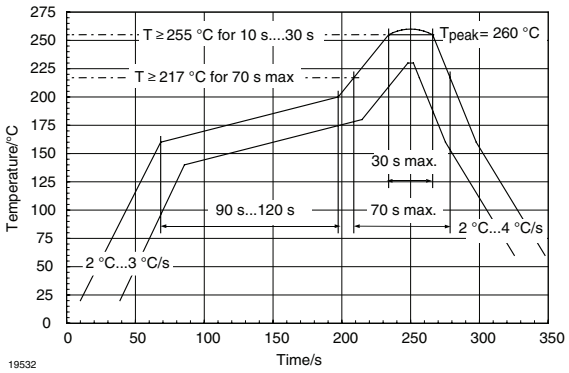


Figure 5. Solder Profile, RSS Recommendation

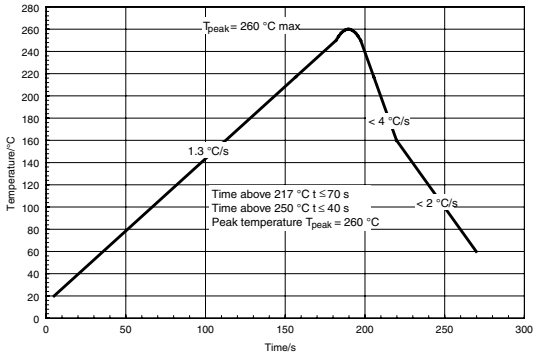


Figure 6. RTS Recommendation

Current Derating Diagram

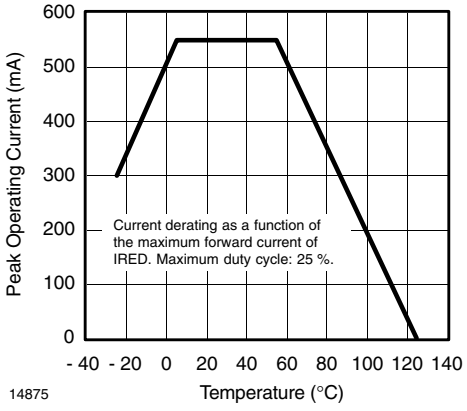
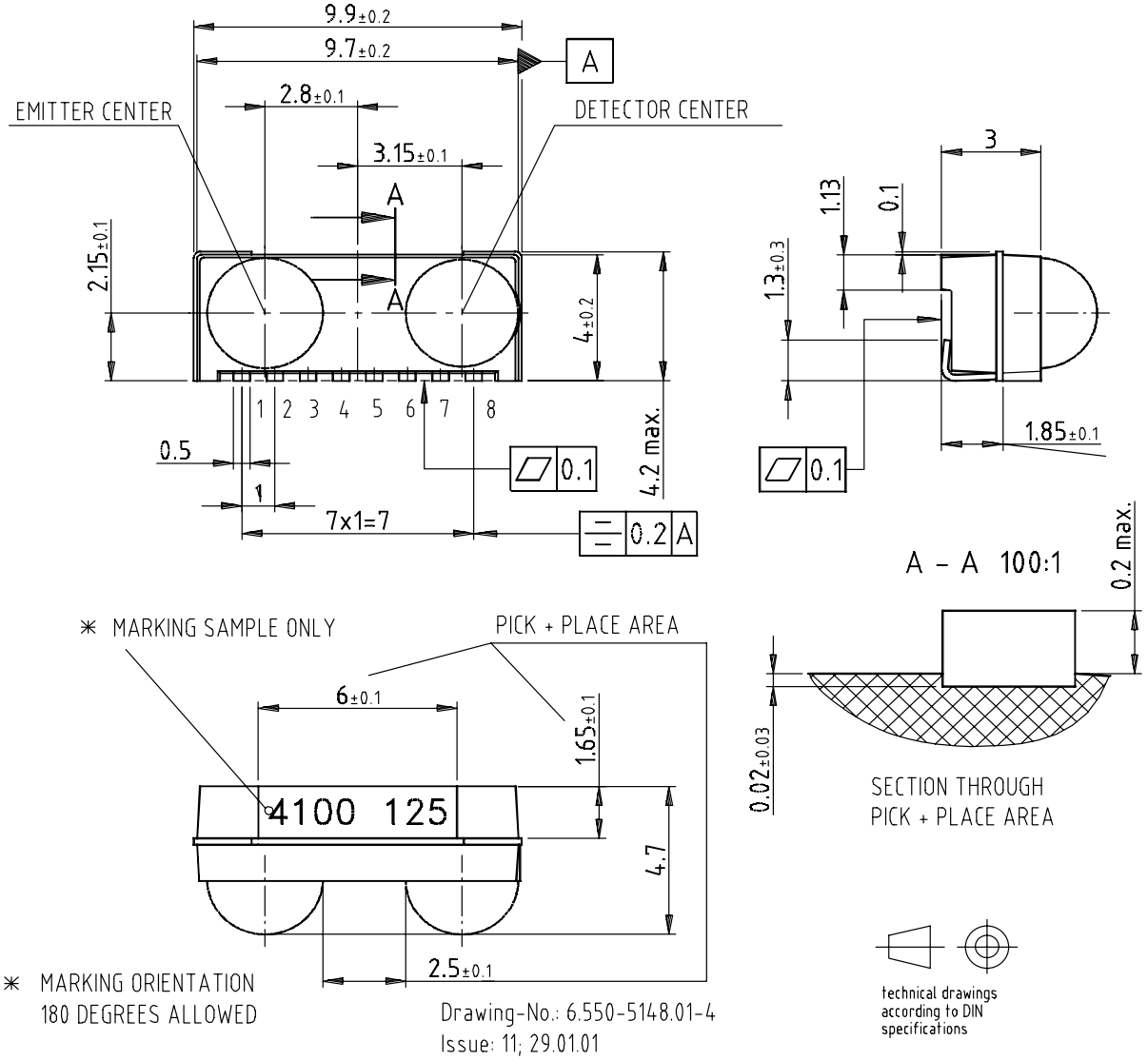


Figure 7. Current Derating Diagram

TFDU8108 - BabyFace (Universal) Package

(Mechanical Dimensions)



18473-1

Figure 8. Mechanical drawing, dimensions in mm, tolerance ± 0.2 mm if not otherwise shown

Recommended SMD Pad Layout

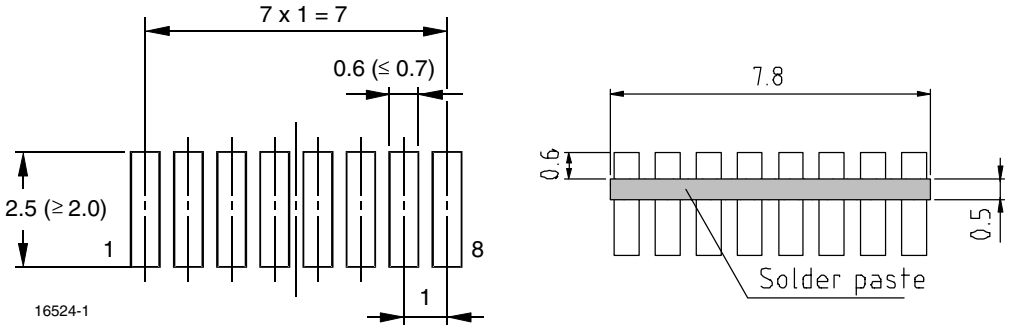


Figure 9. Mechanical drawing, dimensions in mm, tolerance ± 0.2 mm if not otherwise shown

Reel Dimensions

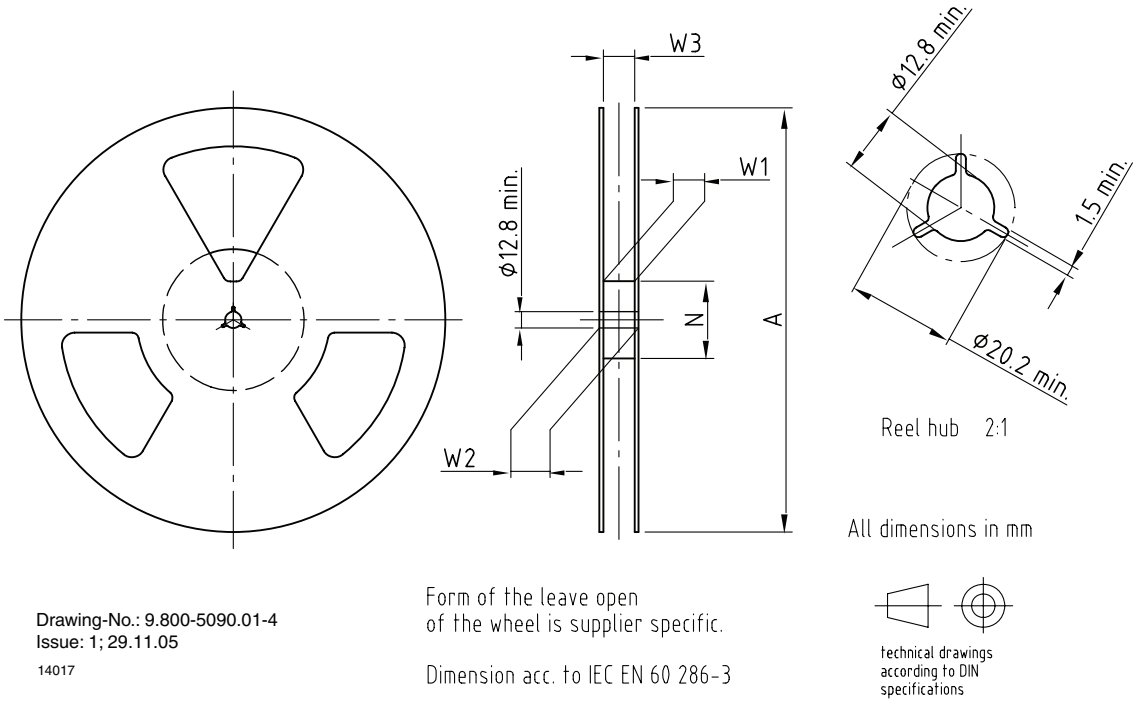
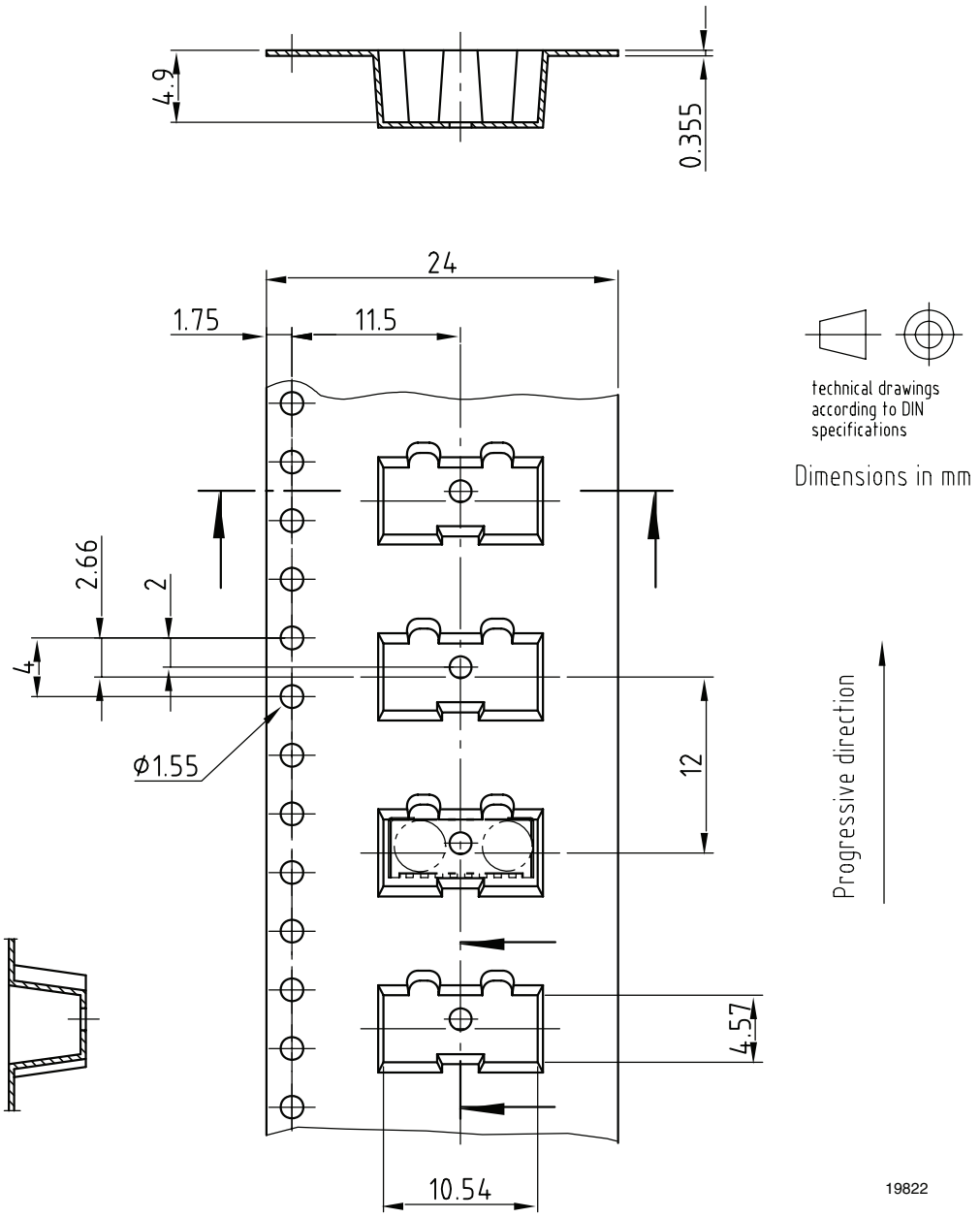


Figure 10. Reel dimensions, dimensions in mm, tolerance ± 0.2 mm

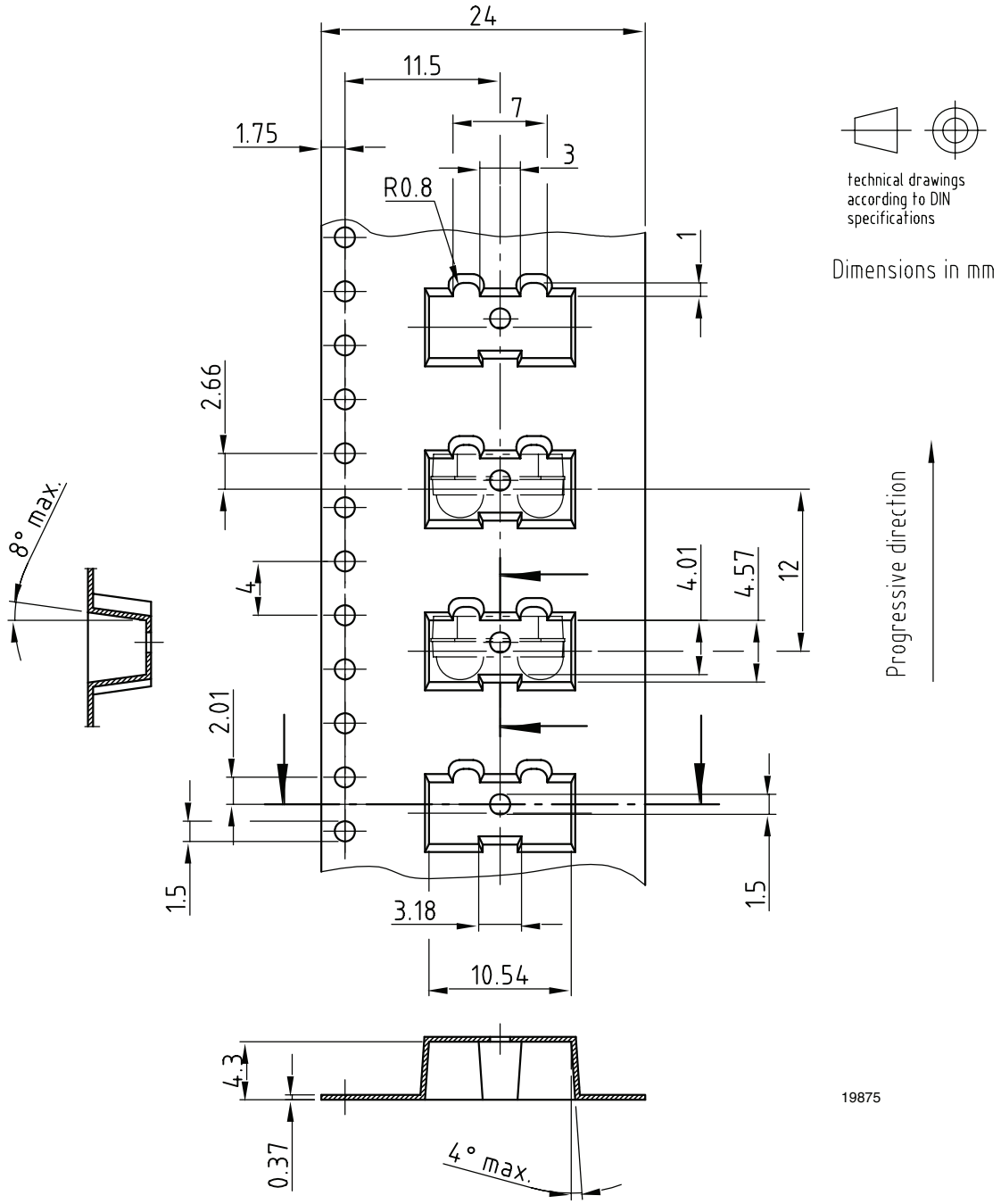
Tape Width	A max.	N	W_1 min.	W_2 max.	W_3 min.	W_3 max.
mm	mm	mm	mm	mm	mm	mm
24	330	60	24.4	30.4	23.9	27.4

Tape Dimensions



Drawing-No.: 9.700-5251.01-4
Issue: 3; 02.09.05

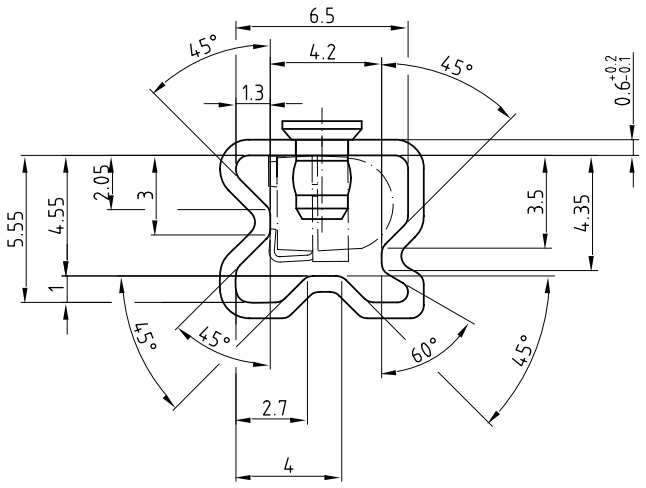
Figure 11. Tape drawing,TFDU8108 for top view mounting, tolerance ± 0.1 mm



Drawing-No.: 9.700-5297.01-4
Issue: 1; 04.08.05

Figure 12. Tape drawing, TFDU8108 for side view mounting
after mounting, tolerance ± 0.1 mm

Tube drawing



With stopper pins
Tolerance: ±0.5mm
Length: 575±1mm
All dimensions in mm

Drawing-No.: 9.700-5187.01-4 Drawing refers to following types: TFDU .10.
Issue: 1; 13.05.05

19496

Figure 13. Tube drawing

Appendix A
Serial Interface Implementation

Basics of the IrDA Definitions

The data lines are multiplexed with the transmitter and receiver signals and separate clocks are used since the transceivers respond to the same address. When no infrared communication is in progress and the serial bus is idle, the IRTX line is kept low and IRRX is kept high.

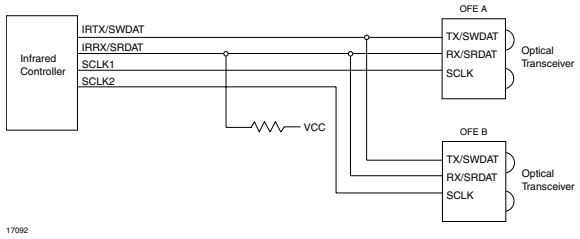


Figure 14. Interface to Two Infrared Transceivers

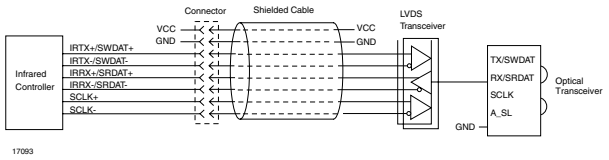


Figure 15. Infrared Dongle with Differential Signaling

Functional description

The serial interface is designed to interconnect two or more devices. One of the devices is always in control of the serial interface and is responsible for starting every transaction. This device functions as the bus master and is always the infrared controller. The infrared transceivers act as bus slaves and only respond to transactions initiated by the master. A bus transaction is made up of one or two phases. The first phase is the Command Phase and is present in every transaction. The second phase is the Response Phase and is present only in those transactions in which data must be returned from the slave. If the operation involves a data transfer from the slave, there will be a Response Phase following the Command Phase in which the slave will output the data.

The Response Phase, if present, must begin 4 clock cycles after the last bit of the Command Phase, as shown in figures 16 and 17, otherwise it is assumed that there will be no response phase and the master can terminate the transaction.

The SCLK line is always driven by the master and is used to clock the data being written to or read from the slave.

This line is driven by a totem-pole output buffer. The SCLK line is always stopped when the serial interface is idle to minimize power consumption and to avoid any interference with the analog circuitry inside the slave. There are no gaps between the bytes in either the Command or Response Phase. Data is always transferred in Little Endian order (least significant bit first). Input data is sampled on the rising edge of SCLK. IRTX/SWDAT output data from the controller is clocked by SCLK falling edge. IRRX/SRDAT output data from the slave is clocked by SCLK rising edge. Each byte of data in both Command and Response Phases is preceded by one start bit. The data to be written to the slave is carried on the IRTX/SWDAT line. When the control interface is idle, this line carries the infrared data signal used to drive the transmitter LED. When the first low-to-high transition on SCLK is detected at the beginning of the command sequence, the slave will disable the transmitter LED. When the first low-to-high transition on SCLK is detected at the beginning of the command sequence, the slave will disable the transmitter LED. The infrared controller then outputs the command string on the IRTX/SWDAT line. On the last SCLK cycle of the command sequence the slave re-enables the transmitter LED and normal infrared transmission can resume. No transition on SCLK must occur until the next command sequence otherwise the slave will disable the transmitter LED again. Read data is carried on the IRRX/SRDAT line. The slave disables the internal signal from the receiver photo diode during the response phase of a read transaction. The addressed slave will output the read data on the IRRX/SRDAT line regardless of the setting of the Receiver Output Enable bit in the main control register (main-ctrl-0). Non addressed slaves will tri-state the IRRX/SRDAT line. When the transceiver is powered up, the IRTX/SWDAT line should be kept low and SCLK should be cycled at least 30 times by the infrared controller before the first command is issued on the IRTX/SWDAT line, see figure 18. This guarantees that the transceiver interface circuitry will properly initialize and be ready to receive commands from the controller. In case of a multiple transceiver configuration, only one transceiver should have the receiver output enabled.

A series resistor (approx. 200 Ω) should be placed on the receiver output from each transceiver to prevent large currents in case a conflict occurs due to a programming error.

Note: Generally the abbreviations IRTX/IRRX and TXD/RXD are used for the data transmission lines for the optical communication. IRTX/IRRX is mostly used at the controller, TXD/RXD at the transceiver

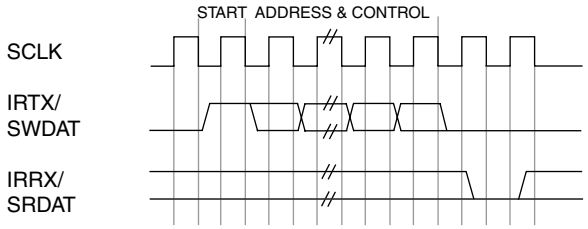


Figure 16. Special Command Waveform

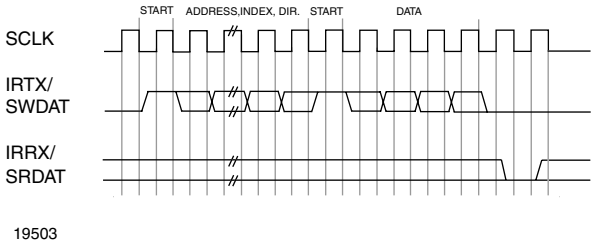


Figure 17. Write Data Waveform

Note: If the APEN bit in control register 0 is set to 1, the internal signal from the receiver photo diode is disconnected and the IRRX/SRDAT line is pulsed low for one clock cycle at the end of a write or special command.

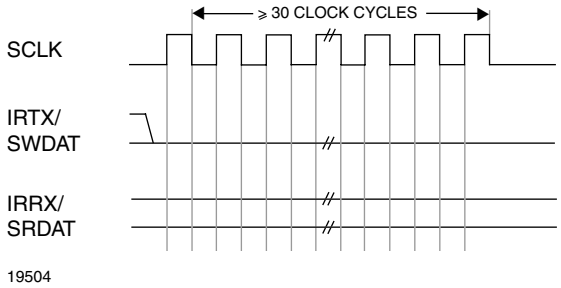


Figure 18. Initial Reset Timing

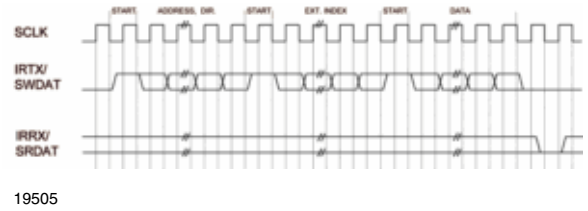


Figure 19. Write Data Waveform with Extended Index

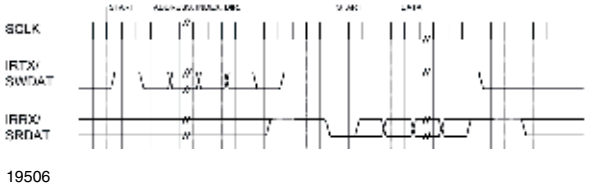


Figure 20. Read Data Waveform

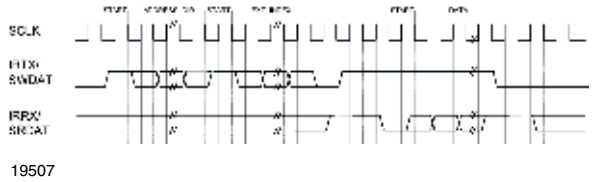


Figure 21. Read Data Waveform with Extended Index

Note: During a read transaction the infrared controller sets the IRTX/SWDAT line high after sending the address and index byte (or bytes). It will then set it low two clock cycles before the end of the transaction. It is strongly recommended that optical transceivers monitor this line instead of counting clock cycles in order to detect the end of the read transaction. This will always guarantee correct operation in case two or more transceivers from different manufacturers are sharing the serial interface.

Switching Characteristics

Maximum capacitive load = 20 pF*)

Symbol	Parameters	Test Conditions	Min.	Max.	Unit
t_{CKp}	SCLK Clock Period	Rising edge of SCLK to next rising edge of SCLK	250	infinity	ns
t_{CKh}	SCLK Clock High Time	At 2.0 V for single-ended signals	60		ns
t_{CKl}	SCLK Clock Low Time	At 0.8 V for single-ended signals	80		ns
t_{DOtv}	Output Data Valid (from infrared controller)	After falling edge of SCLK		40	ns
t_{DOth}	Output Data Hold (from infrared controller)	After falling edge of SCLK	0		ns
t_{DOrv}	Output Data Valid (from optical transceiver)	After rising edge of SCLK		40	ns
t_{DOrh}	Output Data Hold (from optical transceiver)	After rising edge of SCLK		40	ns
t_{DOrf}	Line Float Delay	After rising edge of SCLK		60	ns
t_{DIs}	Input Data Setup	Before rising edge of SCLK	10		ns
t_{DIh}	Input Data Hold	After rising edge of SCLK	5		ns

*) Maximum capacitive load = 20 pF. That is is different from "Serial interface - specification". For the bus protocol see "RECOMMENDED SERIAL INTERFACE FOR TRANSCEIVER CONTROL, Draft Version 1.0a, March 29, 2000, IrDA". In Appendix B the transceiver related data are given.

Appendix B

Application Guideline

In the following some guideline is given for handling the TFDU8108 in an application ambient, especially for testing. It is also a guideline for interfacing with a controller. We recommend to use for first evaluation the Vishay IRM1802 controller. For more information see the special data sheet. Driver software is available on request. Contact irdc@vishay.com.

Serial Interface Capability of the Vishay IrDA Transceivers

Abstract

A serial interface allows an infrared controller to communicate with one or more infrared transceivers. The basic specification of the IrDA specified interface is described in "Serial Interface for Transceiver Control, v 1.0a", IrDA.

This part of the document describes the capabilities of the serial interface implemented in the Vishay IrDA transceivers TFDU8108. The VFIR (16 Mbit/s) device TFDU8108 and the FIR device TFDU6108 (4 Mbit/s) are using the same interface specification (with specific identification and programming).

IrDA Serial Interface Basics

The "Serial Interface for Transceiver Control" is a master/slave synchronous serial bus, which uses the TXD and RXD as data lines and the SCLK as clock line with a minimum period of 250 ns. The transceiver works always as slave and jumps into a control mode on the first rising edge of the clock line remaining there until the command phase is finished. After power-on, it is required to initialize the transceiver by at least 30 clock cycles of SCLK with TXD continuously low before starting programming.

If TXD gets active (high) during the initialization period the initialization must be repeated.

A data word consists of one byte preceded by one start bit.

The specified serial interface allows the communication between infrared controller and transceiver through write and read transactions. In two register blocks with different functions all data is stored for operating the interface. The Main Control Registers allow write and read transactions and here the executable configuration of the device is stored. The Extended Indexed Registers contain the description of the supported functionality of the device and can be read only.

Power-on

After power on the transceiver is in the default mode shown in table B1.

Addressing

The transceiver is addressable by three address bits. There are individual and common addresses with the values shown in table B2.

Registers Data Depth

In general data registers use a data depth of eight bits. Sometimes it is not necessary to implement the full depth. In such cases the invisible bits are considered as a zero.

Registers

The register content is listed in the tables B4 to B7.

Data Acknowledgment

Data acknowledgement generated by the slave is available if the APEN bit is set to 1 in the common control register, see the "main_ctrl_0" register values table B4. In IrDA default state this functionality is disabled. It is recommended to enable this function.

Table B1: Power-on default mode

Function	TFDU8108
Power Mode (active or sleep)	sleep
RXD (Receive)	disable (floating tri-state)
TXD_LED (Emitter driver):	disable
APEN (Acknowledgment)	disable
Infrared Operating Mode (Speed)	SIR
Transmitter Power (Intensity setting)	max. SIR power level

Table B2: Addressing

Description	Address value ADDR [2:0]
Individual address	010
Common (broadcast) address	111

Table B3: Index Commands

Commands INDEX [3:0]	Mode write/read	Actions	Register Name	Data Bits Data	TFDU8108 default
0h	W/R	Common control	main-ctrl-0 register	[4:0]	00h
1h	W/R	Infrared mode	main-ctrl-1 register	[7:0]	00h
2h	W/R	TXD power level	main-ctrl-2 register	[7:4]	70h
3h - Bh	X	Not used			
Ch	X	Not used			
Dh	W	Reset transceiver, Only one byte!			
	R	Not used			
Eh	X	Not used			
Fh	W	Not used			
	R	Extended indexing			

Note: The main_ctrl_1 register is written software dependent on the offset value stored in ext_ctrl_7 and ext_ctrl_8 registers.
The main_ctrl_1 register can be set to the following values, shown in the table.

Tables B4 to B7: Control Register Values

The status of the entire transceiver is stored in the control registers.

Table B4: Register main-ctrl-0

Command structure:

C	0	0	0	0	bit 0	bit 1	bit 2	1	bit 0	bit 1	bit 2	0	bit 4	0	0	0
	INDEX [3:0], 0h				ADDR [0:2]				DATA [7:0]							

C is the transfer direction:

- C = 1: WRITE or RESET transaction
- C = 0: READ transaction

Main-ctrl-0, register values

Value	Function			Default
bit 0	PM SL - Power Mode Select	low power-mode (shutdown (sleep) mode)	normal operation power mode	shutdown
bit 1	RX OEN - Receiver Output Enable	IRRX/SRDAT line disable (tristated)	IRRX/SRDAT line enabled	disabled
bit 2	TLED EN - Transmitter LED Enable	disabled	enabled	disabled
bit 3	not used			not used
bit 4	APEN*)	don't acknowledge	acknowledge	disabled

*) APEN - Acknowledge Pulse Enable, (optional)
This bit is used to enable the acknowledge pulse. When it is set to 1 and RX OEN is 1 (receiver output enabled) the IRRX/SRDAT line will be set low for one clock cycle upon successful completion of every write command or special command with individual (non broadcast) transceiver address. The internal signal from the receiver photo diode is disconnected when this bit is set to 1.

Table B5: Register main-ctrl-1

Command structure:

C	1	0	0	0	bit 0	bit 1	bit 2	1	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
	INDEX [3:0], 1h				ADDR [0:2]				DATA [7:0]							

Main-ctrl-1, register values

DATA [7:0]	Function
00h	SIR (default)
01h	MIR
02h	FIR
03h	Apple Talk® (FIR functionality)
05h	VFIR - 16
08h	Sharp IR® (SIR functionality)
20h	IrDA CIR

Depending on the values of "ext_ctrl_7" and "ext_ctrl_8" check for correct main_ctrl_1. In case of an error, the transceiver will load 00h into the main_ctrl_1 register and will not give an acknowledgement.

Table B6: Register main-ctrl-2

Command structure:

C		1	0	0	bit 0	bit 1	bit 2	1	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
	INDEX [3:0], 1h				ADDR [0:2]				DATA [7:0]							

Main-ctrl-2, DATA [7:0], bit 4 to bit 7

DATA [7:0]	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	TXD - IRED [mA]	Ie [mW/sr] 15° (typ. on axis)	Link distance on axis	Recommended for
8xh-Fxh	1	x	x	x	x	x	x	x	512	140 (240)	VFIR > 0.7 m, FIR > 1 m (link distance limited by receiver sensitivity)	VFIR/FIR standard
7xh*)	0	1	1	1	x	x	x	x	**256**	> 70 (120) *)	**SIR >1 m FIR > 0.7 m, VFIR > 0.5 m**	**SIR, More Ext. FIR LP**
6xh	0	1	1	0					128	35 (60)	SIR > 0.70 m FIR > 0.50 m VFIR > 0.30 m	Extended FIR Low Power
5xh	0	1	0	1					64	16 (30)	SIR > 0.5 m FIR > 0.30 m VFIR > 0.30 m	VFIR Low Power/ FIR Low Power
4xh	0	1	0	0					(48)			
3xh	0	0	1	1					32	8 (19)	SIR > 0.35 m FIR > 0.20 m VFIR > 0.20 m	SIR Low Power
2xh	0	0	1	0					16	40 (10)		SIR Low Power, min without optical windows
1xh	0	0	0	1					8	(5)	SIR > 0.15 m FIR > 0.10 m VFIR > 0.10 m	Close distance, e.g. Docking station
0xh	0	0	0	0	x	x	x	x	0		0	

*) Device is tested under this condition. Default setting is 7xh.

IRED current I_f [mA]	Intensity I_e [mW/sr]	d[m] at E_e = 100 mW/m^2	d[m] at E_e = 40 mW/m^2	d[m] at E_e = 90 mW/m^2	d[m] at E_e = 225 mW/m^2
512	240	1.55	2.45	1.63	1.03
256	120	1.10	1.73	1.15	0.73
128	60	0.77	1.22	0.82	0.52
64	30	0.55	0.87	0.58	0.37
48	22.5	0.47	0.75	0.50	0.32
32	15	0.39	0.61	0.41	0.26
16	7.5	0.27	0.43	0.29	0.18
8	3.75	0.19	0.31	0.20	0.13

Note: Calculated expected range in dependence of IRED drive current for the case that the receiver sensitivity is not limiting the range, on axis, for information only.

IRED current I_f [mA]	Intensity I_e [mW/sr]	d[m] at E_e = 100 mW/m^2	d[m] at E_e = 40 mW/m^2	d[m] at E_e = 90 mW/m^2	d[m] at E_e = 225 mW/m^2
512	140.0	1.18	1.87	1.25	0.79
256	70.0	0.15	0.23	1.16	0.10
128	35.0	0.59	0.94	0.62	0.39
64	17.5	0.42	0.66	0.44	0.28
48	13.1	0.36	0.57	0.38	0.24
32	8.8	0.30	0.47	0.31	0.20
16	4.4	0.21	0.33	0.22	0.14
8	2.2	0.15	0.23	0.16	0.10

Note: Calculated expected range in dependence of IRED drive current for the case that the receiver sensitivity is not limiting the range; 15° off-axis, for information only.

Table B7: Reading Extended Indexed Registers

Note: Read Data with Extended Index E_INDX is one of the Extended Indexed Registers. It must be addressed via a precursor of writing all 1s into the normal index location, thus INDEX[3:0] = Fh. It is an 8 bit address value, which must be followed by 3 SCLK cycles plus a start clock before reading the DATA value. As in the normal Read Transaction, the input signal, TXD, must be set one clock cycle on LOW (master ready to receive) and then on HIGH for the next 3 SCLKs and continuing through the entire Response Phase. The corresponding reaction of the RXD line and the 8 bit DATA value is then read out as depicted below, noting that the Read Data value comes after the 3 SCLK cycles.

Read Command structure:

0	1	1	1	1	bit 0	bit 1	bit 2	1	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
C	INDEX [3:0], Fh				ADDR [0:2]				E_INDEX [0:7]							

Response:

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
DATA [0:7]							

Extended Indexed Registers

Action	E_INDEX [7:0]	Register name	DATA [7:0] in TFDU8108	Definition default in the TFDU8108
Manufacture ID	00h	ext_ctrl_0	0Bh	Chip information (Factory reserved)
Read Support, Device ID	01h	ext_ctrl_1	C6h	Device ID
Receiver Recovery Time Power On Stabilization	04h	ext_ctrl_4	23h	100 µs to 500 µs
Receiver Stabilization	05h	ext_ctrl_5	30h	0

Action	E_INDEX [7:0]	Register name	DATA [7:0] in TFDU8108	Definition default in the TFDU8108
SCLK Max. Frequency (4MHz)				4 MHz
Common Capabilities	06h	ext_ctrl_6	03h	Low Power Mode and Programmable Transmitter Power supported
Supported Infrared Modes	07h	ext_ctrl_7	2Fh	All listed in Receive Mode
Supported Infrared Modes	08h	ext_ctrl_8	01h	Sharp IR
Mask ID: Released Ver. Set, followed by Revision Letter	F0h	ext_ctrl_240	0Ah	Chip information (Factory reserved)

Invalid Commands Handling

Commands and register addresses, which cannot be encoded by the Serial Interface, are ignored by the internal logic as invalid data. Below the different types invalid command handling and the slave reaction is shown.

Reset

Two ways to set the serial interface into a defined state are available: The brute force method is to switch the power off and on and let the device recover in the default state. The software method is to set the IRTX/SWDAT line low for ≥ 30 clock cycles of the clock line. If this line is detected as low for ≥ 30 clock cycles the transceiver is set into the command start state and all registers are set to the as default implemented values.

Table B8: Invalid Commands Handling

Description	Master Command	Slave Reaction on RXD/SRDAT
Invalid command in read mode	Index [3:0] & C = 0	no reaction
Invalid command in write mode	Index [3:0] & C = 1	No acknowledgement generating independent of the value of APEN
Valid command in invalid read mode	Index [3:0] & C = 0	no reaction
Valid command in invalid write mode	Index [3:0] & C = 1	No acknowledgement generating independent of the value of APEN
Valid command in valid write mode and invalid data	Index [3:0] & C = 1	No acknowledgement generating independent of the value of APEN
Broadcast address in read mode	ADDR [2:0] = 111 & C = 0	no reaction

No reaction means that the slave does not start the respond phase.

C is the transfer direction:

- C = 1: WRITE or RESET transaction
- C = 0: READ transaction

Appendix C

Serial Interface Programming Guide

The serial interface port of TFDU8108 enables an interface controller to communicate using a standardized protocol, recall module ID and capability information, and implement receiver bandwidth mode switching, LED power control, shutdown and some other functions.

This interface requires three signal lines: a clock line (SCLK) that is used for timing, and two unidirectional lines multiplexed with the transmitter (TXD, write) and receiver (RXD, read) signal lines.

Programming sequence formats supported are

- one-byte special commands
- two-byte write commands
- two-byte read commands
- three-byte read commands

One-byte special command sequences are reserved for time-critical actions, while the two-byte write command is predominantly used to set basic transceiver characteristics. More information can be found in the IrDA document "Serial Interface for Transceiver Control, v 1.0a" on http://www.IrDA.org.

Serial Interface Timing Specifications

In general, serial interface programming sequences are similar to any clocked-data protocol:

- there is a range of acceptable clock rates, measured from rising edge to rising edge
- there is a minimum data setup time before clock rising edges
- there is a minimum data hold time after clock rising edges

Recommended programming timing:

- f_{SCLK} < 8 MHz (according to the Serial Interface Standard, quasi-static programming is possible)
- T_{SCLK} > 125 ns,
- T_{setup} > 10 ns,
- T_{hold} > 10 ns

The timing diagrams, see figure 22, show the setup and hold time for the serial interface programming sequences.

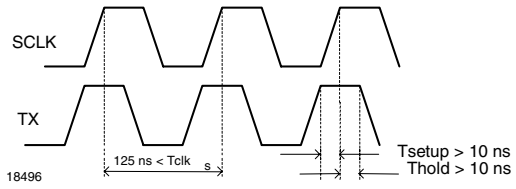


Figure 22. Programming Sequence

Protocol Specifications

The serial interface protocol is a command-based communication standard and allows for the communication between controller and transceiver by way of serial programming sequences on the clock (SCLK), transmit (TXD), and receive (RXD) lines. The SCLK line is used as a clocking signal and the transmit/receive lines are used to write/read data information. The protocol requires all transceivers to implement the write commands, but does not require the read-portion of the protocol to be implemented (though all transceivers must at least follow the various commands, even if they perform no internal action as a result). This serial interface follows but does not support all read/ write commands or extended commands, supporting only the special commands and basic write/read commands. Write commands to the transceiver take place on the SCLK and TXD lines and may use the RXD line for acknowledgment. A command may be directed to a single transceiver on the SCLK, TXD and RXD bus by specifying a unique three-bit transceiver address, or a command may be directed to all transceivers on the bus by way of a special three-bit broadcast address code. The Vishay VFIR transceiver TFDU8108 will respond to transceiver address 010 and the broadcast address 111 only; it ignores all other transceiver addresses.

All commands have a common "header" or series of leading bits, which take the form shown below.

first bit sent to transceiver — last bit sent to transceiver.

0	1	0/1	I0	I1	I2	I3	A0	A1	A2	...	...
Sync. Bits		R/W 0/1	Commands Index				Transceiver Address				

The bits shown are placed on the TXD (DATA) line and clocked into the transceiver using the rising edge of the SCLK signal. Only the data bits are shown as it is assumed that a clock is always present, and that the transceiver samples the data on the rising edge of each clock pulse.

Note: as illustrated in the diagram above, the protocol uses "Little Endian" ordering of bits, so that the LSB is sent first, and the MSB is sent last for register addresses, transceiver addresses, and read/write data bytes. The notation that follows presents all addresses and data in LSB-to-MSB order (bits 0, 1, 2, 3, ... 7) unless otherwise stated.

One-byte Special Commands

One-byte special commands are used for time-critical transceiver commands, such as full transceiver reset. A total of six special commands are possible, although only one command is available on the TFDU8108.

0	1	1	I0	I1	I2	I3	A0	A1	A2	0	0
Sync. Bits		W	Special Command Code				Transceiver Address			Stop Bits	

Command	Programming Sequence (Binary)
RESET (Set all registers to default value)	011 1011 010 00

Two-byte Write Commands

Two-byte write commands are used for setting the contents of transceiver registers which control transceiver such as shutdown/enable, receiver mode, LED power level, etc. The register space requires four register address bits (INDEX), although three codes are used for controlling the transceiver (see above). The 1111 escape code is for extended commands. The 3-bit transceiver address (ADDR) is for selecting the destination, e.g. 010 to TFDU8108 and 001 to TFDU6108. The second byte is data field (DATA) for setting the characteristics of the transceiver module, e.g. SIR mode (00) or VFIR (05) when the register address is 0001.

The basic two-byte write command is illustrated below:

0	1	1	I0	I1	I2	I3	A0	A1	A2	A3	D0..07	0	0
Sync. Bits		W	Commands Index				Transceiver Address				8 Data Bits	Stop Bits	

Some important serial interface programming sequences are shown in table C1.

Table C1: Serial interface programming sequences

Command		TFDU8108 Programming Sequence (Transceiver address: 010)
Common Ctrl main_ctrl_0	**DATA**	SYNC/C/INDEX/ADDR/1/DATA/STOP
Normal (Enable all)	0Fh	01 1 0000 010 1 11110000 00
Shutdown	00h	01 1 0000 010 1 00000000 00
Receiver Mode main_ctrl_1	**DATA**	
SIR	00h	01 1 1000 010 1 00000000 00
MIR	01h	01 1 1000 010 1 10000000 00
FIR	02h	01 1 1000 010 1 01000000 00
Apple Talk	03h	01 1 1000 010 1 11000000 00
VFIR	05h	01 1 1000 010 1 10100000 00
Sharp-IR	08h	01 1 1000 010 1 00010000 00
LED Intensity main_ctrl_2	**DATA**	
8 mA	1xh	01 1 0100 010 1 00001000 00
16 mA	2xh	01 1 0100 010 1 00000100 00
32 mA	3xh	01 1 0100 010 1 00001100 00
64 mA	5xh	01 1 0100 010 1 00001010 00
128 mA	6xh	01 1 0100 010 1 00000110 00
256 mA	7xh	01 1 0100 010 1 00001110 00
512 mA	Fxh	01 1 0100 010 1 00001111 00

Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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and may do so without further notice.
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