MF0ICU1

MIFARE Ultralight contactless single-ticket IC

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028639

Product data sheet
COMPANY PUBLIC

1. General description

The MIFARE MF0ICU1 has been developed by NXP Semiconductors to be used in a contactless smart ticket or smart card in combination with a Proximity Coupling Devices (PCD) in accordance with ISO/IEC 14443 A (see Ref. 1). It is intended for use as single trip or limited use tickets in public transportation networks, loyalty cards or day passes for events as a replacement for conventional ticketing solutions such as paper tickets, magnetic stripe tickets or coins.

As the usage of contactless proximity smart cards becomes more and more common, transport and event operators are switching to completely contactless solutions. The introduction of the MIFARE Ultralight for limited use tickets may lead to a reduction of system installation and maintenance costs. Terminals may be less vulnerable to damage and mechanical failures caused by ticket jams. MF0ICU1 can easily be integrated into existing schemes and even standard paper ticket vending equipment can be upgraded. This solution for low cost tickets can help operators to reduce the circulation of cash within the system.

The mechanical and electronical specifications of MIFARE Ultralight are tailored to meet the requirements of paper ticket manufacturers.

1.1 Contactless energy and data transfer

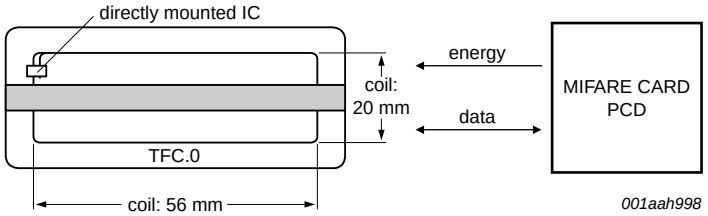
In the MIFARE system, the MF0ICU1 is connected to a coil with a few turns. The MF0ICU1 fits the TFC.0 (Edmondson) and TFC.1 (ISO) ticket formats as defined in BS EN753-2.

TFC.1 format tickets are supported by the MF0ICU10 chip which features a 17 pF on-chip resonance capacitor.

The smaller TFC.0 format tickets are supported by the MF0ICU11 chip which features a 50 pF on-chip resonance capacitor.

1.2 Anticollision

An intelligent anticollision function enables simultaneous multicard operation. The anticollision algorithm individually selects each card and ensures correct execution of a transaction with the selected card without interference from another card in the field.



Evaluations show that an operating distance of approximately 8 cm can be achieved with this ticket configuration (6 turn coil) using a MIFARE demonstration system.

Fig 1. MIFARE card reader

1.2.1 Cascaded Unique IDentification (UID)

The anticollision function is based on an IC individual serial number called Unique Identification (UID) for each IC. The UID of the MF0ICU1 comprises 7 bytes and supports ISO/IEC 14443-3 cascade level 2.

1.3 Security

- 7-byte UID in accordance with ISO/IEC 14443-3 for each device
- 32-bit user definable One-Time Programmable (OTP) area
- Field programmable read-only locking function per page

1.4 Naming conventions

Table 1. Naming conventions

MF0xxU1w/D MF0xxU1w01W/y7DL	Description
MF	MIFARE family
0	Ultralight product family
xx	Identifier for the package type IC ... bare die MOA4 ... contactless module
U1	Product: Ultralight
w	One character identifier for input capacitance 0 ... 17 pF 1 ... 50 pF
/D	Fixed ending for module type
/y7DL	y is a single character identifier for the wafer type S... bare die, 75 μm thickness, Au bumps, e-map file U... bare die, 120 μm thickness, Au bumps, e-map file

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2. Features and benefits

2.1 MIFARE RF interface ISO/IEC 14443 A

- Contactless transmission of data and supply energy
- Operating frequency of 13.56 MHz
- Data integrity of 16-bit CRC, parity, bit coding, bit counting
- 7 byte serial number (cascade level 2 according to ISO/IEC 14443-3)
- Fast counter transaction: < 10 ms
- Operating distance up to 100 mm depending on antenna geometry and reader configuration
- Data transfer of 106 kbit/s
- True anticollision
- Typical ticketing transaction: < 35 ms

2.2 EEPROM

- 512-bit, organized in 16 pages with 4 bytes per page
- 32-bit user definable One-Time Programmable (OTP) area
- Data retention time of 5 years
- Field programmable read-only locking function per page
- 384-bit user Read/Write area (12 pages)
- Write endurance 10000 cycles

3. Quick reference data

Table 2. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			-	13.56	-	MHz
C_i	input capacitance	17 pF version	[1]	14.85	17.0	20.13	pF
		50 pF version	[1]	42.5	50.0	57.5	pF
EEPROM characteristics							
$t_{cy(W)}$	write cycle time			-	3.8	-	ms
t_{ret}	retention time	T_{amb} = 22 °C		5	-	-	year
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C		10000	-	-	cycle

[1] LCR meter HP 4285: T_{amb} = 22 °C, Cp-D, f_i = 13.56 MHz, 2 Veff.

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4. Ordering information

Table 3. Ordering information

Type number	Package			
	Commercial Name	Name	Description	Version
MF0ICU1001W/S7DL	FFC	-	8 inch wafer, sawn, 75 μm thickness, on film frame carrier, electronic fail die marking according to SECSII format, Au bumps, 17 pF input capacitance	-
MF0ICU1101W/S7DL	FFC	-	8 inch wafer, sawn, 75 μm thickness, on film frame carrier, electronic fail die marking according to SECSII format, Au bumps, 50 pF input capacitance	-
MF0ICU1001W/U7DL	FFC	-	8 inch wafer, sawn, 120 μm thickness, on film frame carrier, electronic fail die marking according to SECSII format, Au bumps, 17 pF input capacitance	-
MF0ICU1101W/U7DL	FFC	-	8 inch wafer, sawn, 120 μm thickness, on film frame carrier, electronic fail die marking according to SECSII format, Au bumps, 50 pF input capacitance	-
MF0MOA4U10/D	MOA4	PLLMC	plastic leadless module carrier package; 35 mm SOT500-2 wide tape, 17 pF input capacitance	SOT500-2

5. Block diagram

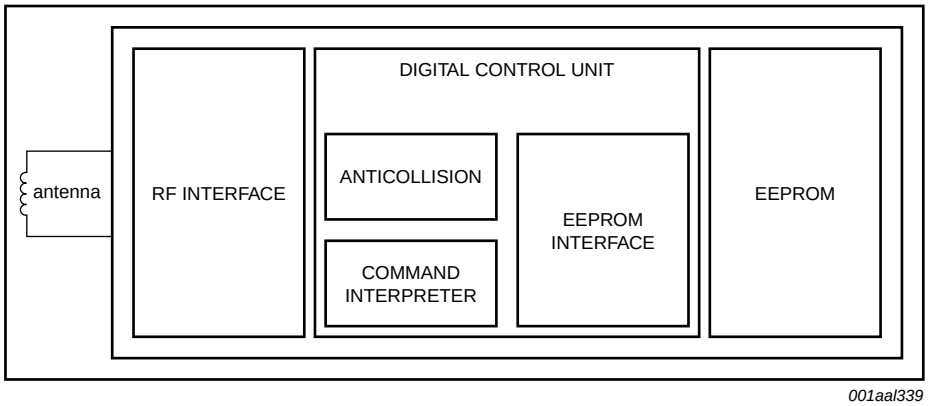


Fig 2. Block diagram

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6. Pinning information

6.1 Pinning

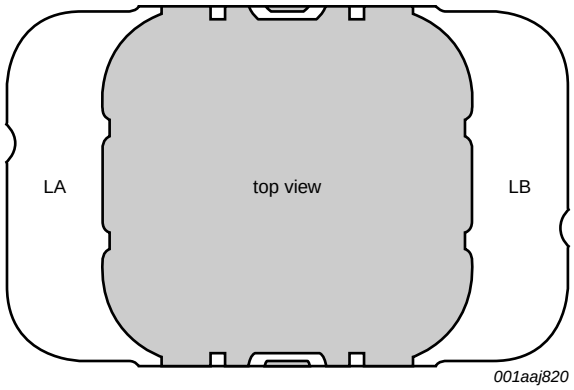


Fig 3. Contact assignments for SOT500-2 (MOA4)

Table 4. Bonding pad assignments to smart card contactless module

Contactless interface module		MF0ICU1DA4/01
Antenna contacts	**Symbol**	**Description**
LA	LA	antenna coil connection LA
LB	LB	antenna coil connection LB

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7. Functional description

7.1 Block description

The MF0ICU1 chip consists of a 512-bit EEPROM, RF interface and Digital Control Unit (DCU). Energy and data are transferred via an antenna consisting of a coil with a small number of turns which is directly connected to the MF0ICU1. No further external components are necessary. Please refer to Ref. 6 for details on antenna design.

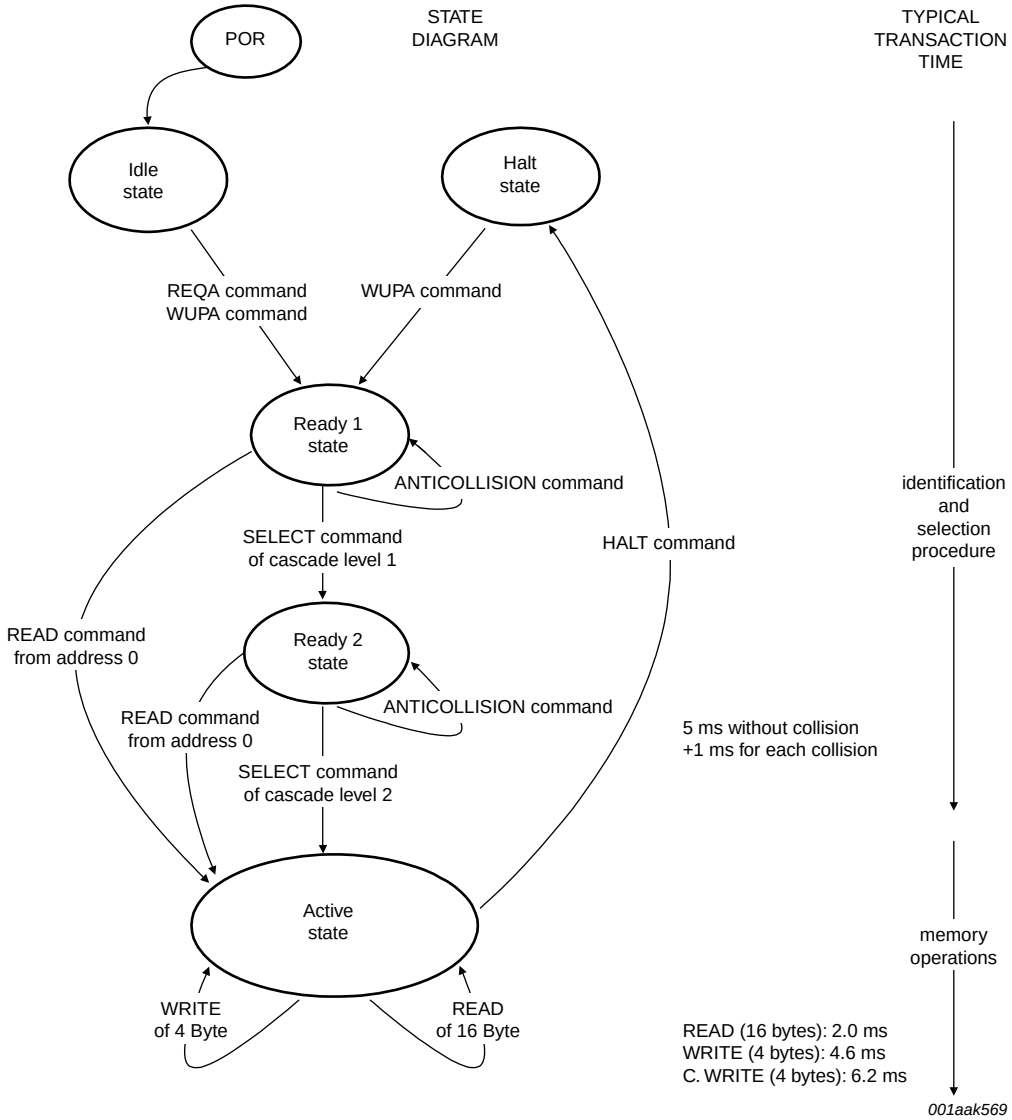
- RF interface:
  - Modulator/demodulator
  - Rectifier
  - Clock regenerator
  - Power-On Reset (POR)
  - Voltage regulator
- Anticollision: Multiple cards may be selected and managed in sequence
- Command interpreter: Processes commands supported by the MF0ICU1 to access the memory
- EEPROM interface
- EEPROM: 512 bits, organized in 16 pages of 4 bytes per page.
  - 80 bits reserved for manufacturer data
  - 16 bits used for the read-only locking mechanism
  - 32 bits available as OTP area
  - 384 bits user programmable Read/Write memory

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7.2 Communication overview

Commands are initiated by the PCD and controlled by the MF0ICU1's command interpreter. This processes the internal states and generates the appropriate response.



In all states, the command interpreter will return to the idle state on receipt of an unexpected command. If the IC was previously in the halt state, it will return to that state.

Fig 4. Communication principle state diagram

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7.2.1 Idle state

After a Power-On Reset (POR), the MF0ICU1 switches directly to the idle state. It only exits this state when a REQA or a WUPA command is received from the PCD. Any other data received while in the idle state is interpreted as an error and the MF0ICU1 remains Idle.

After a correctly executed HALT command out of the ACTIVE state, the halt state changes to the wait state which can be exited with a WUPA command.

7.2.2 Ready 1 state

In this state, the MF0ICU1 supports the PCD when resolving the first part of its UID (3 bytes) with the ANTICOLLISION or SELECT command from cascade level 1. This state is exited correctly after execution of either of the following commands:

- SELECT command from cascade level 1: the PCD switches the MF0ICU1 into Ready 2 state where the second part of the UID is resolved.
- READ command (from address 0): all anticollision mechanisms are bypassed and the MF0ICU1 switches directly to the active state.

Remark: If more than one MF0ICU1 is in the PCD field, a READ command from address 0 causes a collision due to the different serial numbers and all MF0ICU1 devices are selected.

Remark: Any other data received in the Ready 1 state is interpreted as an error and depending on its previous state the MF0ICU1 returns to the wait, idle or halt state.

7.2.3 Ready 2 state

In this state, the MF0ICU1 supports the PCD when resolving the second part of its UID (4 bytes) with the cascade level 2 ANTICOLLISION command. This state is usually exited using the cascade level 2 SELECT command.

Alternatively, state Ready 2 may be skipped using a READ command (from address 0) as described in state Ready 1.

Remark: If more than one MF0ICU1 is in the PCD field, a READ command from address 0 causes a collision due to the different serial numbers and all MF0ICU1 devices are selected.

Remark: The response of the MF0ICU1 to the cascade level 2 SELECT command is the Select Acknowledge (SAK) byte. In accordance with ISO/IEC 14443 this byte indicates if the anticollision cascade procedure has finished. It also defines the type of device selected for the MIFARE architecture platform. The MF0ICU1 is now uniquely selected and only this device will communicate with the PCD even when other contactless devices are present in the PCD field.

Remark: Any other data received when the device is in this state is interpreted as an error and depending on its previous state the MF0ICU1 returns to the wait, idle or halt state.

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7.2.4 Active state

In the active state either a 16-byte READ or 4-byte WRITE command can be performed. The ACTIVE state is gratefully exited with the HLTA command and upon reception the MF0ICU1 transits to the HALT state. Any other data received when the device is in this state is interpreted as an error. Depending on its previous state the MF0ICU1 returns to either the IDLE state or HALT state.

7.2.5 Halt state

The HALT and IDLE states constitute the two wait states implemented in the MF0ICU1. An already processed MF0ICU1 can be set into the HALT state using the HLTA command. In the anticollision phase, this state helps the PCD to distinguish between processed cards and cards yet to be selected. The MF0ICU1 can only exit this state on execution of the WUPA command. Any other data received when the device is in this state is interpreted as an error and the MF0ICU1 state remains unchanged. Refer to Ref. 3 for correct implementation of an anticollision procedure based on the IDLE and HALT states and the REQA and WUPA commands.

7.3 Data integrity

Reliable data transmission is ensured over the contactless communication link between PCD and MF0ICU1 as follows:

- 16-bit CRC for each block
- Parity bits for each byte
- Bit count checking
- Bit coding to distinguish between logic 1, logic 0 and no information
- Channel monitoring (protocol sequence and bit stream analysis)

7.4 RF interface

The RF interface is based on the ISO/IEC 14443 A standard for contactless smart cards. The RF field from the PCD is always present as it is used for the card power supply. However, it is sequentially interrupted during data transmission to allow the data to be sent. There is only one start bit at the beginning of each frame for data communication irrespective of direction. Each byte is transmitted with an odd parity bit at the end of the byte. The LSB of the byte with the lowest selected block address is transmitted first. The maximum frame length is 163-bit:
(16 data bytes + 2 CRC bytes = 16 * 9 + 2 * 9 + 1 start bit = 163).

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7.5 Memory organization

The 512-bit EEPROM memory is organized in 16 pages with 4 bytes per page. In the erased state the EEPROM cells are read as logic 0, in the written state as logic 1.

Table 5. Memory organization

Page address		Byte number			
Decimal	**Hex**	**0**	**1**	**2**	**3**
0	00h	serial number			
1	01h	serial number			
2	02h	serial number	internal	lock bytes	lock bytes
3	03h	OTP	OTP	OTP	OTP
4 to 15	04h to 0Fh	user memory			

7.5.1 UID/serial number

The unique 7-byte serial number (UID) and its two check bytes are programmed into the first 9 bytes of memory covering page addresses 00h, 01h and the first byte of page 02h. The second byte of page address 02h is reserved for internal data. These bytes are programmed by the IC manufacturer and because of the security requirements are write protected.

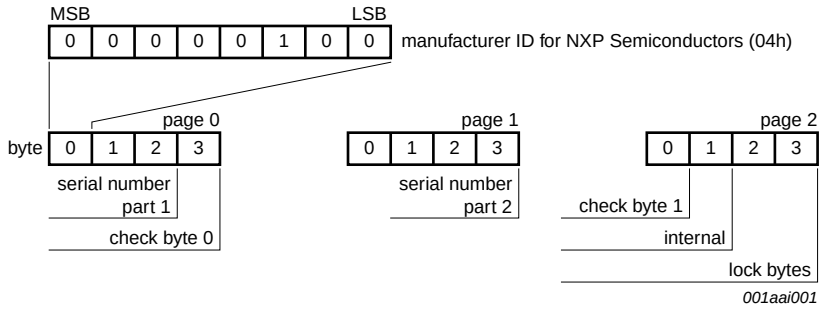


Fig 5. UID/serial number

In accordance with ISO/IEC 14443-3 Check Byte0 (BCC0) is defined as CT ⊕ SN0 ⊕ SN1 ⊕ SN2 and Check Byte 1 (BCC1) is defined as SN3 ⊕ SN4 ⊕ SN5 ⊕ SN6.

SN0 holds the Manufacturer ID for NXP Semiconductors (04h) in accordance with ISO/IEC 14443-3 and ISO/IEC 7816-6 AMD.1

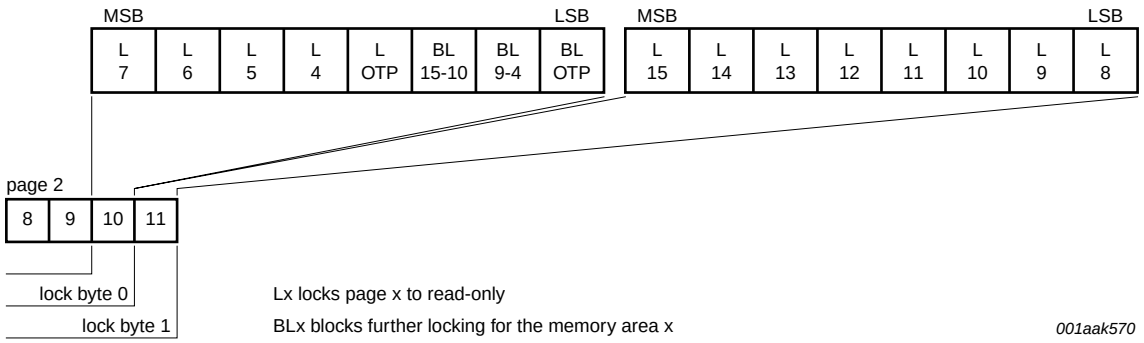
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7.5.2 Lock bytes

The bits of byte 02h and 03h of page 02h represent the field programmable read-only locking mechanism. Each page from 03h (OTP) to 0Eh can be individually locked by setting the corresponding locking bit Lx to logic 1 to prevent further write access. After locking, the page becomes read-only memory.

The three least significant bits of lock byte 0 are the block-locking bits. Bit 2 deals with pages 0Fh to 0Ah, bit 01h deals with pages 09h to 04h and bit 0 deals with page 03h (OTP). Once the block-locking bits are set, the locking configuration for the corresponding memory area is frozen.



Important security: To activate the new locking configuration after a write to the lock bit area, a REQA or WUPA command must be carried out.

Fig 6. Lock bytes

In Figure 6 for example if BL15-10 is set to logic 1, then bits L15 to L10 (lock byte 2 bit[7:2]) can no longer be changed.

The locking and block-locking bits are set by a WRITE command to page 2. Bytes 2 and 3 of the WRITE command, and the contents of the lock bytes are bitwise OR'ed and the result then becomes the new contents of the lock bytes. This process is irreversible if a bit is set to logic 1, it cannot be changed back to logic 0.

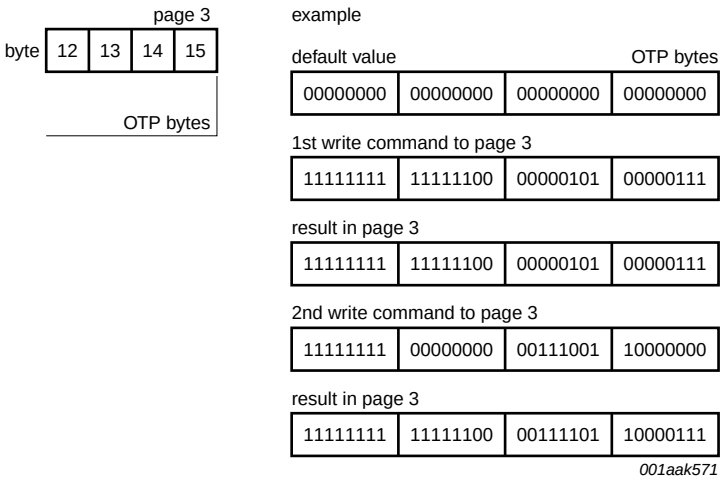
The contents of bytes 0 and 1 of page 2 are unaffected by the corresponding data bytes of the WRITE command.

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7.5.3 OTP bytes

Page 03h is the OTP page and it is preset so that all bits are set to logic 0 after production. These bytes can be bitwise modified using the WRITE command.



This memory area can be used as a 32 tick one-time counter.

Fig 7. OTP bytes

The WRITE command bytes and the current contents of the OTP bytes are bitwise OR'ed. The result is the new OTP byte contents. This process is irreversible and if a bit is set to logic 1, it cannot be changed back to logic 0.

7.5.4 Data pages

Pages 04h to 0Fh are the user read/write area.

After production the data pages are initialized to the following values:

- Page 04h is initialized to FFh
- Pages 05h to 15h are initialized to 00h

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7.6 Command set

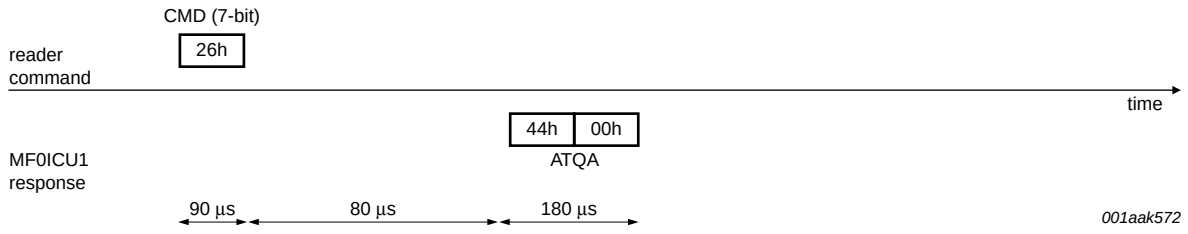
The MF0ICU1 comprises the following command set:

7.6.1 REQA

Table 6. REQA

Command	Code	Parameter	Data	Integrity mechanism	Response
REQA	26h (7-bit)	-	-	parity	ATQA 44 00h

The MF0ICU1 accepts the REQA command only in the idle state. The response is the 2-byte ATQA (44 00h). REQA and ATQA commands are fully implemented in accordance with ISO/IEC 14443-3.



Time units are not to scale and rounded off to the nearest 10 µs

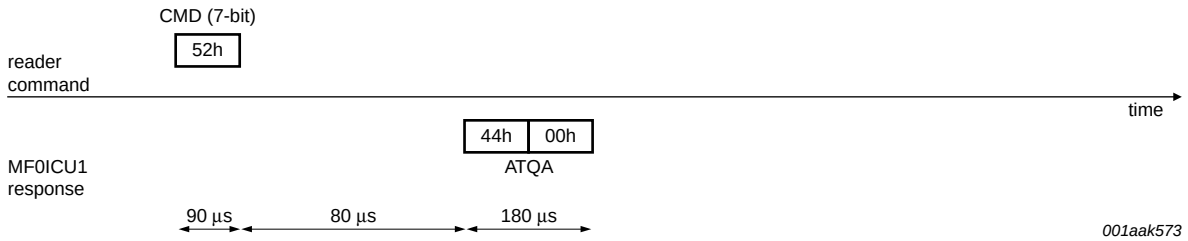
Fig 8. REQA

7.6.2 WUPA

Table 7. WUPA

Command	Code	Parameter	Data	Integrity mechanism	Response
WUPA	52h (7-bit)	-	-	parity	ATQA 44 00h

The MF0ICU1 accepts the WUPA command only in the idle and halt states. The response is the 2-byte ATQA (44 00h). WUPA command is fully implemented in accordance with ISO/IEC 14443-3.



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Fig 9. WUPA

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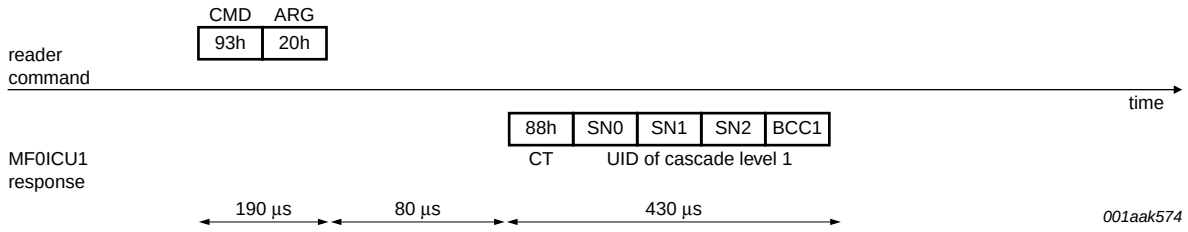
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7.6.3 Cascade level 1: ANTICOLLISION and SELECT commands

Table 8. Cascade level 1: ANTICOLLISION and SELECT commands

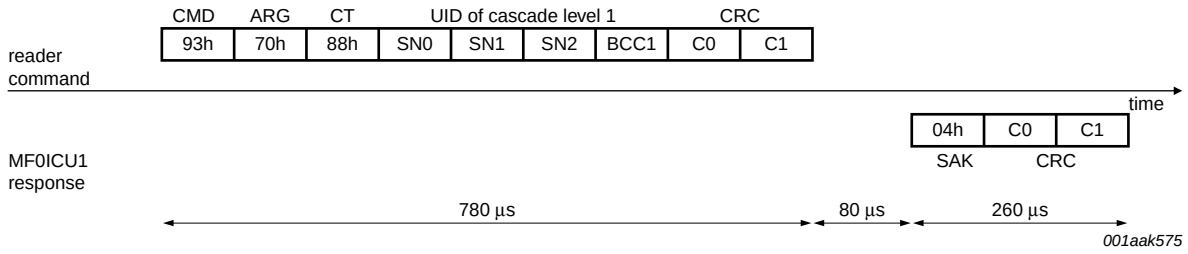
Command	Code	Parameter	Data	Integrity mechanism	Response
ANTICOLLISION	93h	20h to 67h	part of the UID	parity	parts of UID
SELECT	93h	70h	UID: first 3 bytes	parity, BCC, CRC	SAK (04h)

The ANTICOLLISION and SELECT commands are based on the same command code. Only the parameter byte is different. This byte is as the 70h definition in case of the SELECT command. The MF0ICU1 accepts these commands only in the Ready 1 state. The response is part 1 of the UID for the anticollision and SAK (04h) for SELECT.



Time units are not to scale and rounded off to the nearest 10 µs

Fig 10. Cascade level 1: ANTICOLLISION command



Time units are not to scale and rounded off to the nearest 10 µs

Fig 11. Cascade level 1: SELECT command

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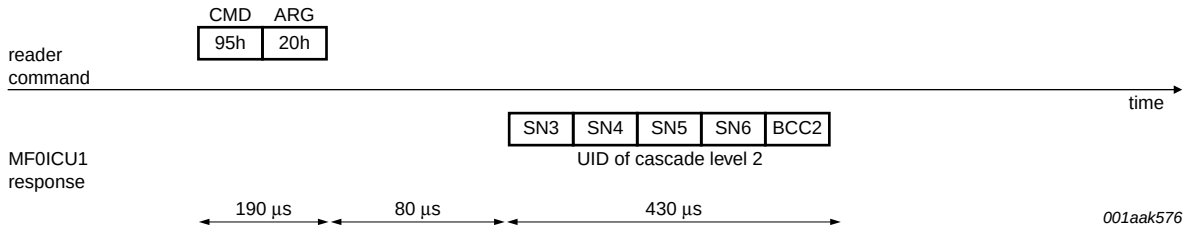
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7.6.4 Cascade level 2: ANTICOLLISION and SELECT commands

Table 9. Cascade level 2: ANTICOLLISION and SELECT commands

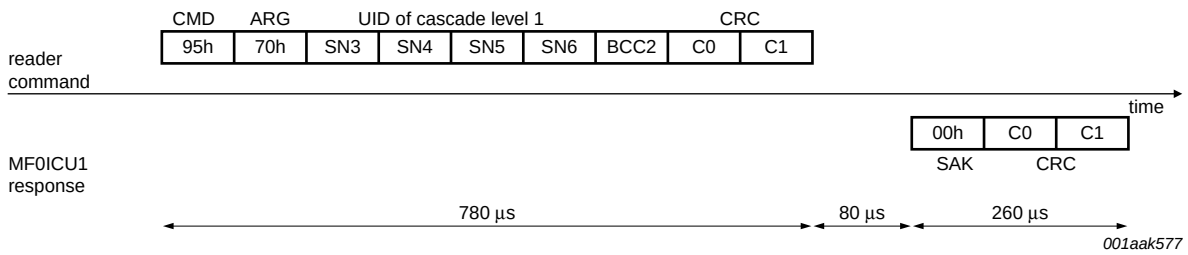
Command	Code	Parameter	Data	Integrity mechanism	Response
ANTICOLLISION	95h	20h to 67h	part of the UID	parity	parts of UID
SELECT	95h	70h	UID: second 4 bytes	parity, BCC, CRC	SAK (00h)

The ANTICOLLISION and SELECT commands are based on the same command code. Only the parameter byte is different. This byte is as the 70h definition in case of the SELECT command. The MF0ICU1 accepts these commands only in the Ready 2 state. The response is part 2 of the UID for the anticollision and SAK (04h) for SELECT.



Time units are not to scale and rounded off to the nearest 10 µs

Fig 12. Cascade level 2: ANTICOLLISION command



Time units are not to scale and rounded off to the nearest 10 µs

Fig 13. Cascade level 2: SELECT command

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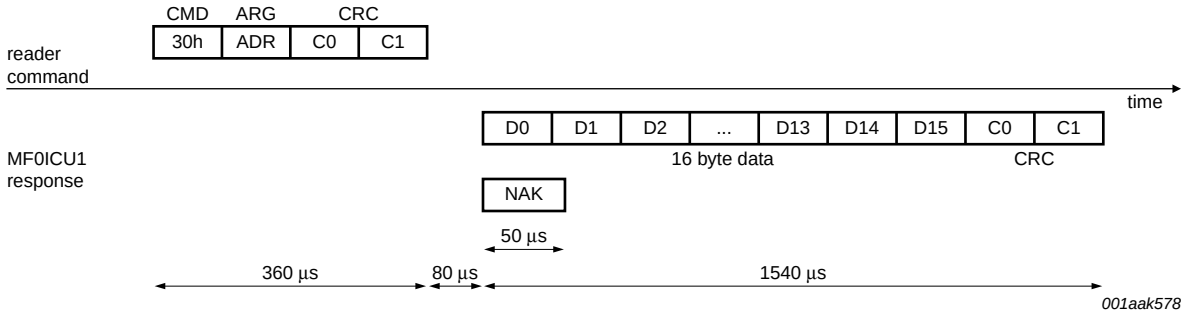
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7.6.5 READ

Table 10. READ

Command	Code	Parameter address	Data	Integrity mechanism	Response
READ	30h	00h to 0Fh	-	CRC	16-byte Date

The READ command needs the page address as a parameter. Only addresses 00h to 0Fh are decoded. The MF0ICU1 returns a NAK for higher addresses. The MF0ICU1 responds to the READ command by sending 16 bytes starting from the page address defined by the command argument. For example; if address (ADR) is 03h then pages 03h, 04h, 05h, 06h are returned. A roll-back is implemented for example; if address (ADR) is 0Eh, then the contents of pages 0Eh, 0Fh, 00h and 01h are returned).



Time units are not to scale and rounded off to the nearest 10 µs

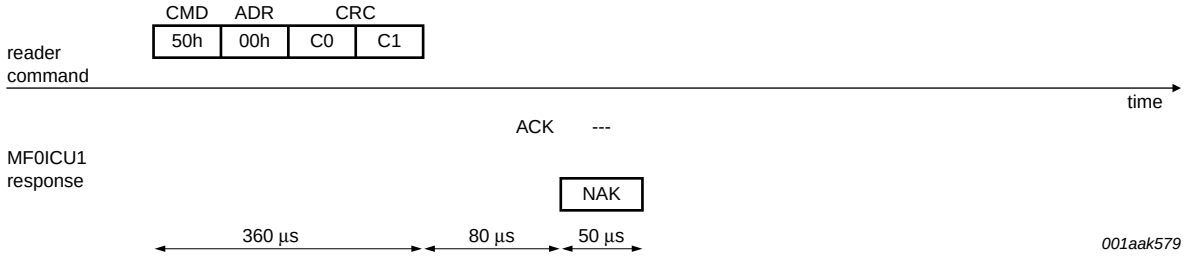
Fig 14. READ

7.6.6 HALT

Table 11. HALT

Command	Code	Parameter address	Data	Integrity mechanism	Response
HALT	50h	00h	-	parity, CRC	passive ACK, NAK

The HALT command is used to set the MF0ICU1 ICs into a different wait state (halt instead of idle), enabling devices whose UIDs are already known because they have passed the anticollision procedure, to be separated from devices yet to be identified by their UIDs. This mechanism is a very efficient way of finding all contactless devices in the PCD field.



Time units are not to scale and rounded off to the nearest 10 µs

Fig 15. HALT

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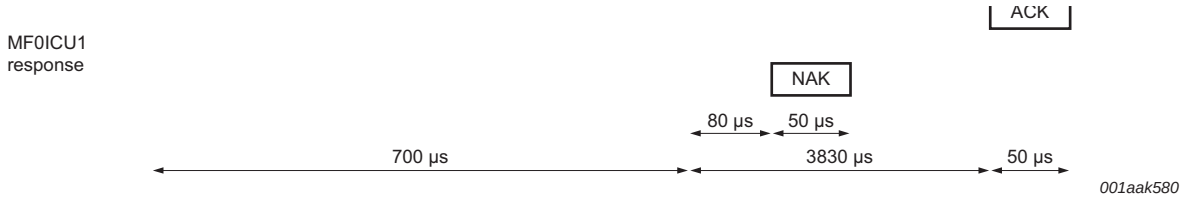
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7.6.7 WRITE

Table 12. WRITE

Command	Code	Parameter address	Data	Code	Parameter
WRITE	A2h	00h to 0Fh	4-byte	A2h	0 to 7

The WRITE command is used to program the lock bytes in page 02h, the OTP bytes in page 03h and the data bytes in pages 04h to 0Fh. A WRITE command is performed page-wise, programming 4 bytes in a row.



Time units are not to scale and rounded off to the nearest 10 µs

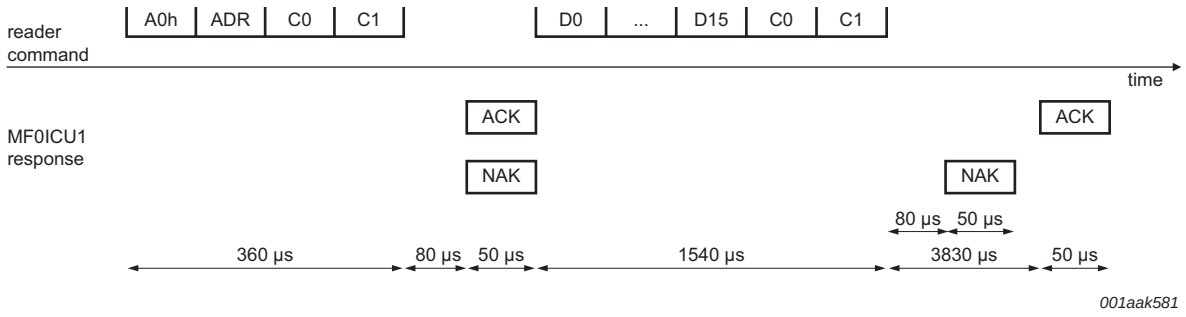
Fig 16. WRITE

7.6.8 COMPATIBILITY WRITE

Table 13. COMPATIBILITY WRITE

Command	Code	Parameter address	Data	Integrity mechanism	Response
COMPATIBILITY WRITE	A0h	00h to 0Fh	16-byte	parity, CRC	ACK or NAK

The COMPATIBILITY WRITE command was implemented to accommodate the established MIFARE PCD infrastructure. Even though 16 bytes are transferred to the MF0ICU1, only the least significant 4 bytes (bytes 0 to 3) are written to the specified address. It is recommended to set the remaining bytes 04h to 0Fh to all logic 0.



Time units are not to scale and rounded off to the nearest 10 µs

Fig 17. COMPATIBILITY WRITE

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7.7 Summary of relevant data for device identification

Table 14. Summary of relevant data for device identification

Code	Type	Value	Binary Format	Remark
ATQA	2-byte	44h	0000 0000 0100 0100; 1st 1 indicates cascade level 2 2nd 1 indicates MIFARE family	hard coded
CT	1-byte	88h	1000 1000	hard coded
	cascade tag		ensures collision with cascade level 1 products	
SAK (cascade level 1)	1-byte	04h	0000 0100; 1 indicates additional cascade level	hard coded
SAK (cascade level 2)	1-byte	00h	0000 0000; indicates complete UID and MF0ICU1 functionality	hard coded
manufacturer Byte	1-byte	04h	0000 0100; indicates manufacturer NXP Semiconductors	in accordance with ISO/IEC 14443-3 and ISO/IEC 7816-6 AMD.1

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8. Limiting values

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134)[1]

Symbol	Parameter	Conditions		Min	Max[2][3]	Unit
I_I	input current			-	30	mA
T_{stg}	storage temperature			−55	125	°C
T_{amb}	ambient temperature			−25	70	°C
V_{ESD}	electrostatic discharge voltage	measured between pins LA and LB	[4]	2	-	kV
I_{lu}	latch-up current			±100	-	mA

[1] Exposure to limiting values for extended periods may affect device reliability.

[2] Stresses above one or more of the limiting values may cause permanent damage to the device.

[3] These are stress ratings only. Operation of the device at these or any other conditions above those given in Section 9.1 of the specification is not implied.

[4] JEDEC norm JESD22-A114; Human body model: C = 100 pF, R = 1.5 kΩ.

9. Characteristics

9.1 Electrical characteristics

Table 16. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			-	13.56	-	MHz
C_i	input capacitance	17 pF version	[1]	14.85	17.0	20.13	pF
		50 pF version	[1]	42.5	50.0	57.5	pF
EEPROM characteristics							
$t_{cy(W)}$	write cycle time			-	3.8	-	ms
t_{ret}	retention time	T_{amb} = 22 °C		5	-	-	year
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C		10000	-	-	cycle

[1] LCR meter HP 4285: T_{amb} = 22 °C, Cp-D, f_i = 13.56 MHz, 2 Veff.

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10. Wafer specification

For more details on the wafer delivery forms see Ref. 8.

Table 17. Specifications

Wafer	
diameter	200 mm (8 inches)
maximum diameter after foil expansion	210 mm
die separation process	laser dicing
thickness	120 μm ±15 μm (U7DL types)
	75 μm ±10 μm (S7DL types)
flatness	not applicable
Potential Good Dies per Wafer (PGDW)	72778
Wafer underside	
material	Si
flatness	not applicable
roughness	R_a max = 0.5 μm
	R_t max = 5 μm
Chip dimensions	
step size[1]	x = 645 μm
	y = 665 μm
gap between chips[1]	typical = 20 μm
	minimum = 5 μm
Passivation	
type	sandwich structure
material	PSG/nitride (on top)
thickness	500 nm/600 nm
Au bump (substrate connected to VSS)	
material	99.9 % pure Au
hardness	35 to 80 HV 0.005
shear strength	>70 MPa
height	18 μm
height uniformity	within a die = ±2 μm
	within a wafer = ±3 μm
	wafer to wafer = ±4 μm
flatness	minimum = ±1.5 μm
size	LA, LB = 90 μm × 90 μm
	VSS, TESTIO[2] = 60 μm × 60 μm
size variation	±5 μm
under bump metallization	sputtered TiW

[1] The step size and the gap between chips may vary due to changing foil expansion

[2] Pads VSS and TESTIO are disconnected when wafer is sawn.

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10.1 Fail die identification

The wafers are not inked.

Electronic wafer mapping (SECS II format) covers the electrical test results and the additional mechanical/visual inspection results.

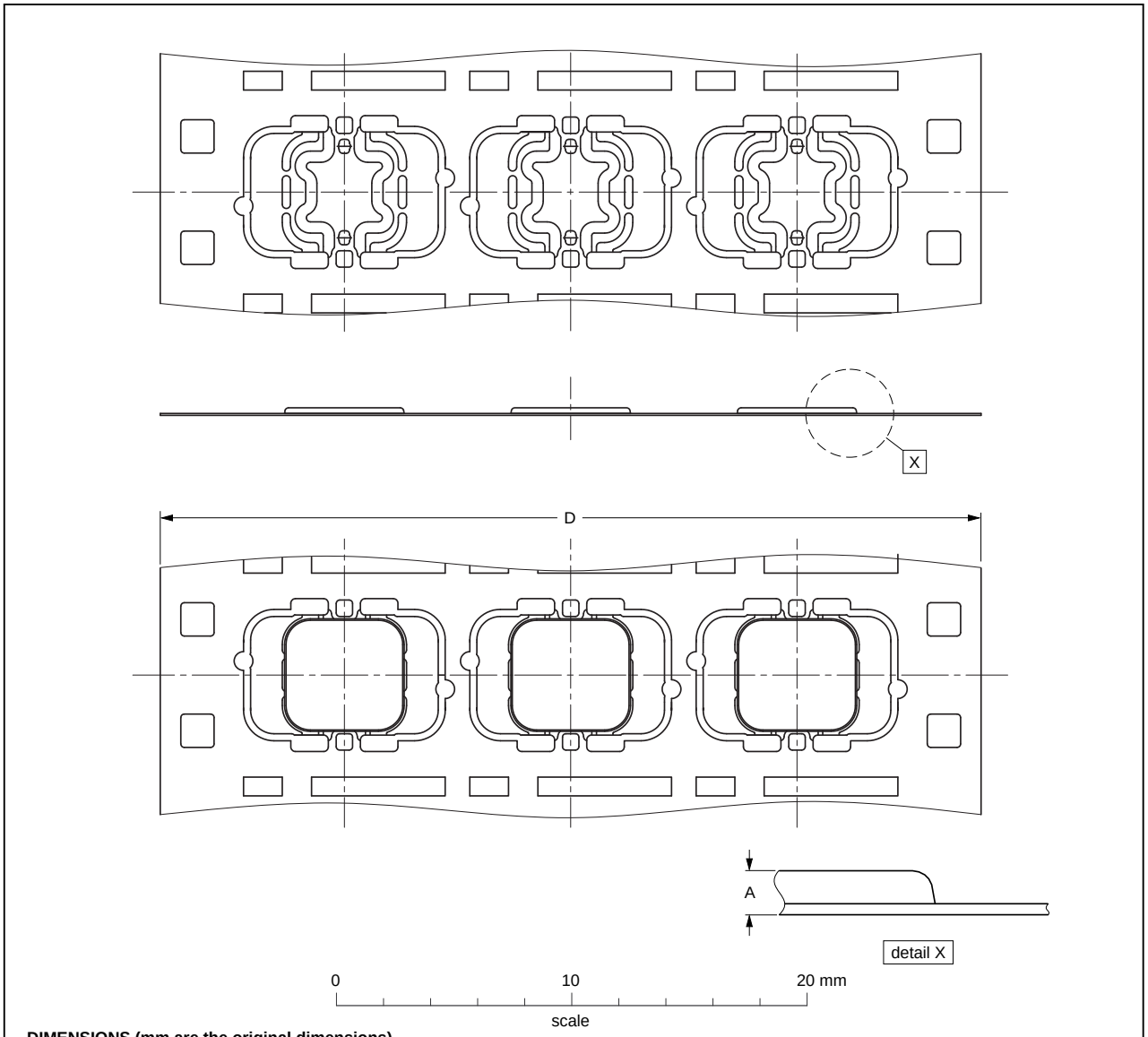
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11. Package outline

For further details on the contactless module MOA4 please refer to Ref. 7.

PLLMC: plastic leadless module carrier package; 35 mm wide tape **SOT500-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	D	
mm	0.33	35.05 34.95	For unspecified dimensions see PLLMC-drawing given in the subpackage code.

Note

1. Total package thickness, exclusive punching burr.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT500-2	- - -	- - -	- - -			~~03-09-17~~ 06-05-22

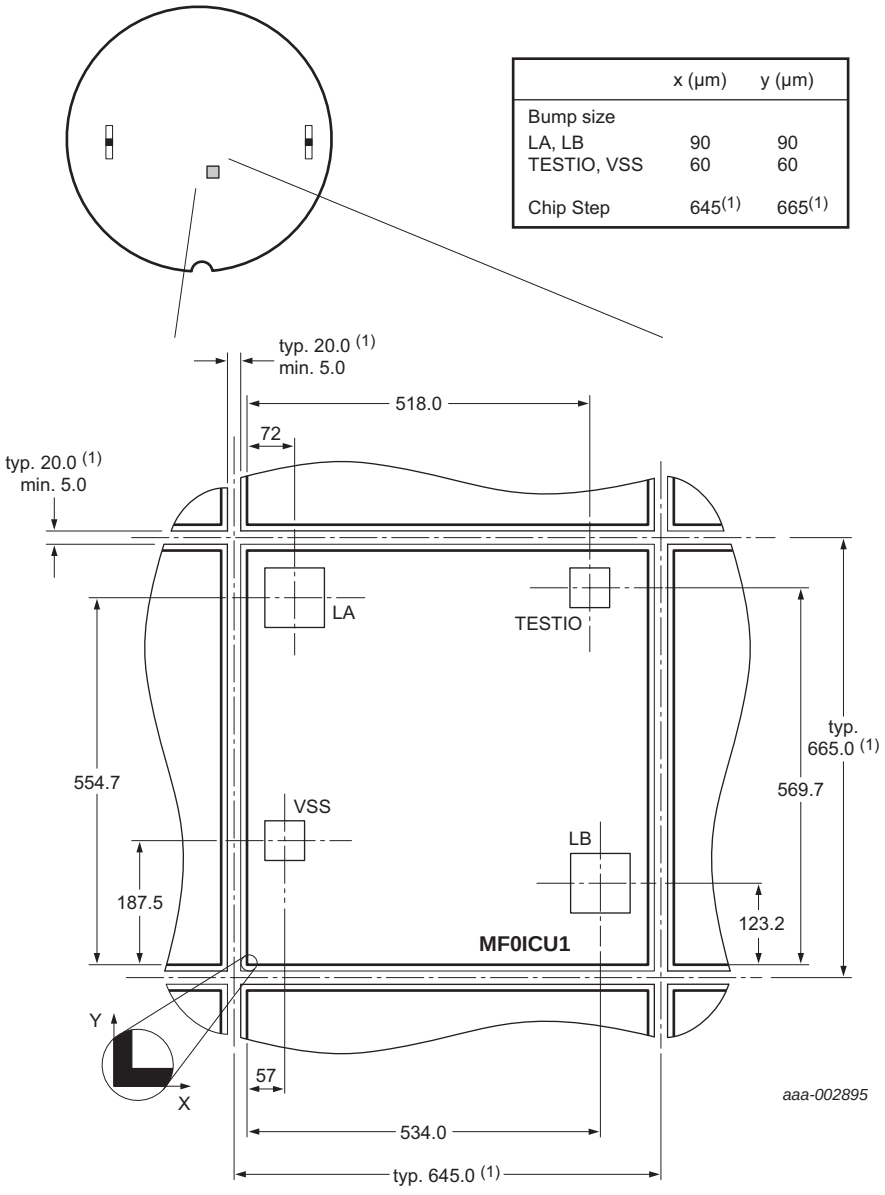
Fig 18. Package outline SOT500-2

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12. Bare die outline

For more details on the wafer delivery forms, see Ref. 8.



Note
(1) The air gap and thus the step size may vary due to varying foil expansion
(2) All dimensions in µm, pad locations measured from metal ring edge (see detail)

Fig 19. Bare die outline

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13. Abbreviations

Table 18. Abbreviations

Acronym	Description
ARG	Argument
ATQA	Answer To Request (type A)
BCC	Block Check Character
CMD	Command
CRC	Cyclic Redundancy Check
CT	Cascade Tag
EEPROM	Electrically Erasable Programmable Read-Only Memory
LSB	Least Significant Bit
MSB	Most Significant Bit
NAK	Negative Acknowledge
OTP	One-Time Programmable
Passive ACK	Passive (implicit) ACKnowledge without PICC answer
PCD	Proximity Coupling Device
PGDW	Potential Good Dies per Wafer
PICC	Proximity Integrated Circuit Card
POR	Power-On Reset
REQA	Request Answer (type A)
RF	Radio Frequency
SAK	Select ACKnowledge (type A)
UID	Unique IDentifier/IDentification
WUPA	Wake-UP command (type A)

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14. References

[1] **ISO/IEC 14443 A —** International Organization for Standardization/International Electrotechnical Commission: Identification cards - Contactless integrated circuit(s) cards - Proximity cards, part 1-4, Type A

[2] **MIFARE Interface Platform Type Identification Procedure —** Application note, BL-ID Document number 0184, Version number **[1]

[3] **MIFARE ISO/IEC 14443 PICC Selection —** Application note, BL-ID Document number 1308, Version number **[1]

[4] **MIFARE Ultralight Features and Hints —** Application note, BL-ID Document number 0731, Version number **[1]

[5] **MIFARE Ultralight as Type 2 Tag —** Application note, BL-ID Document number 1303, Version number **[1]

[6] **MIFARE (Card) Coil Design Guide —** Application note, BL-ID Document number 0117, Version number **[1]

[7] **Contactless smart card module specification MOA4 —** Delivery Type Description, BU-ID Document number 0823**[1]

[8] **General specification for 8" wafer on UV-tape with electronic fail die marking; delivery types —** Delivery Type Description, BU-ID Document number 1093**[1]

1. ** ... document version number

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15. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MF0ICU1 v.3.9	20140723	Product data sheet	-	MF0ICU1_38
Modifications:	• Figure 19 “Bare die outline”: updated • Corrected typo in Section 7.5.2 “Lock bytes” Lock Bytes for the block locking bit 2 • Corrected wafer thickness tolerance for 75 μm thin wafers • Corrected bump size for VSS pad • Corrected reference Ref. 8 to wafer delivery with electronic fail die marking • New template structure applied • Editorial changes			
MF0ICU1 v.3.8	20101222	Product data sheet	-	MF0ICU1_37
Modifications:	• Unit of write endurance corrected in cycles			
MF0ICU1_37	20100414	Product data sheet	-	028636
Modifications:	• Figure 4 “Chip orientation and bondpad locations”: format updated			
028636	20100212	Product data sheet	-	028635
Modifications:	• Updated information on memory content after production • Information on laser dicing types included (no separate wafer addendum needed) • Packaging information included • Fig. 4 “Chip orientation and bondpad locations”: format updated • Multiple minor changes • Section 5 “Legal information”: updated			
028635	20080820	Product data sheet	-	028634
Modifications:	• Section 1 “General description” and Section 2 “Features”: rephrasing of sentences			
028634	20080204	Product data sheet	-	028633
Modifications:	• Update • General rewording of MIFARE designation and commercial conditions			
028633	July 2008	Product data sheet	-	028632
Modifications:	• exchange of figures 11 and 13			
028632	April 2007	Product data sheet	-	028631
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name.			
028631	March 2007	Product data sheet	-	028630
028630	March 2003	Product data sheet	-	028625
028625	March 2003	Preliminary data sheet	-	028624
028624	February 2003	Preliminary data sheet	-	028623
028623	January 2003	Preliminary data sheet	-	028622
028622	January 2003	Preliminary data sheet	-	028621
028621	January 2003	Preliminary data sheet	-	028620
028620		Preliminary data sheet	-	028610

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Table 19. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
028610		Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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