BLA8G1011L(S)-300; BLA8G1011L(S)-300G

Power LDMOS transistor

AMPLEON

Rev. 4 — 4 August 2016

Product data sheet

1. Product profile

1.1 General description

300 W LDMOS power transistor for avionics applications at frequencies from 1030 MHz to 1090 MHz.

Table 1. Test information

Typical RF performance at T_{case} = 25 °C in a class-AB production test circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D	t_r	t_f
	(MHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
pulsed RF	1060	32	300	16.5	56	14	5

1.2 Features and benefits

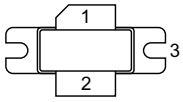
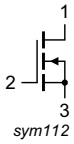
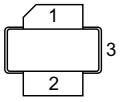
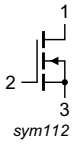
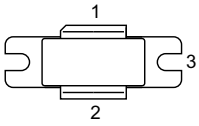
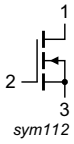
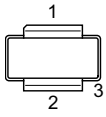
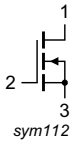
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1030 MHz to 1090 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Avionics transmitter applications in the 1030 MHz to 1090 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLA8G1011L-300 (SOT502A)			
1	drain		
2	gate		
3	source [1]		
BLA8G1011LS-300 (SOT502B)			
1	drain		
2	gate		
3	source [1]		
BLA8G1011L-300G (SOT502F)			
1	drain		
2	gate		
3	source [1]		
BLA8G1011LS-300G (SOT502E)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA8G1011L-300	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLA8G1011LS-300	-	earless flanged ceramic package; 2 leads	SOT502B
BLA8G1011L-300G	-	eared flanged ceramic package; 2 leads; 2 mounting holes	SOT502F
BLA8G1011LS-300G	-	earless flanged ceramic package; 2 leads	SOT502E

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4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 25 °C; t_p = 10 μs; δ = 10 %	0.112	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 4.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 450 mA	1.5	1.8	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	67.9	82	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 450 mA	2.67	3.92	5.25	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 15.75 A	0.008	0.04	0.079	Ω

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 50 μs; δ = 2 %; V_{DS} = 32 V; f = 1060 MHz; I_{Dq} = 150 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit for straight leads.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 300 W	15	16.5	-	dB
RL_{in}	input return loss	P_L = 300 W	-	−16	−11	dB
η_D	drain efficiency	P_L = 300 W	52	56	-	%
t_r	rise time	P_L = 300 W	-	14	-	ns
t_f	fall time	P_L = 300 W	-	5	-	ns

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7. Test information

7.1 Ruggedness in class-AB operation

The BLA8G1011L-300, BLA8G1011LS-300, BLA8G1011L-300G and BLA8G1011LS-300G are enhanced rugged devices and are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: t_p = 50 μs; δ = 2 %; V_{DS} = 32 V; I_{Dq} = 100 mA; P_L = 300 W; f = 1030 MHz to 1090 MHz.

7.2 Impedance information

Table 8. Typical impedance

Typical values unless otherwise specified.

f	Z_S	Z_L
(MHz)	(Ω)	(Ω)
1000	2.84 – j3.69	0.80 – j1.00
1050	3.98 – j3.26	0.62 – j1.26
1100	5.22 – j2.92	0.66 – j1.17

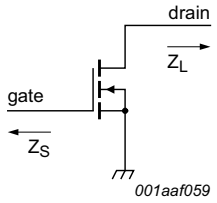
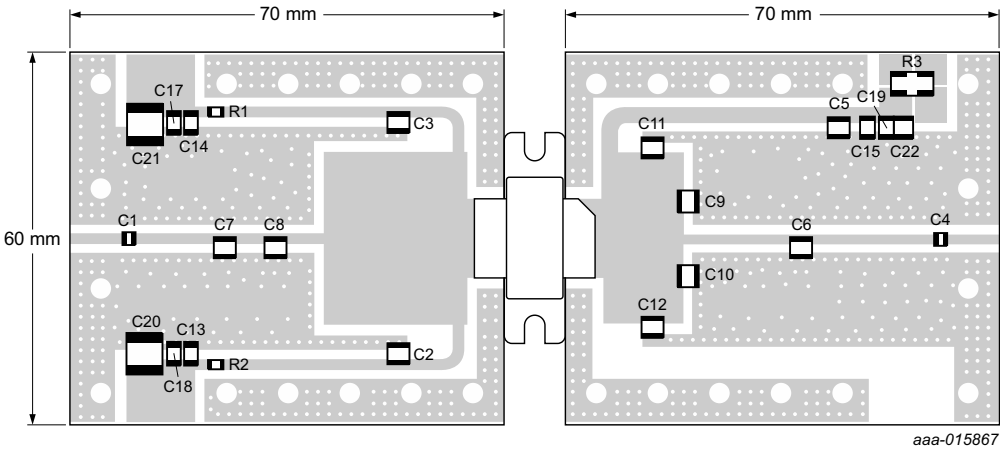


Fig 1. Definition of transistor impedance

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7.3 Test circuit



Printed-Circuit Board (PCB): Rogers 4350B; ε_r = 3.66; thickness = 0.765 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 2. Component layout

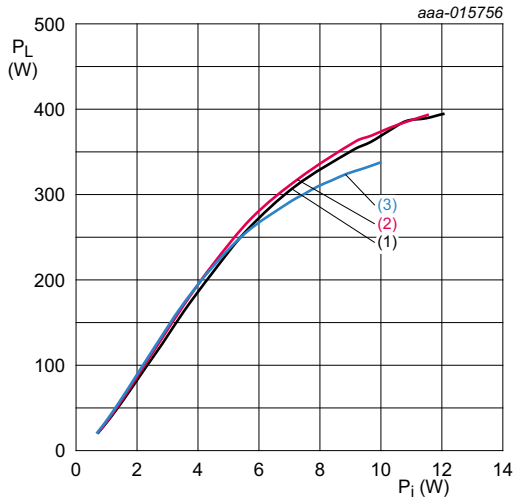
Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C4	multilayer ceramic chip capacitor	91 pF	ATC: ATC100A910FT150XT
C2, C3, C5	multilayer ceramic chip capacitor	39 pF	ATC: ATC100B390FT500XTV
C6	multilayer ceramic chip capacitor	1.5 pF	ATC: ATC800B1R5BT500XTV
C7	multilayer ceramic chip capacitor	3.3 pF	ATC: ATC100B3R3BT500XTV
C8	multilayer ceramic chip capacitor	2.4 pF	ATC: ATC100B2R4BT500XTV
C9, C10	multilayer ceramic chip capacitor	0.6 pF	ATC: ATC100B0R6BT500XTV
C11, C12	multilayer ceramic chip capacitor	2.7 pF	ATC: ATC100B2R7BT500XTV
C13, C14, C15	multilayer ceramic chip capacitor	0.1 μF	Murata: GRM31C5C1H104JA01K
C17, C18, C19	multilayer ceramic chip capacitor	1 μF	Murata: GRM31MR71H105KA88L
C20, C21	multilayer ceramic chip capacitor	4.7 μF	TDK: C5750X7R2A475K230KA
C22	multilayer ceramic chip capacitor	4.7 μF	Murata: GRM32ER71H475KA88L
R1, R2	SMD resistor	9.1 Ω	Yageo: RC0805FR-079R1L
R3	SMD resistor	0.01 Ω	Ohmite: LVK25R010FER

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7.4 Graphical data



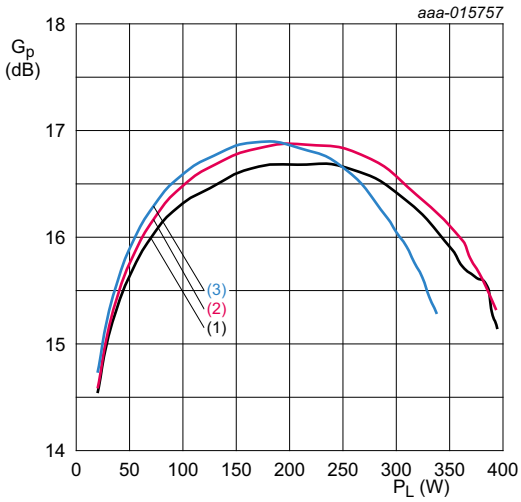
V_{DS} = 32 V; I_{Dq} = 150 mA; t_p = 50 μs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1060 MHz

(3) f = 1090 MHz

Fig 3. Output power as a function of input power; typical values



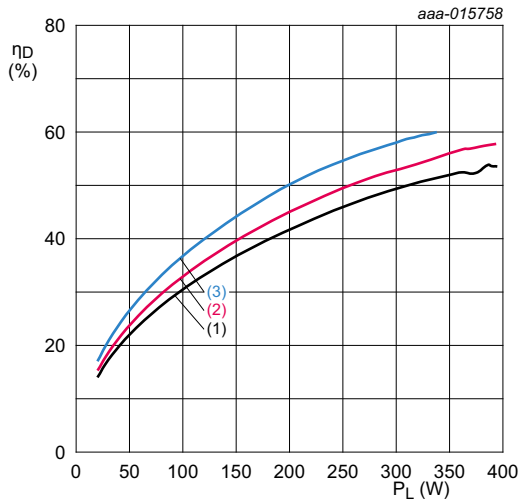
V_{DS} = 32 V; I_{Dq} = 150 mA; t_p = 50 μs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1060 MHz

(3) f = 1090 MHz

Fig 4. Power gain as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 150 mA; t_p = 50 μs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1060 MHz

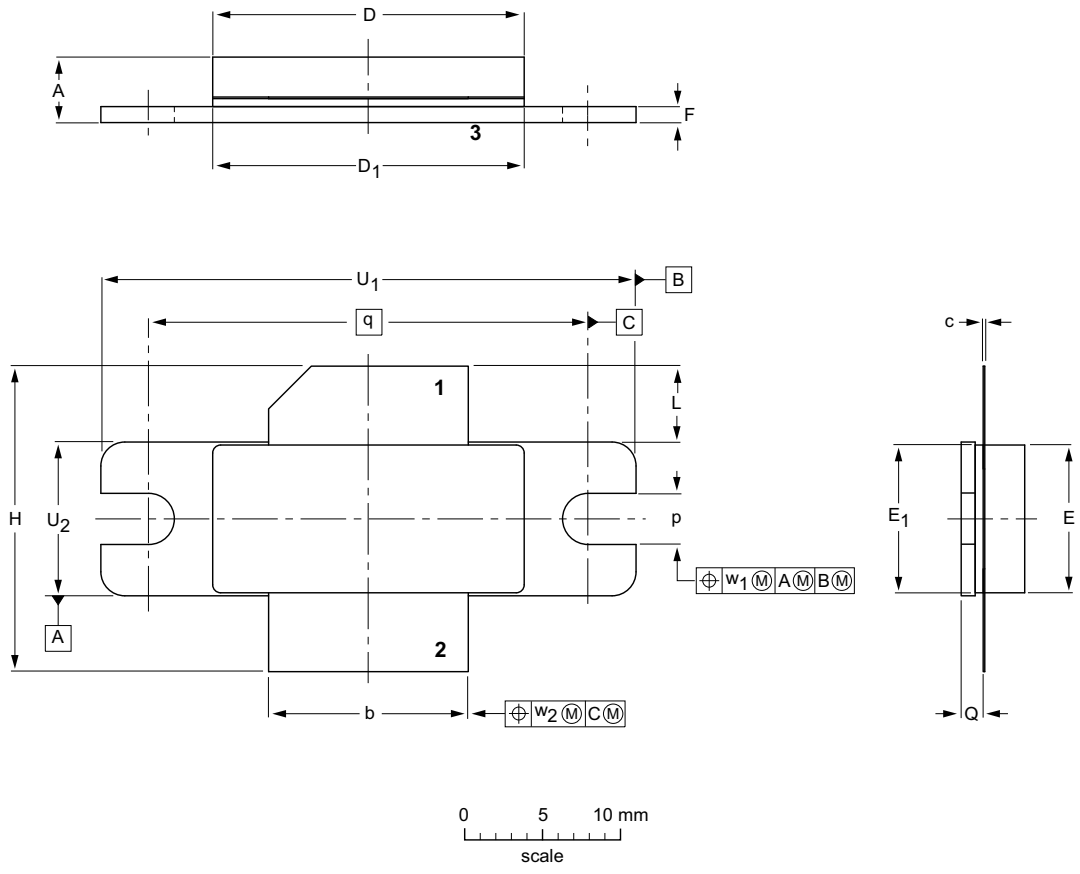
(3) f = 1090 MHz

Fig 5. Drain efficiency as a function of output power; typical values

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8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

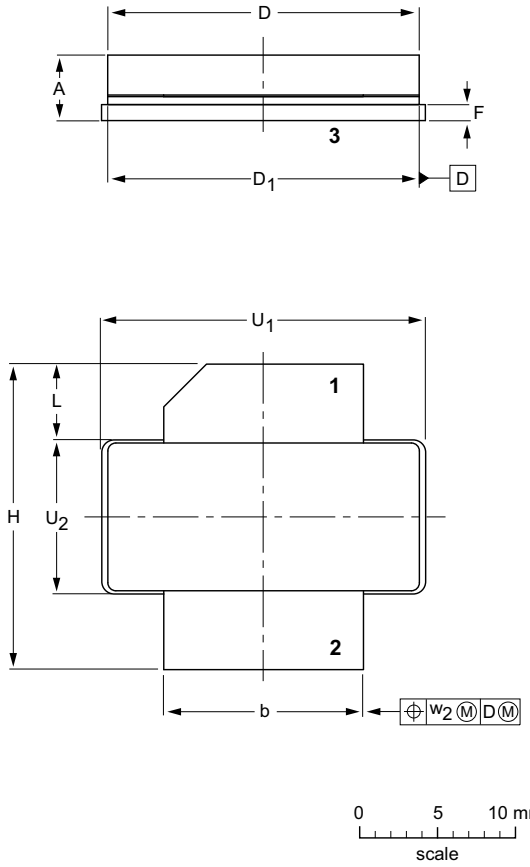
UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 6. Package outline SOT502A

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Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

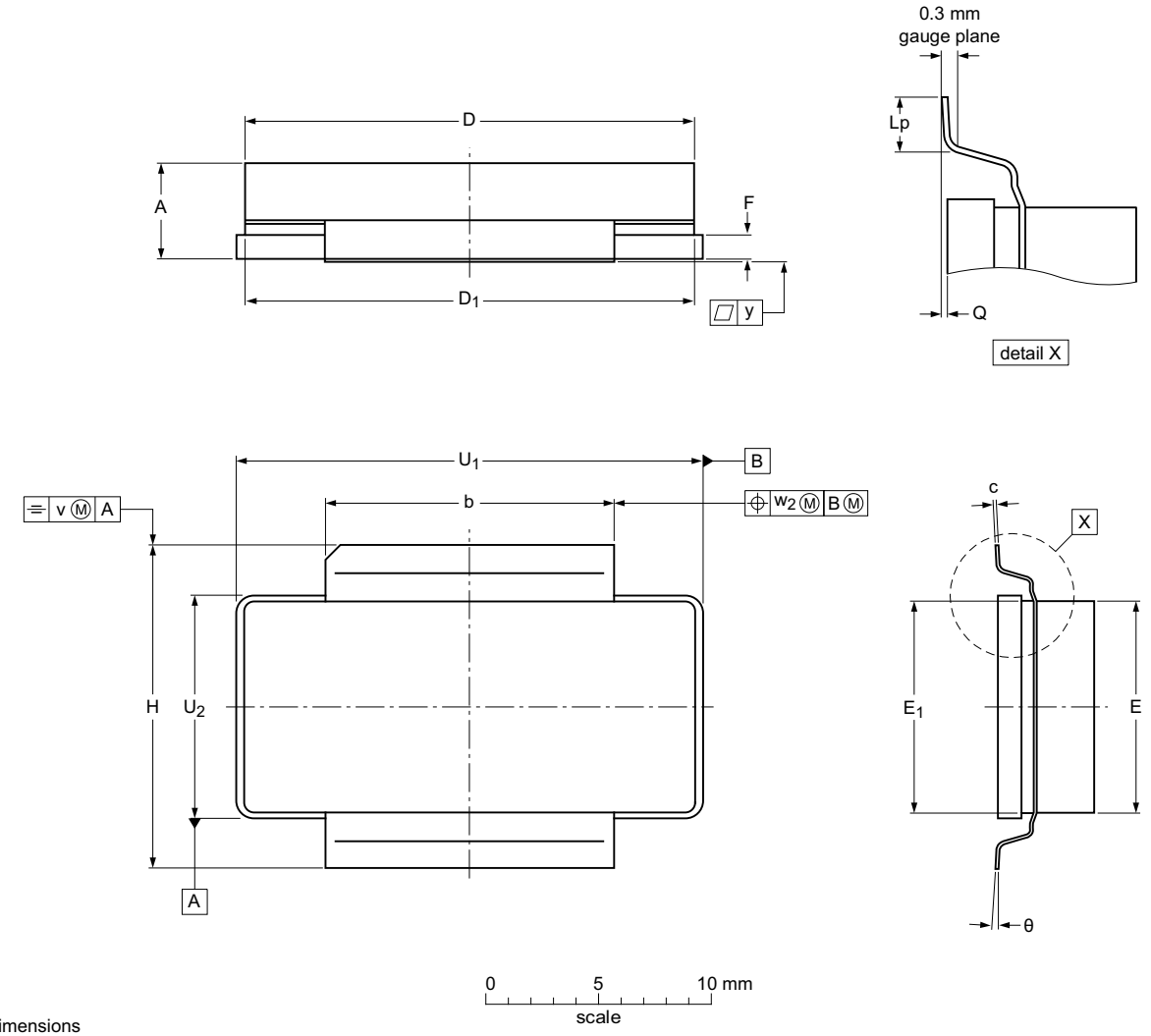
UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 7. Package outline SOT502B

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Earless flanged ceramic package; 2 leads **SOT502E**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	L_p	Q	U_1	U_2	v	w_2	y	θ
mm	max	4.72	12.83	0.15	20.02	19.96	9.53	9.53	1.14	14.3	1.38	0.195	20.70	9.91	0.25	0.25	0.15	7°
	nom																	
	min	3.43	12.57	0.07	19.61	19.66	9.27	9.27	0.89	14.1	0.98	0.055	20.45	9.65				0°
inches	max	0.185	0.505	0.006	0.788	0.786	0.375	0.375	0.045	0.563	0.055	0.008	0.815	0.390	0.010	0.010	0.006	7°
	nom																	
	min	0.135	0.495	0.003	0.772	0.774	0.365	0.365	0.035	0.555	0.039	0.002	0.805	0.380				0°

Note
1. Millimeter dimensions are derived from the original inch dimensions.

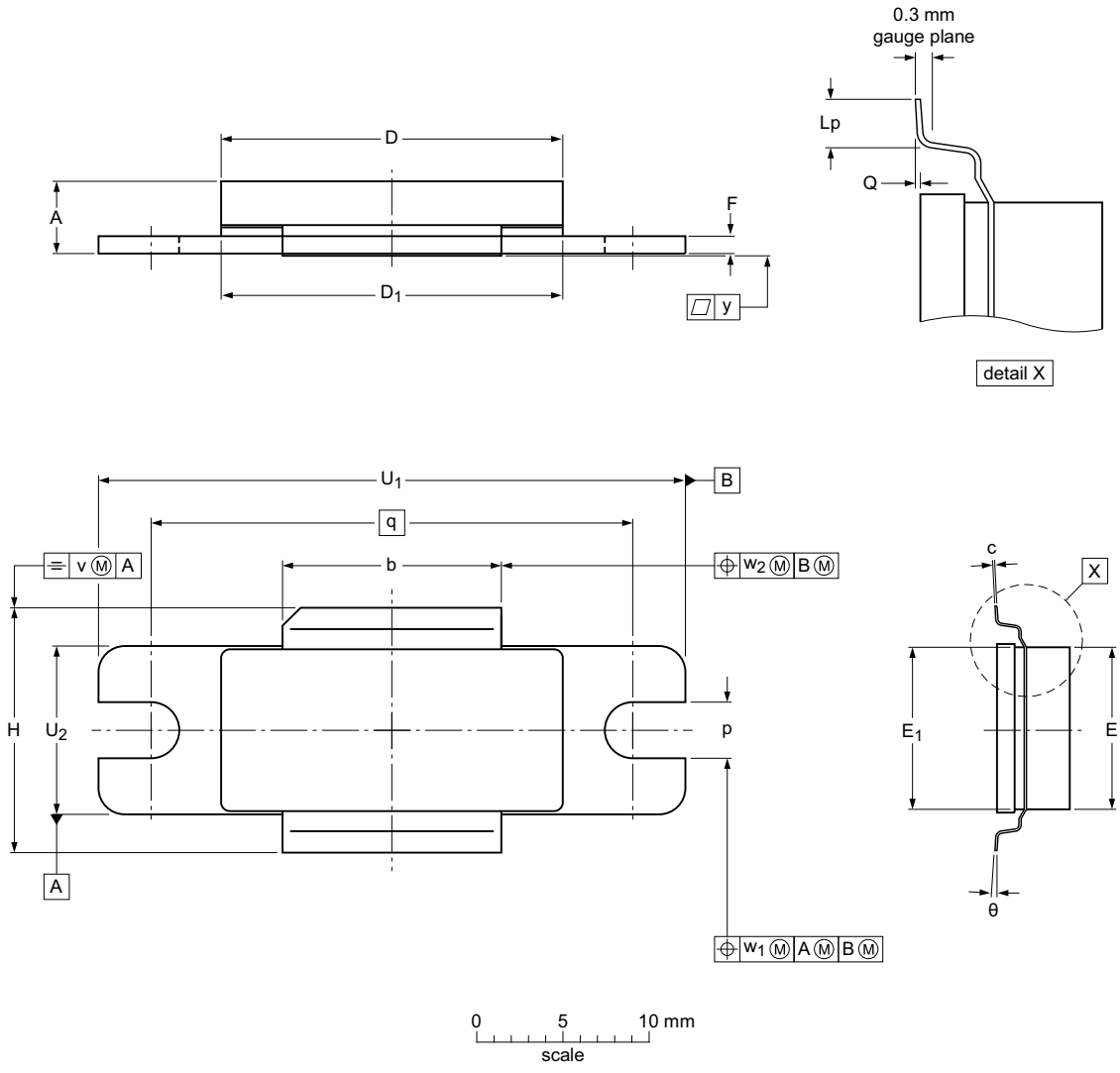
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Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT502E						~~12-05-14~~ 12-05-30

Fig 8. Package outline SOT502E

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Eared flanged ceramic package; 2 leads; 2 mounting holes **SOT502F**



Dimensions (mm are the original dimensions)

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	L_p	p	Q	q	U_1	U_2	v	w_1	w_2	θ	U1
mm	max	4.70	12.83	0.15	20.02	19.96	9.53	9.53	1.14	14.3	1.38	3.38	0.195		34.16	9.91				7°	
	nom													27.94			0.25	0.25	0.25		0.15
	min	3.43	12.57	0.07	19.61	19.66	9.27	9.27	0.89	14.1	0.98	3.12	0.055		33.91	9.65				0°	

sot502f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT502F						~~14-02-19~~ 14-03-14

Fig 9. Package outline SOT502F

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA8G1011L-300_LS-300_L-300G_LS-300G v.4	20160804	Product data sheet		BLA8G1011L-300_LS-300_L-300G_LS-300G v.3
Modifications:	• Table 9 on page 5: row 4 to row 7, value units corrected from nF to pF			
BLA8G1011L-300_LS-300_L-300G_LS-300G v.3	20150901	Product data sheet		BLA8G1011L-300_LS-300_L-300G_LS-300G v.2
BLA8G1011L-300_LS-300_L-300G_LS-300G v.2	20150126	Product data sheet		BLA8G1011L-300_LS-300_L-300G_LS-300G v.1
BLA8G1011L-300_LS-300_L-300G_LS-300G v.1	20140929	Objective data sheet		-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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